1/2.5-Inch, 5-Megapixel CMOS Digital Image Sensor Die

MT9P014 Wafer Data Sheet

For latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Support for external mechanical shutter
- Support for external LED or xenon flash
- High frame rate preview mode with arbitrary downsize scaling from maximum resolution
- Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning
- Data interface: CCP2-compliant, sub-low-voltage differential signalling (sub-LVDS) or single/dual lane serial mobile industry processor interface (MIPI)
- On-die phase-lock-loop (PLL) oscillator
- Bayer pattern down-size scaler
- Integrated color and lens shading correction
- One-time programmable (OTP) memory for storing module information
- Superior low-light performance
- Position and color-based shading correction

General Physical Specifications

- Die thickness: 200µm ±12µm
- Wafer thickness: 750µm ±25µm
  (Consult factory for other thickness)
- Back side wafer surface of bare silicon
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 3.1kÅ
- Typical metal 4 thickness: 4.15kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Die Database

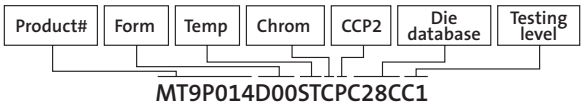
- Die outline, see Figure 3 on page 11
- Die size (stepping interval)
  – 7,725.05µm x 6,889.25µm
- Singulated die size: 7,683 ±25µm x 6,847 ±25µm
- Bond Pad Location and Identification Tables, see pages 7–10

Options	Designator
• Form	
– Die	D
– Wafer	W
• Testing	
– Standard (level 1) probe	C1

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Order Information

Die:	MT9P014D00STCP C28CC1 (CCP2)
Die:	MT9P014D00STCM C28CC1 (MIPI)
Wafer:	MT9P014W00STCP C28CC1 (CCP2)
Wafer:	MT9P014W00STCM C28CC1 (MIPI)



Key Performance Parameters

- Optical format: 1/2.5-inch (4:3)
- Active imager size: 5.70mm(H) x 4.28mm(V), 7.13mm diagonal
- Active pixels: 2592H x 1944V
- Pixel size: 2.2 x 2.2µm
- Chief ray angle: 29.02° maximum
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS) with global reset release (GRR)
- Input clock frequency: 6–27 MHz
- Maximum data rate
  – CCP2: 650 Mbps
  – MIPI: 768 Mbps per lane

Key Performance Parameters (continued)

- Frame rate
  - Full resolution: 15 fps
  - VGA (640H x 480V) with 2X skip and 2X bin: 70 fps
  - HD: 720 at 60 fps and 1080 at 30 fps
- ADC resolution: 12-bit, on-die
- Responsivity: 0.8V/lux-sec (at 550nm)
- Dynamic range: 69db
- SNR MAX: 39db
- Supply voltage
  - I/O digital: 1.7–1.9V (1.8V nominal)
  - Digital: 1.7–1.9V (1.8V nominal)
  - Analog: 2.4–3.1V (2.8V nominal)
- Power consumption
  - Full resolution: 332mW at 1.8V/2.8V (T_J = ambient, CCP2 = 640 Mbps, 15 fps, RAW 8)
  - Standby: 69.8µW at 1.8V/2.8V (T_J = ambient, hard standby, clock off)
- Operating temperature: –30°C to +70°C (at junction)

General Description

The Aptina™ MT9P014 is a 1/2.5-inch format CMOS active-pixel digital image sensor die with a pixel array of 2592H x 1944V (2608H x 1960V including border pixels). It incorporates sophisticated on-die camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9P014 digital image sensor die features our breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

When operated in its default mode, the sensor generates a full resolution image at 15 frames per second (fps). An on-die analog-to-digital converter (ADC) generates a 12-bit value for each pixel.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's standard package. Since the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

These specifications are provided for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9P014 imager die has 53 bond pads. Refer to Table 1 and 2 on pages 7–10 for a complete list of bond pads and coordinates.

The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 5 and Figure 2 on page 6 show the MT9P014 typical die connections. For low-noise operation, the MT9P014 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9P014 also supports different digital core (V_{DD}/D_{GND}) and I/O power ($V_{DD}IO$/D_{GND}) power domains that can be at different voltages. The PLL requires a clean power source (V_{DD}_PLL).

Wafer Saw

The die size (stepping interval) provided is measured from the center of the die street on one side of the die to the center of the die street on the other side of the die. A singulated die is approximately 42µm smaller in length and width. The dimensional tolerance of a singulated die is ±25µm. For example, if the die width (stepping interval) is 5,080µm and the die length (stepping interval) is 7,620µm, the dimensions of the singulated die will be 5,038µm ±25µm by 7,578µm ±25µm.

Wafer-Level Processing

Customers should choose the wafer form when post-processing of die is required. This includes adding extra passivation or metal layers or bumping of the bond pads. For these customers, the street widths are provided in Table 3 on page 12. Also, a reference from the center of bond pad 1 to the center of the intersection of two streets is provided for easy alignment.

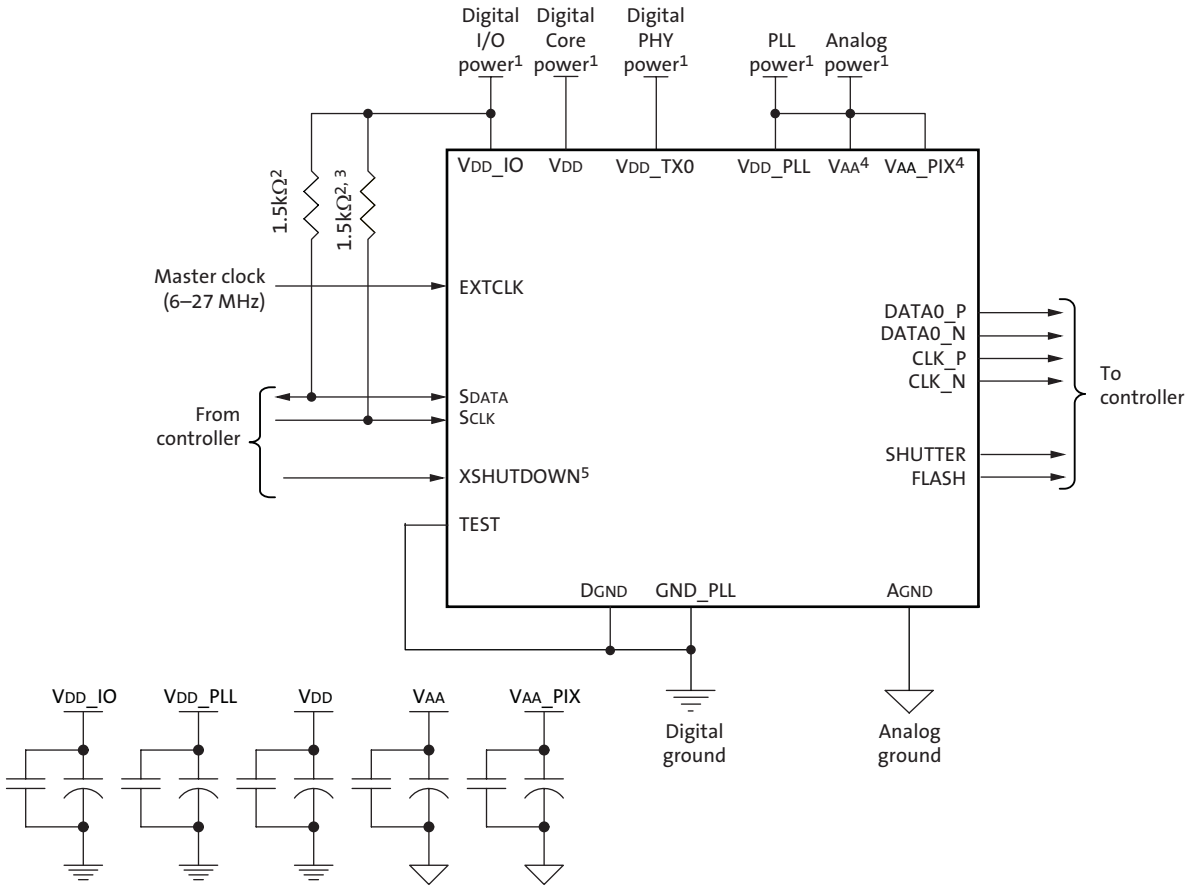
Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Aptina recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connections

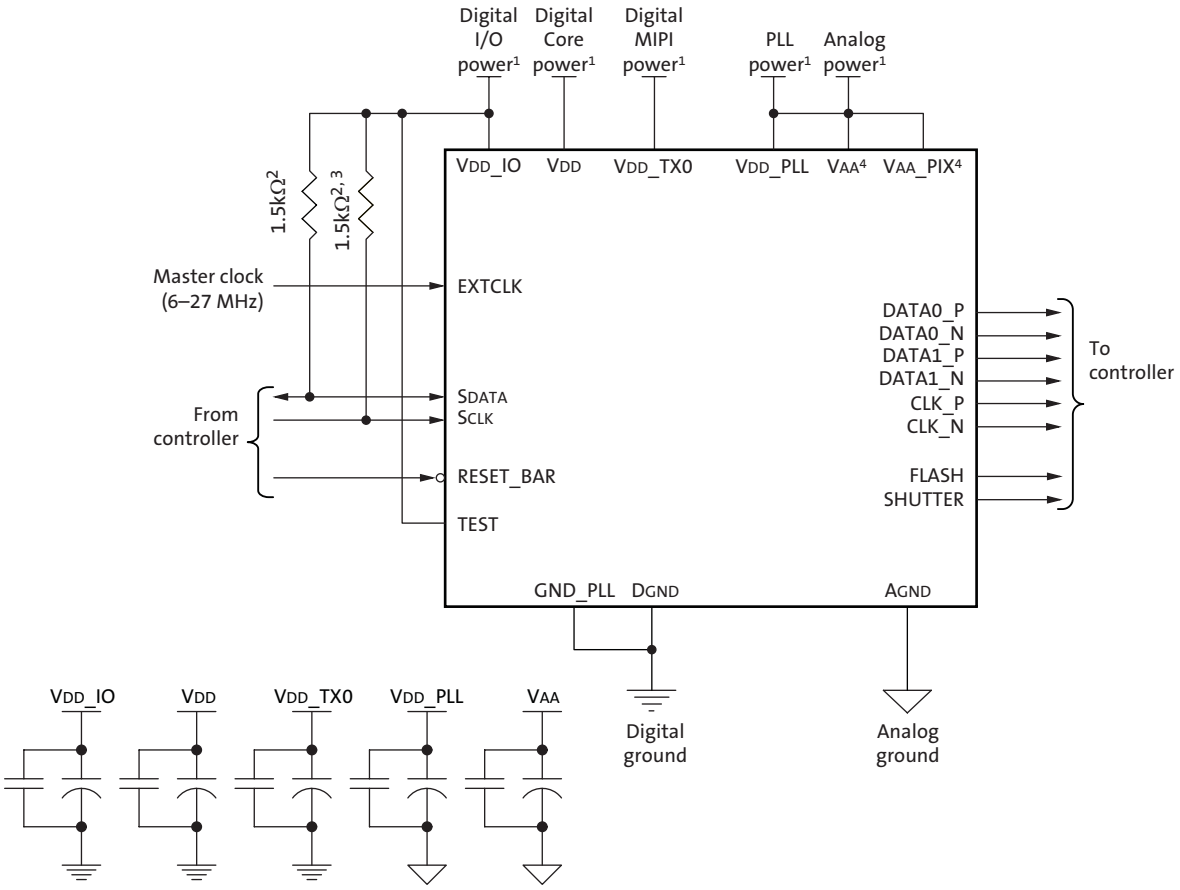
Figure 1 below and Figure 2 on page 6 show typical connection schematics for the MT9P014 die.

Figure 1: Typical Connection: Serial CCP2 Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. Also referred to as RESET_BAR.
6. VPP, which can be used during the module manufacturing process, is not shown in Figure 1. This pad is left unconnected during normal operation.
7. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply be mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
8. TEST must be tied to DGND.
9. Aptina recommends that GND_PLL be tied to DGND.
10. Aptina recommends that VDD_TX0 be tied to VDD.

Figure 2: Typical Connection: Serial Dual-Lane MIPI Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 2. This pad is left unconnected during normal operation.
6. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply be mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
7. TEST must be tied to VDD_IO.
8. Aptina recommends that GND_PLL be tied to DGND.
9. Aptina recommends that VDD_TX0 be tied to VDD.

Bond Pad Location and Identification Tables

Table 1: Bond Pad Location and Identification from Center of Pad 1
To ensure proper device operation, all power supply bond pads must be bonded

Pad	MT9P014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD2	0.00	0.00	0.0000000	0.0000000
2	DGND2	170.52	0.00	0.0067134	0.0000000
3	VDD_IO2	341.04	0.00	0.0134268	0.0000000
4	FLASH	511.56	0.00	0.0201402	0.0000000
5	SHUTTER	718.04	0.00	0.0282693	0.0000000
6	VDD_IO3	888.56	0.00	0.0349827	0.0000000
7	DGND3	1059.08	0.00	0.0416961	0.0000000
8	GPI0	1229.60	0.00	0.0484094	0.0000000
9	GPI1	1400.12	0.00	0.0551228	0.0000000
10	GPI2	1570.64	0.00	0.0618362	0.0000000
11	GPI3	1741.16	0.00	0.0685496	0.0000000
12	SCLK	1911.68	0.00	0.0752630	0.0000000
13	SDATA	2082.20	0.00	0.0819764	0.0000000
14	VDD3	2252.72	0.00	0.0886898	0.0000000
15	TEST	2423.24	0.00	0.0954031	0.0000000
16	DGND4	2593.76	0.00	0.1021165	0.0000000
17	VDD_IO4	2906.96	0.00	0.1144472	0.0000000
18	EXTCLK	3077.59	0.00	0.1211648	0.0000000
19	RESET_BAR (XSHUTDOWN)	3248.58	0.00	0.1278969	0.0000000
20	GND_PLL	3419.11	0.00	0.1346106	0.0000000
21	VDD_PLL	4974.66	0.00	0.1958528	0.0000000
22	CLK_P	5202.76	0.00	0.2048331	0.0000000
23	CLK_N	5432.76	0.00	0.2138882	0.0000000
24	DATA0_P	5662.77	0.00	0.2229435	0.0000000
25	DATA0_N	5892.77	0.00	0.2319986	0.0000000
26	DATA1_P	6122.77	0.00	0.2410539	0.0000000
27	DATA1_N	6352.77	0.00	0.2501091	0.0000000
28	VDD_TX0	6614.32	0.00	0.2604063	0.0000000
29	VDD4	6784.84	0.00	0.2671197	0.0000000
30	DGND5	6955.36	0.00	0.2738331	0.0000000
31	VDD_IO5	7125.88	0.00	0.2805465	0.0000000
32	DNU[2]	7407.18	–315.52	0.2916213	–0.0124220
33	VAA4	7407.18	–1043.42	0.2916213	–0.0410795
34	AGND7	7407.18	–1213.94	0.2916213	–0.0477929
35	VAA3	7407.18	–2536.34	0.2916213	–0.0998559
36	AGND6	7407.18	–2706.86	0.2916213	–0.1065693
37	VAA_PIX3	7407.18	–2877.38	0.2916213	–0.1132827
38	VAA_PIX2	7407.18	–3047.90	0.2916213	–0.1199961
39	VAA_PIX1	7407.18	–3218.42	0.2916213	–0.1267094
40	DNU	7407.18	–3349.50	0.2916213	–0.1318701
41	DNU	7407.18	–3459.70	0.2916213	–0.1362087

Table 1: Bond Pad Location and Identification from Center of Pad 1 (continued)
To ensure proper device operation, all power supply bond pads must be bonded

Pad	MT9P014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
42	DNU	7407.18	–3569.90	0.2916213	–0.1405472
43	VPP	7407.18	–3728.24	0.2916213	–0.1467811
44	AGND5	7407.18	–3902.24	0.2916213	–0.1536315
45	AGND4	7407.18	–4072.76	0.2916213	–0.1603449
46	AGND3	7407.18	–4243.28	0.2916213	–0.1670583
47	AGND2	7407.18	–4413.80	0.2916213	–0.1737717
48	VAA2	7407.18	–4584.32	0.2916213	–0.1804850
49	AGND1	7407.18	–5891.64	0.2916213	–0.2319543
50	VAA1	7407.18	–6062.16	0.2916213	–0.2386677
51	VDD1	–61.48	–6077.24	–0.0024205	–0.2392614
52	DGND1	–61.48	–5906.72	–0.0024205	–0.2325480
53	VDD_IO1	–61.48	–5736.20	–0.0024205	–0.2258346

Notes: 1. Reference to center of each bond pad from center of pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.

Table 2: Bond Pad Location and Identification from Center of Die (0,0)
To ensure proper device operation, all power supply bond pads must be bonded

Pad	MT9P014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD2	–3672.85	3316.44	–0.1446004	0.1305685
2	DGND2	–3502.33	3316.44	–0.1378870	0.1305685
3	VDD_IO2	–3331.81	3316.44	–0.1311736	0.1305685
4	FLASH	–3161.29	3316.44	–0.1244602	0.1305685
5	SHUTTER	–2954.81	3316.44	–0.1163311	0.1305685
6	VDD_IO3	–2784.29	3316.44	–0.1096177	0.1305685
7	DGND3	–2613.77	3316.44	–0.1029043	0.1305685
8	GPI0	–2443.25	3316.44	–0.0961909	0.1305685
9	GPI1	–2272.73	3316.44	–0.0894776	0.1305685
10	GPI2	–2102.21	3316.44	–0.0827642	0.1305685
11	GPI3	–1931.69	3316.44	–0.0760508	0.1305685
12	SCLK	–1761.17	3316.44	–0.0693374	0.1305685
13	SDATA	–1590.65	3316.44	–0.0626240	0.1305685
14	VDD3	–1420.13	3316.44	–0.0559106	0.1305685
15	TEST	–1249.61	3316.44	–0.0491972	0.1305685
16	DGND4	–1079.09	3316.44	–0.0424839	0.1305685
17	VDD_IO4	–765.89	3316.44	–0.0301531	0.1305685
18	EXTCLK	–595.27	3316.44	–0.0234356	0.1305685
19	RESET_BAR (XSHUTDOWN)	–424.27	3316.44	–0.0167035	0.1305685
20	GND_PLL	–253.74	3316.44	–0.0099898	0.1305685
21	VDD_PLL	1301.81	3316.44	0.0512524	0.1305685
22	CLK_P	1529.91	3316.44	0.0602327	0.1305685
23	CLK_N	1759.91	3316.44	0.0692878	0.1305685
24	DATA0_P	1989.92	3316.44	0.0783431	0.1305685
25	DATA0_N	2219.92	3316.44	0.0873982	0.1305685
26	DATA1_P	2449.92	3316.44	0.0964535	0.1305685
27	DATA1_N	2679.92	3316.44	0.1055087	0.1305685
28	VDD_TX0	2941.47	3316.44	0.1158059	0.1305685
29	VDD4	3111.99	3316.44	0.1225193	0.1305685
30	DGND5	3282.51	3316.44	0.1292327	0.1305685
31	VDD_IO5	3453.03	3316.44	0.1359461	0.1305685
32	DNU[2]	3734.33	3000.92	0.1470209	0.1181465
33	VAA4	3734.33	2273.02	0.1470209	0.0894890
34	AGND7	3734.33	2102.50	0.1470209	0.0827756
35	VAA3	3734.33	780.10	0.1470209	0.0307126
36	AGND6	3734.33	609.58	0.1470209	0.0239992
37	VAA_PIX3	3734.33	439.06	0.1470209	0.0172858
38	VAA_PIX2	3734.33	268.54	0.1470209	0.0105724
39	VAA_PIX1	3734.33	98.02	0.1470209	0.0038591
40	DNU	3734.33	–33.06	0.1470209	–0.0013016
41	DNU	3734.33	–143.26	0.1470209	–0.0056402
42	DNU	3734.33	–253.46	0.1470209	–0.0099787
43	VPP	3734.33	–411.80	0.1470209	–0.0162126
44	AGND5	3734.33	–585.80	0.1470209	–0.0230630

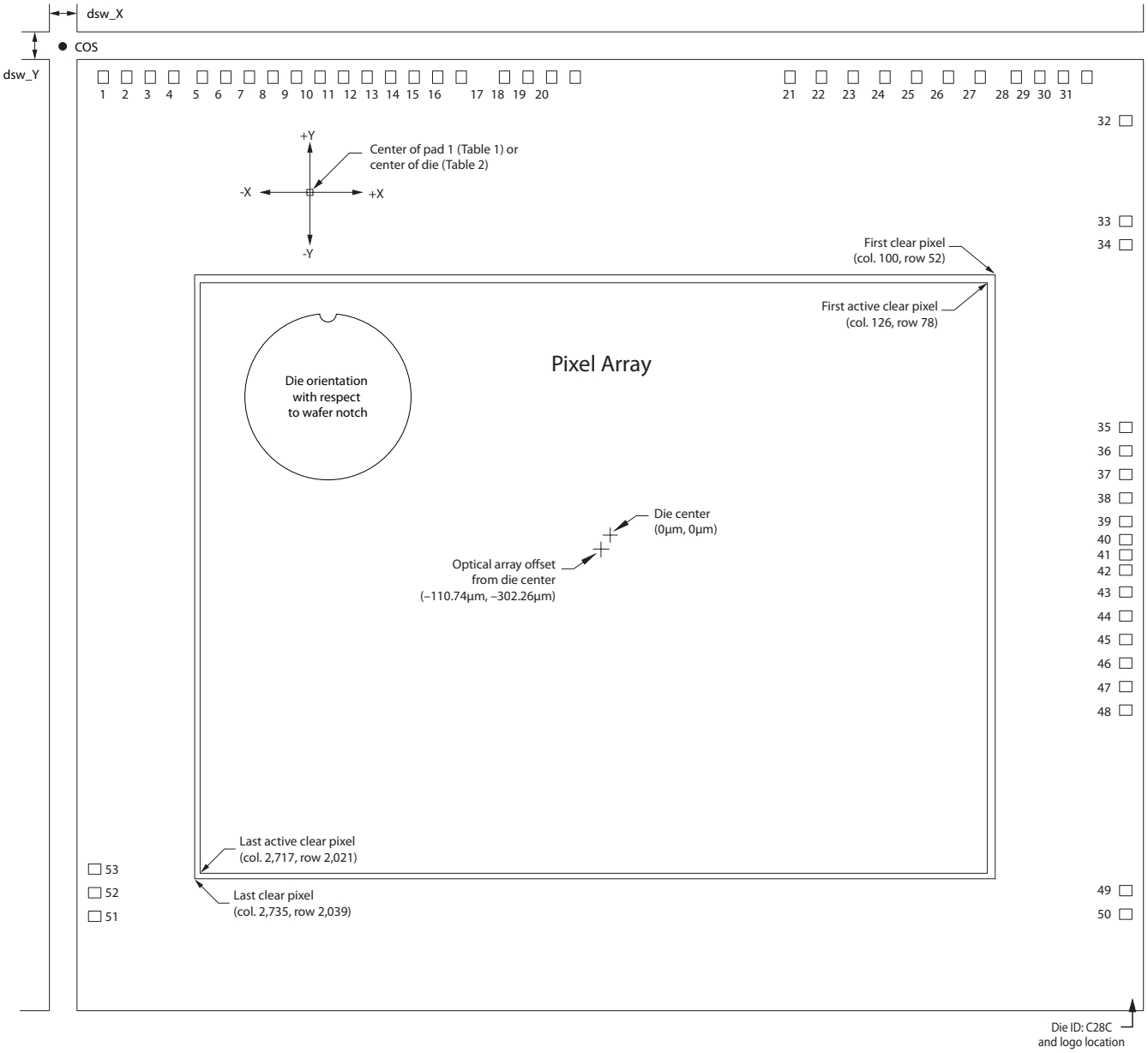
Table 2: Bond Pad Location and Identification from Center of Die (0,0) (continued)
To ensure proper device operation, all power supply bond pads must be bonded

Pad	MT9P014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
45	AGND4	3734.33	–756.32	0.1470209	–0.0297764
46	AGND3	3734.33	–926.84	0.1470209	–0.0364898
47	AGND2	3734.33	–1097.36	0.1470209	–0.0432031
48	VAA2	3734.33	–1267.88	0.1470209	–0.0499165
49	AGND1	3734.33	–2575.20	0.1470209	–0.1013858
50	VAA1	3734.33	–2745.72	0.1470209	–0.1080992
51	VDD1	–3734.33	–2760.80	–0.1470209	–0.1086929
52	DGND1	–3734.33	–2590.28	–0.1470209	–0.1019795
53	VDD_IO1	–3734.33	–2419.76	–0.1470209	–0.0952661

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 3.

Die Features

Figure 3: Die Outline (Top View)



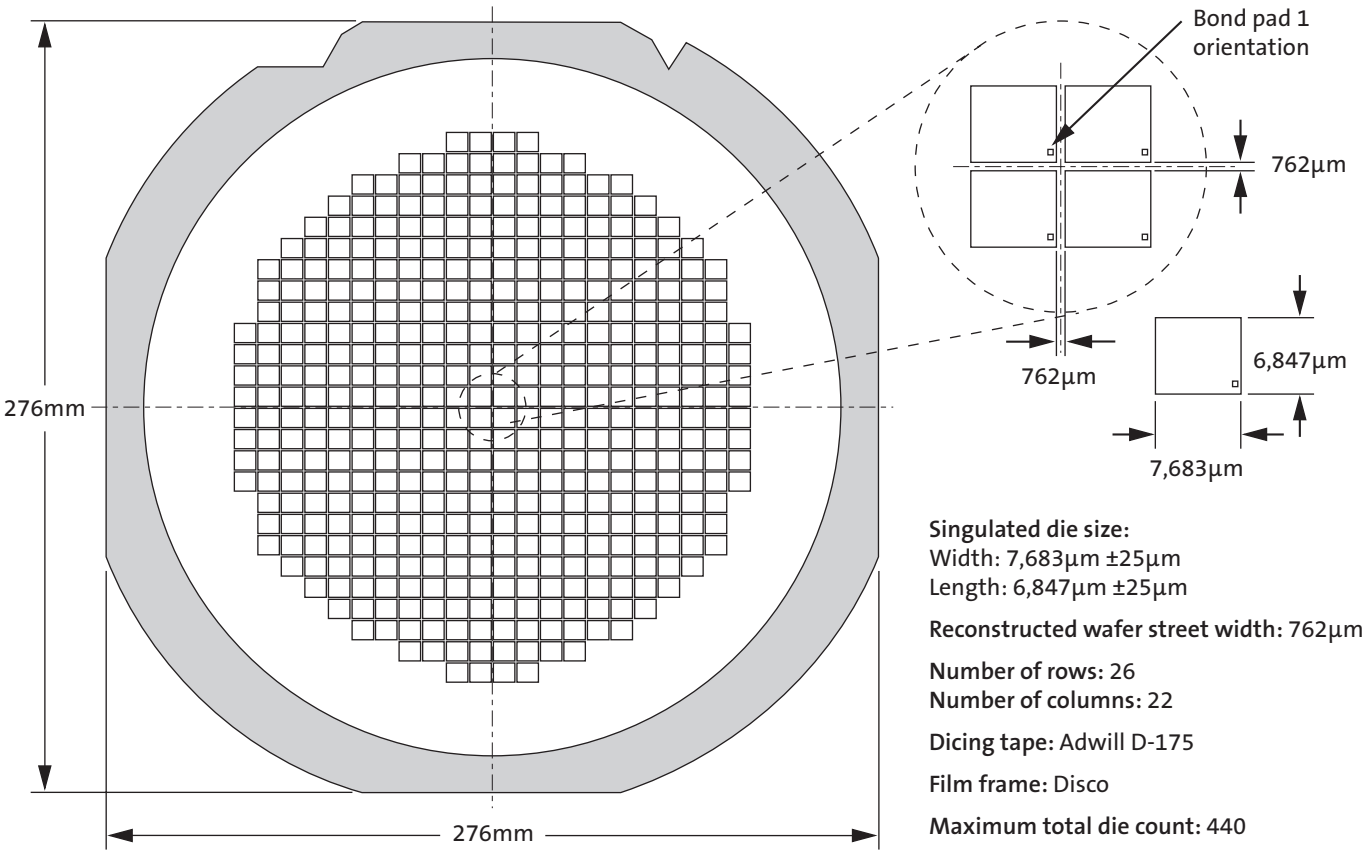
Note: Die street widths are not drawn to scale.

Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) Width (X dimension): Length (Y dimension):	 7,683 ±25µm 6,847 ±25µm
Bond pad size (MIN)	85µm x 100µm
Passivation openings (MIN)	75µm x 90µm
Minimum bond pad pitch between any two bondable pads	170.52µm
Optical array offset Optical center from die center: Optical center from center of pad 1:	 X = –110.74µm, Y = –302.26µm X = 3,562.11µm, Y = –3,618.70µm
First clear pixel (col. 100, row 52) From die center: From center of pad 1:	 X = 2,788.86µm, Y = 1,884.54µm X = 6,463.71µm, Y = –1,431.90µm
First clear active pixel (col. 126, row 78) From die center: From center of pad 1:	 X = 2,731.66µm, Y = 1,827.34µm X = 6,406.51µm, Y = –1,489.10µm
Last clear active pixel (col. 2,717, row 2,021) From die center: From center of pad 1:	 X = –2,970.74µm, Y = –2,449.46µm X = 704.11µm, Y = –5,765.90µm
Last clear pixel (col. 2,735, row 2,039) From die center: From center of pad 1:	 X = –3,010.34µm, Y = –2,489.06µm X = 664.51µm, Y = –5,805.50µm

Figure 4: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 7,683µm ±25µm
Length: 6,847µm ±25µm

Reconstructed wafer street width: 762µm

Number of rows: 26
Number of columns: 22

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 440

Revision History

Rev. D 5/15/12

- Updated trademarks
- Applied updated Aptina template

Rev. C 7/21/10

- Updated to Aptina template

Rev. B 4/6/09

- Updated to Production
- Updated to new Aptina template
- Updated power consumption to 332mW and standby current to 69.8µW in "Key Performance Parameters (continued)" on page 2

Rev. A 06/08

- Initial release, Advance.

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