1/6-Inch SOC VGA CMOS Digital Image Sensor Die

MT9V112

For production data sheet, refer to Micron's Web site: www.micron.com

Features

- Micron® DigitalClarity® CMOS imaging technology
- System-on-chip (SOC)—Completely integrated camera system
- Ultra low-power, low-cost, progressive scan CMOS image sensor
- Superior low-light performance
- On-die image flow processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens-shading correction, and on-the-fly defect correction
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Automatic features: auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Fully automatic xenon and LED-type flash support including fast exposure adaptation
- Multiple parameter contexts for easy/fast mode switching
- Camera control sequencer that automates snapshots, snapshots with flash, and video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats

General Physical Specifications

- Wafer thickness:
  750µm ±25µm (available in wafer form only)
  200µm ±12µm (available in die and wafer form)
  (Consult factory for other die thickness)
- Backside wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

Wafer: MT9V112W00STCK12AC1

Die: MT9V112D00STCK12AC1

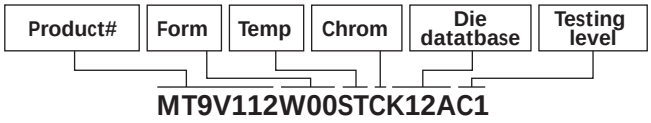
Die Database K12A

- Die outline, see Figure 2 on page 7
- Die size (stepping interval):
  4,946.80µm x 4,946.80µm
- Bond Pad Location and Identification Tables, see pages 5–6

Option

- Form
  - Die — D
  - Wafer – 200mm (8in) — W
- Testing
  - Standard (level 1) probe — C1

1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.



Key Performance Parameters

- Optical format: 1/6-inch (4:3)
- Active imager size: 2.30mm(H) x 1.73mm(V), 2.88mm diagonal
- Active pixels: 640H x 480V
- Pixel size: 3.6µm x 3.6µm
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Maximum data rate/master clock:
  12–13.5 MPS/24–27 MHz
- Frame rate: VGA (640H x 480V) 30 fps at 27 MHz
- ADC resolution: 10 bit, on-die
- Responsivity: 1.0 V/lux-sec (550nm)
- Dynamic range: 71dB
- SNR MAX: 44dB
- Supply voltage
  - I/O digital 1.7–3.1V
  - Core digital 1.7–1.9V or 2.5–3.1V (1.8V or 2.8V nominal)
  - Analog 2.5–3.1V (2.8V nominal)
- Power consumption:
  76mW at 1.8V and 15 frames per second (fps)
- Operating temperature: –30°C to +70°C

General Description

The Micron Imaging MT9V112 die is an VGA-format single-die camera CMOS active-pixel digital image sensor. This device combines the MT9V012 image sensor core with fourth-generation digital-image-flow processor technology from Micron Imaging. It captures high-quality color images at VGA resolution.

This VGA CMOS image sensor features DigitalClarity —a Micron breakthrough—low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete camera-on-a-die solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-die and is programmable through a simple two-wire serial interface.

The MT9V112 die performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure (AE), automatic 50Hz/60Hz flicker avoidance, lens-shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both xenon and LED-type flash light sources in several snapshot modes.

The MT9V112 die can be programmed to output progressive-scan images up to 30 fps. The image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated bond pads, along with a pixel clock that is synchronous with valid data.

Die Testing Procedures

Micron Imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die analog-to-digital converter (ADC), logic, serial interface bus, pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9V112 imager die has 39 bond pads. Refer to Tables 1 and 2 on pages 5–6 for a complete list of bond pads and coordinates.

The MT9V112 imager die does not require the user to determine bond option features.

The MT9V112 imager die also has two pads defined as "do not use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows the MT9V112 typical die connections. For low-noise operation the MT9V112 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

Bond pad 27 (TEST_ENABLE) must be grounded for proper device functionality.

The MT9V112 imager die also supports different digital core (V_{DD}/D_{GND}) and I/O power ($V_{DD}Q$/$D_{GND}Q$) power domains that can be at different voltages.

Wafer Saw

The die size (stepping interval) provided is measured from the center of the die street on one side of the die to the center of the die street on the other side of the die. A singulated die is approximately 42µm smaller in length and width. The dimensional tolerance of a singulated die is ±25µm. For example, if the die width (stepping interval) is 5,080µm and the die length (stepping interval) is 7,620µm, the dimensions of the singulated die will be 5,038µm ±25µm by 7,578µm ±25µm.

Wafer-Level Processing

Customers should choose the wafer form when post-processing of die is required. This includes adding extra passivation or metal layers or bumping of the bond pads. For these customers, the street widths are provided in the die outline. Also, a reference from the center of bond pad 1 to the center of the intersection of two streets is provided for easy alignment.

Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Micron recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

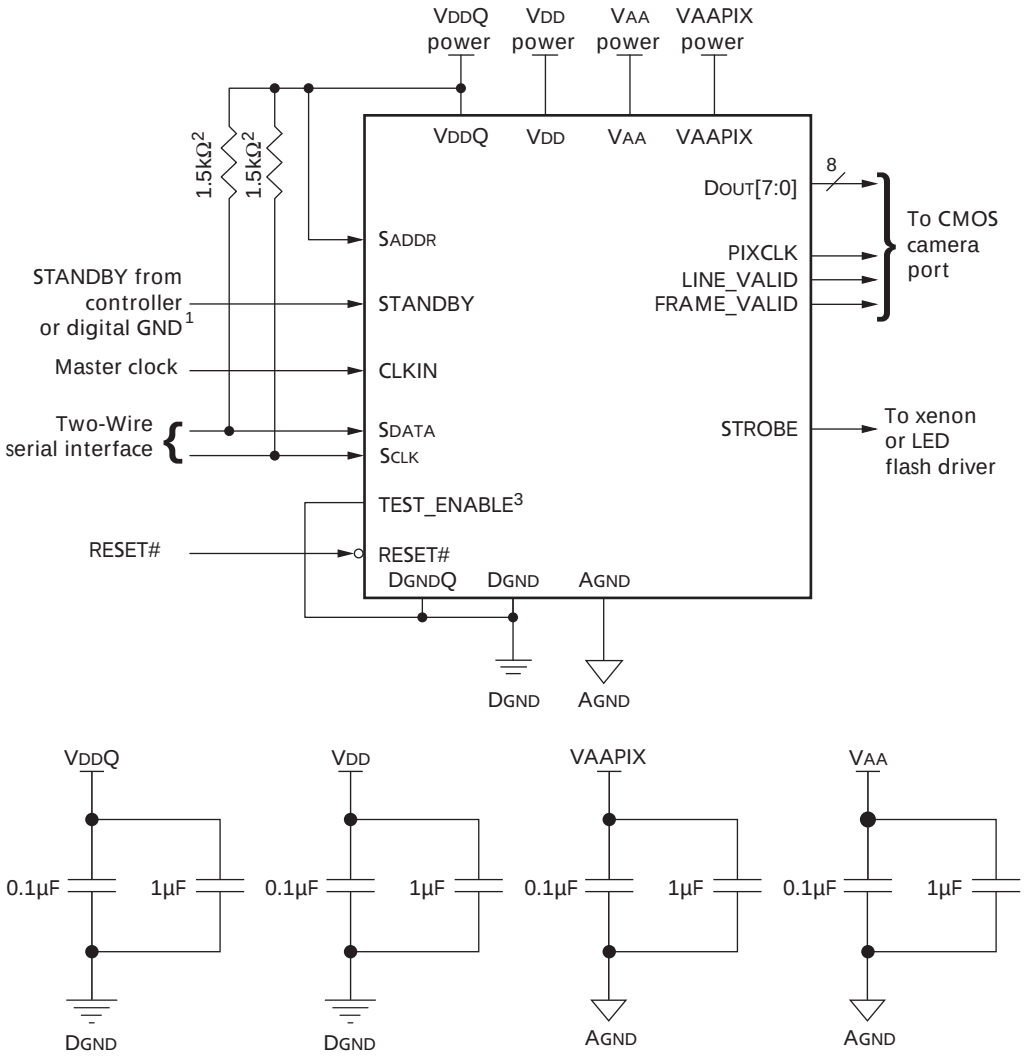
Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and

"Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Typical Connection

Figure 1: Typical Configuration (Connection)



Notes:
1. MT9V112 STANDBY can be connected to customer's ASIC controller directly or to DGND, depending on the controller's capability.
2. A 1.5kΩ resistor value is recommended, but may be greater for slower two-wire speed.
3. TEST_ENABLE must be connected to DGND for proper device functionality.

Bond Pad Location and Identification Tables

Table 1: MT9V112 Bond Pad Location and Identification from Center of Pad 1

Pad	MT9V112	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND1	0.00	0.00	0.0000000	0.0000000
2	VDD1	141.84	0.00	0.0055843	0.0000000
3	DOUT0	334.64	0.00	0.0131748	0.0000000
4	DOUT1	567.92	0.00	0.0223591	0.0000000
5	DOUT2	801.20	0.00	0.0315433	0.0000000
6	DOUT3	1034.48	0.00	0.0407276	0.0000000
7	DOUT4	1267.76	0.00	0.0499118	0.0000000
8	DOUT5	1501.04	0.00	0.0590961	0.0000000
9	DGNDQ0	1672.56	0.00	0.0658488	0.0000000
10	VDDQ0	1814.40	0.00	0.0714331	0.0000000
11	DOUT6	2007.20	0.00	0.0790236	0.0000000
12	DOUT7	2240.48	0.00	0.0882079	0.0000000
13	FRAME_VALID	2473.76	0.00	0.0973921	0.0000000
14	LINE_VALID	2707.04	0.00	0.1065764	0.0000000
15	CLKIN	2900.94	0.00	0.1142100	0.0000000
16	DGND0	3048.48	0.00	0.1200189	0.0000000
17	VDD0	3190.32	0.00	0.1256031	0.0000000
18	DNU[2]	3988.72	0.00	0.1570360	0.0000000
19	DNU	4130.56	0.00	0.1626203	0.0000000
20	DGND3	4414.96	–4596.21	0.1738173	–0.1809531
21	VDD3	4273.12	–4596.21	0.1682331	–0.1809531
22	VAAPIX	3578.00	–4596.21	0.1408661	–0.1809531
23	AGND	3446.96	–4596.21	0.1357071	–0.1809531
24	VAA1	3305.12	–4596.21	0.1301228	–0.1809531
25	VAA0	3163.28	–4596.21	0.1245386	–0.1809531
26	SDATA	2358.16	–4596.21	0.0928409	–0.1809531
27	TEST_ENABLE[3]	2164.27	–4596.21	0.0852073	–0.1809531
28	STANDBY	1994.35	–4596.21	0.0785175	–0.1809531
29	RESET#	1824.43	–4596.21	0.0718278	–0.1809531
30	SCLK	1654.51	–4596.21	0.0651380	–0.1809531
31	DGNDQ1	1506.96	–4596.21	0.0593291	–0.1809531
32	VDDQ1	1365.12	–4596.21	0.0537449	–0.1809531
33	STROBE	1172.32	–4596.21	0.0461543	–0.1809531
34	PIXCLK	939.04	–4596.21	0.0369701	–0.1809531
35	DOUTLSB1[4]	705.76	–4596.21	0.0277858	–0.1809531
36	DOUTLSB0[4]	472.48	–4596.21	0.0186016	–0.1809531
37	SADDR	278.59	–4596.21	0.0109679	–0.1809531
38	DGND2	131.04	–4596.21	0.0051591	–0.1809531
39	VDD2	–10.80	–4596.21	–0.0004252	–0.1809531

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. TEST_ENABLE must be connected to DGND for proper device functionality.
4. Typically not used for normal SOC operation.

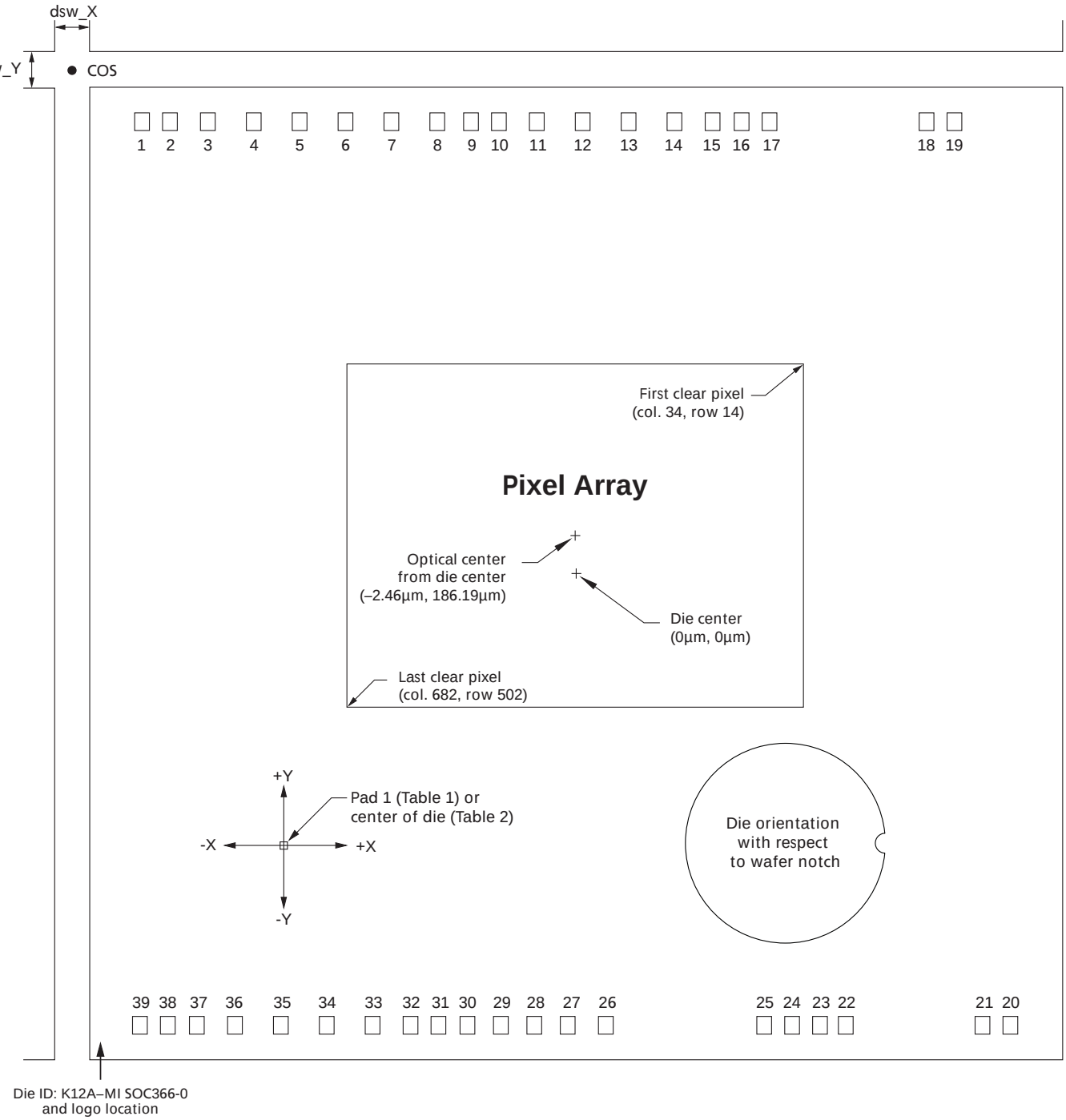
Table 2: MT9V112 Bond Pad Location and Identification from Center of Die (0, 0)

Pad	MT9V112	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND1	–2207.48	2298.11	–0.0869087	0.0904766
2	VDD1	–2065.64	2298.11	–0.0813244	0.0904766
3	DOUT0	–1872.84	2298.11	–0.0737339	0.0904766
4	DOUT1	–1639.56	2298.11	–0.0645496	0.0904766
5	DOUT2	–1406.28	2298.11	–0.0553654	0.0904766
6	DOUT3	–1173.00	2298.11	–0.0461811	0.0904766
7	DOUT4	–939.72	2298.11	–0.0369969	0.0904766
8	DOUT5	–706.44	2298.11	–0.0278126	0.0904766
9	DGNDQ0	–534.92	2298.11	–0.0210598	0.0904766
10	VDDQ0	–393.08	2298.11	–0.0154756	0.0904766
11	DOUT6	–200.28	2298.11	–0.0078850	0.0904766
12	DOUT7	33.00	2298.11	0.0012992	0.0904766
13	FRAME_VALID	266.28	2298.11	0.0104835	0.0904766
14	LINE_VALID	499.56	2298.11	0.0196677	0.0904766
15	CLKIN	693.46	2298.11	0.0273014	0.0904766
16	DGND0	841.00	2298.11	0.0331102	0.0904766
17	VDD0	982.84	2298.11	0.0386945	0.0904766
18	DNU[2]	1781.24	2298.11	0.0701274	0.0904766
19	DNU	1923.08	2298.11	0.0757116	0.0904766
20	DGND3	2207.48	–2298.11	0.0869087	–0.0904766
21	VDD3	2065.64	–2298.11	0.0813244	–0.0904766
22	VAAPIX	1370.52	–2298.11	0.0539575	–0.0904766
23	AGND	1239.48	–2298.11	0.0487984	–0.0904766
24	VAA1	1097.64	–2298.11	0.0432142	–0.0904766
25	VAA0	955.80	–2298.11	0.0376299	–0.0904766
26	SDATA	150.68	–2298.11	0.0059323	–0.0904766
27	TEST_ENABLE[3]	–43.22	–2298.11	–0.0017014	–0.0904766
28	STANDBY	–213.14	–2298.11	–0.0083911	–0.0904766
29	RESET#	–383.06	–2298.11	–0.0150809	–0.0904766
30	SCLK	–552.98	–2298.11	–0.0217707	–0.0904766
31	DGNDQ1	–700.52	–2298.11	–0.0275795	–0.0904766
32	VDDQ1	–842.36	–2298.11	–0.0331638	–0.0904766
33	STROBE	–1035.16	–2298.11	–0.0407543	–0.0904766
34	PIXCLK	–1268.44	–2298.11	–0.0499386	–0.0904766
35	DOUTLSB1[4]	–1501.72	–2298.11	–0.0591228	–0.0904766
36	DOUTLSB0[4]	–1735.00	–2298.11	–0.0683071	–0.0904766
37	SADDR	–1928.90	–2298.11	–0.0759407	–0.0904766
38	DGND2	–2076.44	–2298.11	–0.0817496	–0.0904766
39	VDD2	–2218.28	–2298.11	–0.0873339	–0.0904766

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. TEST_ENABLE must be connected to DGND for proper device functionality.
4. Typically not used for normal SOC operation.

Die Features

Figure 2: Die Outline (Top View)



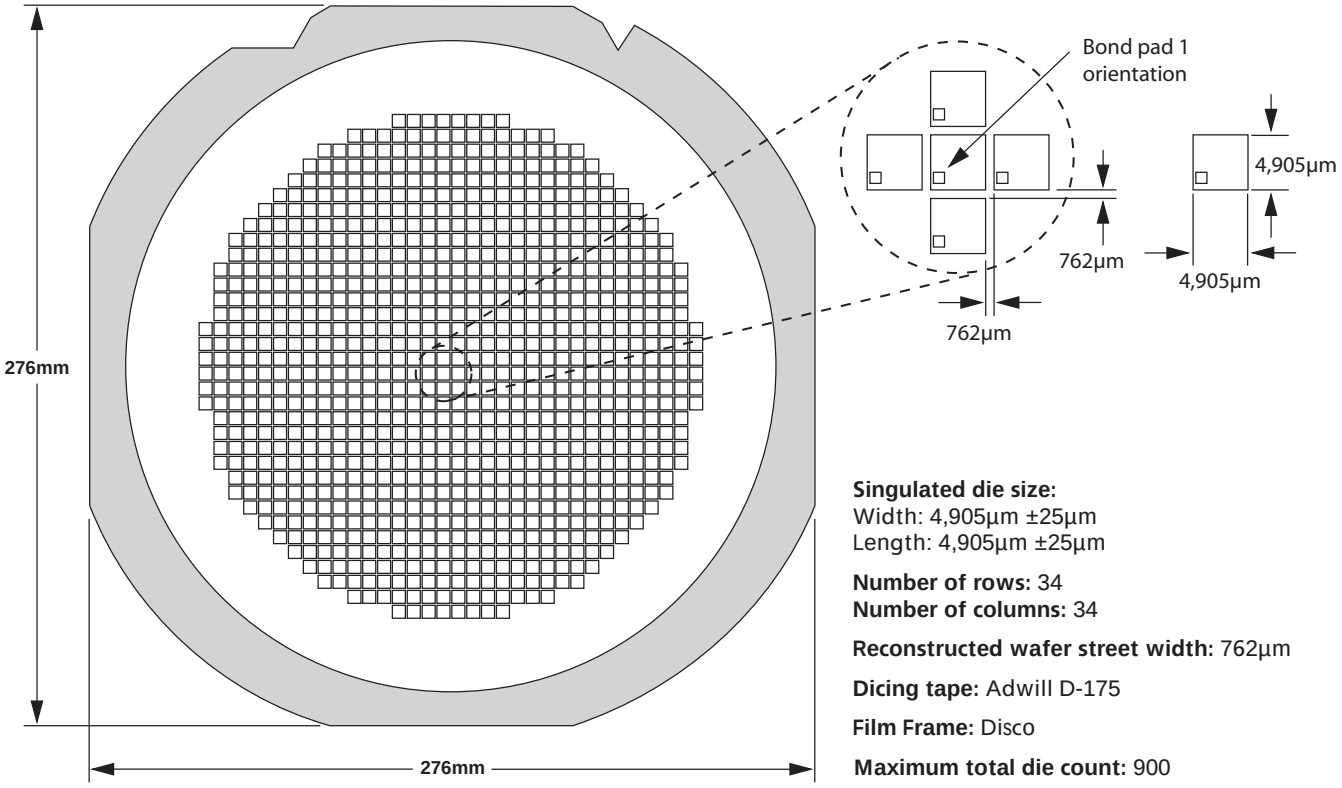
Notes: 1. Die street widths are not drawn to scale. Die outline shows streets and bond pads passivation openings.

Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Wafer thickness	675µm ±12µm (available in wafer form only) 200µm ±12µm (available in die and wafer form)
Singulated die size *Width:* *Length:*	 4,905µm ±25µm 4,905µm ±25µm
Die size (stepping interval)	4,946.80µm x 4,946.80µm (194.760 mil x 194.760 mil)
Street width along X-axis (dsw_X)	127.0µm (5.00 mil)
Street width along Y-axis (dsw_Y)	127.0µm (5.00 mil)
Center of streets (COS) (relative to center of bond pad 1)	X = –265.92µm, Y = 175.30µm (X = –10.469 mil, Y = 6.901 mil)
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	131.04µm (5.159 mil)
Optical array Optical center from die center:	 X = –2.46µm, Y = 186.19µm
First clear pixel (col. 34, row 14) *From die center:* *From center of pad 1:*	 X = 1,162.15µm, Y = 1,062.95µm X = 3,369.63µm, Y = –1,235.17µm
Last clear pixel (col. 682, row 502) *From die center:* *From center of pad 1:*	 X = –1,170.77µm, Y = –693.83µm X = 1,036.72µm, Y = –2,991.94µm

Figure 3: MT9V112 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 4,905µm ±25µm
Length: 4,905µm ±25µm

Number of rows: 34
Number of columns: 34

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film Frame: Disco

Maximum total die count: 900

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Revision History

Rev. D, Production **5/07**

- Updated Figure 3 on page 9
- Added DigitalClarity trademark
- Updated “Functional Specifications” text

Rev. C, Production **7/06**

- Added TEST_ENABLE paragraph to “Bonding Instructions” on page 3
- Updated Figure 1 and added TEST_ENABLE note
- Added TEST_ENABLE note to Table 1 and Table 2

Rev. B, Production **3/05**

- Removed preliminary designation
- Updated template
- Updated “Wafer Saw” text
- Added singulated die size
- Changed supply voltage: I/O digital from 1.7–3.6V to 1.7–3.1V

Rev. A, Preliminary **11/04**

- Changed power consumption from 78mW at 2.8V and 30 frames per second (fps) to 76mW at 1.8V and 15
- frames per second (fps) on page 1

Rev. A, Preliminary **11/04**

- Initial release