1-Inch 10Mp CMOS Digital Image Sensor

AR1011HS Data Sheet, Rev. C

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- 3.4µm pixel size with Aptina DR-Pix™ technology
- 1/80 sec frame readout time, 1-inch optical size, 10Mpixel imager
- 60 fps continuous readout in 10Mp full resolution mode
- Multiple operation modes including: HD60_3:2 at 60fps, HD120_16:9 at 120fps, Hi-Speed at 400fps, and Super Hi-Speed at 1200fps
- Low noise, low power consumption high speed differential serial video output (HiSPI™)
- External master clock frequency 48 MHz

Applications

- Digital still camera

Description

The AR1011HS is an image sensor with 1-inch optical format, 10M pixel resolution, and 1/80 sec. frame readout speed in still mode for digital camera applications.

The operation modes of the AR1011HS are highly specified. Although many combinations of operation settings are possible by various register settings, only the image sensor operational modes specified in this document are guaranteed.

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
AR1011HSSC00SHAA0	124 CLCC, 0 deg. CRA

Key Specifications

Table 2: Key Performance Parameters

Parameter		Value
Optical format		16.3mm diagonal (3:2)
		13.5mm x 9.2mm
Pixel size		3.4mm x 3.4mm with DR-PixTM
Entire arry format		3984 (H) x 2712 (V)
Primary modes		Full resolution: 3984 x 2712 at 1/80
		HD60_3:2: 3984 x 2712 at 60fps
		HD120_16:9: 3984 x 1800 at 120fps
		Hi-Speed: 3984 x 520 at 400fps
		Super Hi-Speed: 3984 x 146 at 1200fps
Chief ray angle		0 degree
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Master clock		48MHz
Control interface		2-wire serial (Max 400kHz)
Outputs		Data: 24 lanes (576Mbps/lane)
		Clock: 6 lanes (288MHz DDR)
ADC resolution		13-bit, on-chip ADC (12bit output)
Analog gain		1x, 2x, 4x, and 8x
Responsivity		27ke-/lux*sec
Dynamic range		84dB
SNR_{MAX}		41dB
Supply voltage	V_{DD}	1.7-1.9V, typ. 1.8V
	V_{AA}	2.8-3.2V, typ. 3.0V
	V_{AA}1.8	1.7-1.9V, typ. 1.8V
	V_{AA_PIX}	2.8-3.2V, typ. 3.0V
	V_{DD_HiSPi}	0.35-0.45V, typ. 0.4V
	V_{DD_PLL}	2.7-2.9V, typ. 2.8V
Package		124pin CLCC
		27.4mm x 23mm x 2.4mm

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General Description

The AR1011HS is a CMOS image sensor with a full resolution high speed capable sensor in various readout operation modes for digital camera applications.

Functional Overview and Operation Modes

The AR1011HS is a 10Mpixel image sensor designed using Aptina's latest 3.4µm pixel technology. Aptina's Dual Conversion Gain (DCG) technology, which enables the pixel level selection of the high/low sensitivity control, is implemented in the sensor.

This document describes the subresolution schemes, which enable the special video modes, that is, 1080p/60 HDTV mode, HD_60_16:9_LP mode, Hd_60_16:9_FS mode, Pre-Flash B mode, EVF mode, Hi-Speed mode, Super Hi-Speed mode, and Pre-Flash A mode, as shown in Table 3. The operation timings are designed based on an external clock at 48.000 MHz.

Another feature of the AR1011HS is context mode change by a macro control register, which enables the very quick mode change from video mode to still image capture mode, minimizing shutter lag.

Table 3: Operating Modes

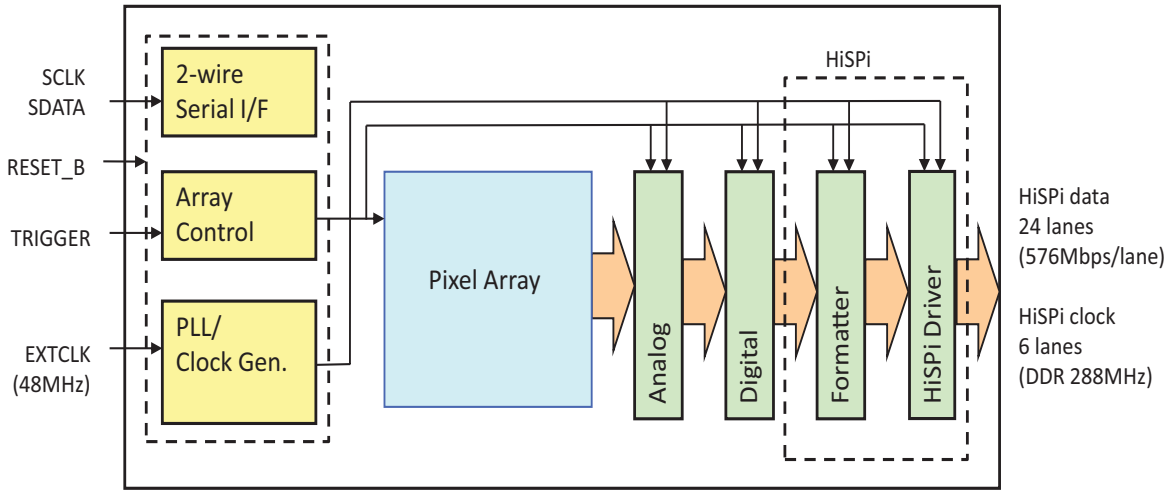
Operating Mode	Sub Res		Image Area Size		Frame Cycle (mclks)	Row Cycle (mclks)		Frame Cycle (rows)		Frame Rate	
	H	V	H	V		Total	Effect.	Total	Effect.	with VB	w/o VB
Full Resolution	Full	Full	3984	2712	800360	220	180	3638	2712	59.97	80.45
HDTV	Full	Bin(1/2)	3984	2240	800800	700	180	1144	1120	59.94	-
HD_60_3:2_SLV	Full	Full	3984	2712	800800	220	180	3640	2712	59.94	-
HD_60_16:9_FS	Full	Full	3984	2240	800800	308	180	2600	2240	59.94	-
HD_60_16:9_LP	Full	Full	3984	2240	800800	350	180	2288	2240	59.94	-
HD_120_16:9_SLV	Full	Full	3200	1800	400400	220	180	1820	1800	119.88	-
Hi-Speed	Full	Skip (2/5)	3984	1300	121000	220	180	550	520	396.69	-
Super Hi-Speed	Full	Skip (1/5)	3984	726	40040	220	180	182	146	1198.8	-
Pre-flash A	Bin (1/3)	Skip (1/15)	3984	2686	400400	440	60	910	180	119.88	606.06
Pre-flash B	Bin (1/3)	Skip (1/45)	3984	2656	400400	440	60	910	60	119.88	1818.18
EVF	Full	Skip (2/3)	3984	2682	800800	440	180	1820	1788	59.94	-

Block Diagram

The AR1011HS consists of the pixel array, analog signal processors, digital signal processors, output HiSPi™ formatters, HiSPi drivers, two-wire serial I/F controller, an array controller, and clock generator with PLL.

The image sensor is controlled by the serial I/F, which sends and receives SDATA according to SCLK timing. All the internal pulses are generated by the internal PLL from external clock EXTCLK. TRIGGER controls the sensor operation timing.

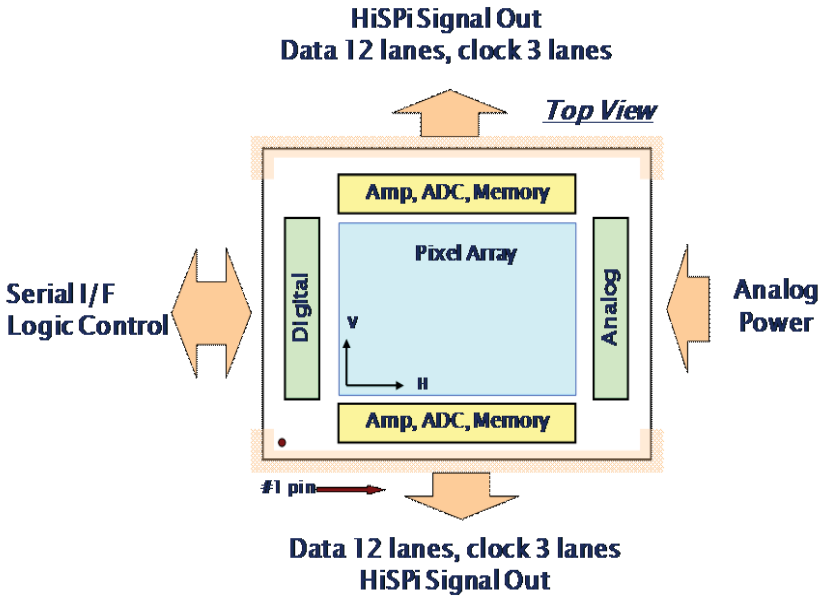
Figure 1: AR1011HS Block Diagram



Signal Descriptions

Floorplan

Figure 2: Package Pin Signal Grouping



Pin Assignment

Table 4 below and Figure 3 on page 13 show the pin names and the pin assignment in a package. Figure 4 on page 14 shows the pin connections.

Table 4: Package Pin List

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	DATA_1_N	43	VREF1_BOT	85	DATA_8_N
2	DATA_1_P	44	ATEST_BOT	86	DGND
3	DATA_3_N	45	VRS_HI	87	DATA_6_P
4	DATA_3_P	46	VRST_LO	88	DATA_6_N
5	D_CLK_1_N	47	VTX_LO2	89	DATA_4_P
6	D_CLK_1_P	48	VTX_LO1	90	DATA_4_N
7	DATA_5_N	49	AGND	91	D_CLK_0_P
8	DATA_5_P	50	VAA	92	D_CLK_0_N
9	DATA_7_N	51	VDCG_LO2	93	DATA_2_P
10	DATA_7_P	52	VDCG_LO1	94	DATA_2_N
11	DGND	53	VDCG_HI	95	DATA_0_P
12	DATA_9_N	54	ATEST_TOP	96	DATA_0_N
13	DATA_9_P	55	VREF1_TOP	97	VDD_SLVS
14	DATA_11_N	56	VBIAS_TOP	98	VDD
15	DATA_11_P	57	VAA_PIX	99	DGND
16	VDD_HiSPi	58	AGND	100	VAA
17	VDD	59	VAA	101	AGND
18	D_CLK_3_N	60	DGND	102	VAA_PIX
19	D_CLK_3_P	61	VDD	103	DGND
20	DATA_13_N	62	VDD_HiSPi	104	VDD
21	DATA_13_P	63	DATA_22_P	105	SCLK
22	DATA_15_N	64	DATA_22_N	106	SDATA
23	DATA_15_P	65	DATA_20_P	107	PHY_STABLE
24	DGND	66	DATA_20_N	108	TEST
25	DATA_17_N	67	D_CLK_4_P	109	TRIGGER
26	DATA_17_P	68	D_CLK_4_N	110	VDD_PLL
27	DATA_19_N	69	DATA_18_P	111	DGND
28	DATA_19_P	70	DATA_18_N	112	VDD
29	D_CLK_5_N	71	DATA_16_P	113	EXTCLK
30	D_CLK_5_P	72	DATA_16_N	114	RESET_B
31	DATA_21_N	73	DGND	115	OM1
32	DATA_21_P	74	DATA_14_P	116	OM2
33	DATA_23_N	75	DATA_14_N	117	VDD
34	DATA_23_P	76	DATA_12_P	118	DGND
35	VDD_HiSPi	77	DATA_12_N	119	VAA_PIX
36	VDD	78	D_CLK_2_P	120	AGND
37	DGND	79	D_CLK_2_N	121	VAA
38	AGND	80	VDD	122	DGND
39	VAA	81	VDD_HiSPi	123	VDD
40	AGND	82	DATA_10_P	124	VDD_HiSPi
41	VAA_PIX	83	DATA_10_N		
42	VBIAS_BOT	84	DATA_8_P		

Figure 3: Pin Assignment (Top View)

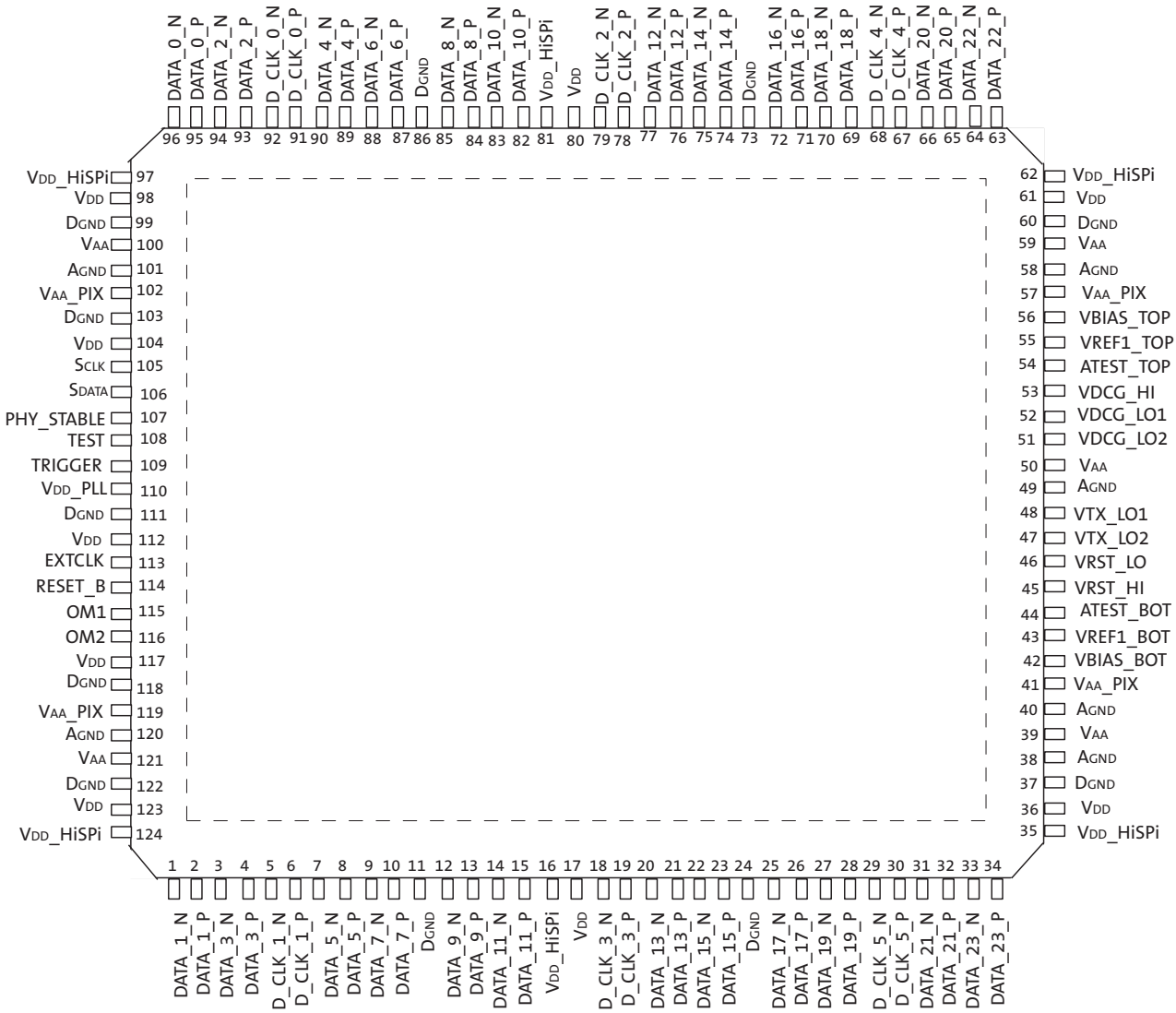


Figure 4: Typical Pin Connection

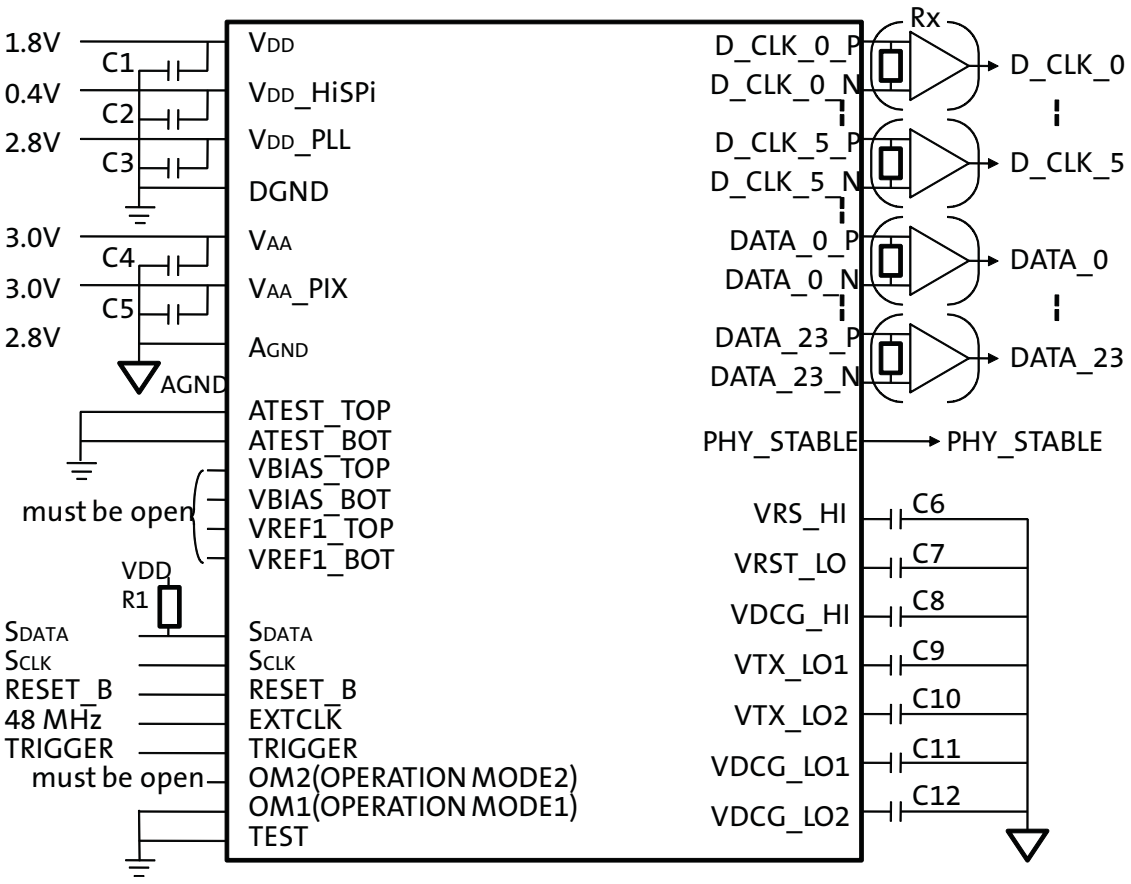


Table 5: Capacitance and Resistor Values

	Values		Values		Values
C1	0.1µF(ceramic) +10µF	C2	0.1µF(ceramic) +10µF	C3	0.1µF(ceramic) +10µF
C4	0.1µF(ceramic) +10µF	C5	0.1µF(ceramic) +10µF	C6	0.1µF(ceramic)
C7	0.1µF(ceramic)	C8	0.1µF(ceramic)	C9	0.1µF(ceramic)
C10	0.1µF(ceramic)	C11	0.1µF(ceramic)	C12	0.1µF(ceramic)
R1	1.5kΩ				

Signal Descriptions

Power Supplies and Ground

Table 6: Power Supplies and Ground

Name	Description	DC Value (V)			Ripple (V)	Comments
		Min	Typ	Max		
VDD	Digital power supply	1.7	1.8	1.9	-	
VAA	Analog power supply	2.8	3.0	3.2	100	Must be separated from VAA_PIX
VAA_PIX	Pixel power supply	2.8	3.0	3.2	100	
VDD_HiSPi	HiSPi power supply	0.35	0.4	0.45	-	
VDD_PLL	PLL power supply	2.7	2.8	2.9	-	
DGND	Digital ground	-			-	
AGND	Analog ground	-			-	

Absolute Ratings

Table 7: Absolute Maximum Ratings

Name	Definition	Absolute Max Value
Supply Name		(V)
VDD	Digital power supply	2.85
VAA	Analog power supply	4.8
VAA_PIX	Pixel power supply	4.8
VDD_HiSPi	HiSPi power supply	0.675
VDD_PLL	PLL power supply	4.35
Current		(mA)
I_{Supply}	Maximum supply to power input	300
I_{GND}	Maximum negative supply to GND	-100

Table 8: Absolute Minimum and Maximum Temperature Ratings (°C)

Symbol	Definition	Min	Max
^{t}OP	Operating temperature	-10	70
^{t}PE	Performing temperature	-10	60
^{t}ST	Storage temperature	-30	80

Note: All temperature is defined by chip surface.

Bias/Analog Test Signals

Table 9: Bias/Analog Test Signals

Name	Type	Description
VRS_HI	Decoupling	External noise decoupling. Internal analog voltage.
VRST_LO	Decoupling	External noise decoupling. Internal analog voltage.
VTX_LO1	Decoupling	External noise decoupling. Internal analog voltage.
VTX_LO2	Decoupling	External noise decoupling. Internal analog voltage.
VDCG_HI	Decoupling	External noise decoupling. Internal analog voltage.
VDCG_LO1	Decoupling	External noise decoupling. Internal analog voltage.
VDCG_LO2	Decoupling	External noise decoupling. Internal analog voltage.
ATEST_TOP	Test	Reserved for test. Tied to VAA.
ATEST_BOT	Test	Reserved for test. Tied to VAA.
VREF1_TOP	Test	Reserved for test. Must be opened.
VREF1_BOT	Test	Reserved for test. Must be opened.
VBIAS_TOP	Test	Reserved for test. Must be opened.
VBIAS_BOT	Test	Reserved for test. Must be opened.

Digital Signals

Voltage levels for digital input are:

LOW: -0.3V to 0.3V

HIGH: VDD-0.3V to VDD+0.3V

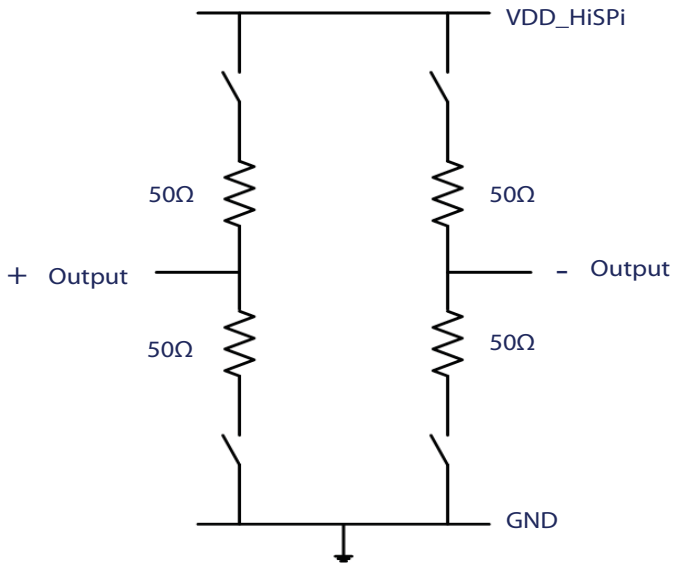
Table 10: Digital Signals

Name	I/O Type	Description	Input Capacitance (Typical)
DATA_[23:0]_P	O	Differential data of channel [23:0], HiSPi, positive	-
DATA_[23:0]_N	O	Differential data of channel [23:0], HiSPi, negative	-
D_CLK_[5:0]_P	O	Differential clock[5:0], DDR, HiSPi, positive	-
D_CLK_[5:0]_N	O	Differential clock[5:0], DDR, HiSPi, negative	-
EXTCLK	I	External clock input. Typical 48.000 MHz.	2.6 pF
RESET_B	I	Hard reset. Low active.	6 pF
SCLK	I	Serial I/F clock.	6 pF
SDATA	I/O	Serial I/F data input/output	6 pF
TRIGGER	I	Trigger input for starting exposure or starting readout in Full Resolution mode. Also controls operation start timing in video modes.	7.9 pF
PHY_STABLE	O	Output signal which indicates the status of HiSPi PHY.	
TEST	I	Reserved for test. Must be tied to DGND.	
OM1	I	Reserved for test. Must be tied to DGND	
OM2	O	Reserved for test. Must be opened.	

HiSPi™Output Equivalent Circuit

HiSPi™ Output signal DATA_P, DATA_N, D_CLK_P, D_CLKL_N are composed as the equivalent circuit below.

Figure 5: HiSPi™ Output Equivalent Circuit



Power Consumption Estimate

Table 11: Max Power Consumption without HiSPi™ Power Save with Typical Power Supply Voltages at 30°C

Name	Current Consumption (mA)										
	(V)	Wait TRIGGER	Full Res	HDTV	Pre-Flash B	EVF	Pre-Flash A	HD60_16:9_LP	HD60_16:9_FS	Hi-Speed	Super Hi-Speed
VDD	1.8V	134.8	236.5	178.2	147.0	187.7	148.6	202.9	201.7	235.2	232.7
VAA	3.0V	74.8	259.0	172.6	141.1	170.7	141.1	172.8	255.9	258.6	257.6
VAA_PIX	3.0V	38.9	56.8	42.4	42.9	42.9	42.9	41.6	57.8	56.7	56.5
VDD_HiSPi	0.4V	0.01	59.9	17.6	13.4	28.6	13.3	36.7	42.8	59.9	59.9
VDD_PLL	2.8	9.6	9.6	9.6	9.6	9.6	9.6	9.6	9.6	9.6	9.6
Total power (mW)			1400								

Notes: 1. When previous operating mode is full resolution or Hi-Speed or Super Hi-Speed modes, HiSPi™ drivers keep output during the Wait TRIGGER. When the previous operating mode is one of the other video modes, HiSPi drivers are in power save status, therefore VDD_HiSPi current is cut off.

Table 12: Max Power Consumption without HiSPi™ Power Save and Inverter Amp OFF with Typical Power Supply Voltages at 30°C

Name	Current Consumption (mA)										
	(V)	Wait TRIGGER	Full Res	HDTV	Pre-Flash B	EVF	Pre-Flash A	HD60_16:9_LP	HD60_16:9_FS	Hi-Speed	Super Hi-Speed
VDD	1.8V			176.8	147.1	186.2	148.7	199.0	202.1	236.1	233.5
VAA	3.0V			143.0	108.6	141.0	108.6	143.6	197.6	202.5	201.8
VAA_PIX	3.0V			42.7	43.2	43.0	43.1	43.0	58.1	57.1	57.0
VDD_HiSPi	0.4V			17.5	13.4	28.5	13.4	36.4	41.9	58.6	58.7
VDD_PLL	2.8			9.6	9.6	9.6	9.6	9.6	9.6	9.6	9.6

Notes: 1. Wait trigger status doesn't depend on Inv Amp status. The Full Resolution Mode power difference trend between inverter amp ON and OFF is same as Super Hi-Speed Mode.

External Pulse Timing

The EXTCLK frequency is specified at 48.000 MHz for the standard video formats.

The AR1011HS employs internal PLL, which generates internal master clock from EXTCLK. All the circuits in the AR1011HS operate with the internal master clock asynchronously against EXTCLK. Therefore, the rise and fall time of TRIGGER to EXTCLK is not so sensitive to the sensor operation. However, the AC parameters to TRIGGER are critical and have to stay in the values specified in the next chapter.

Figure 6: External Pulse Timing

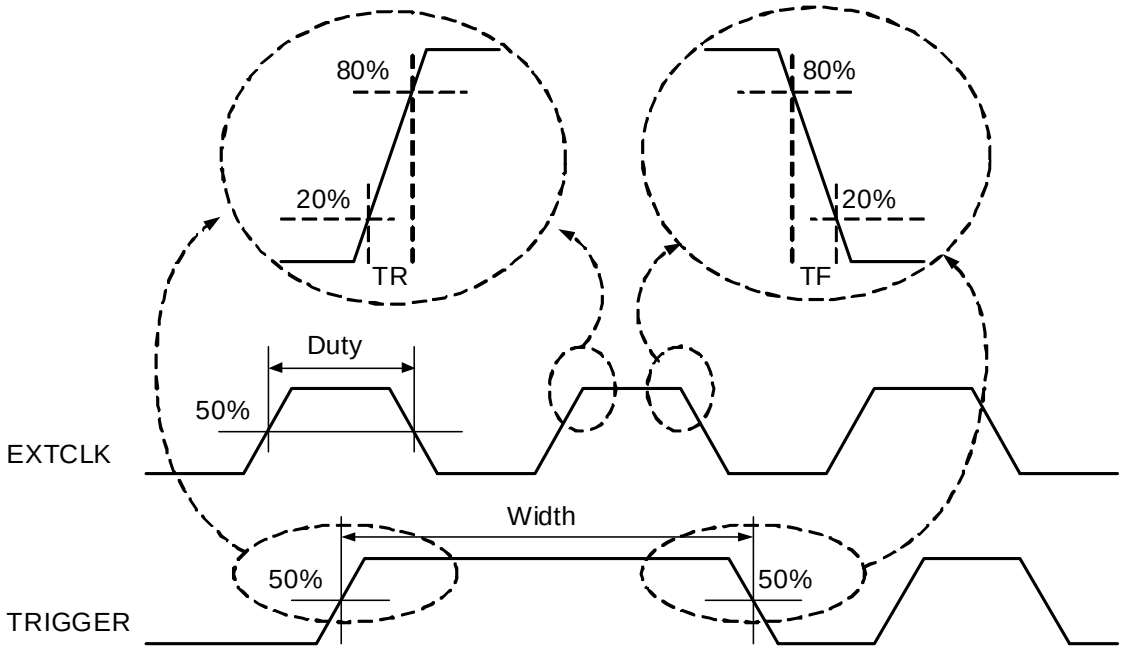


Table 13: External Pulse Definition

Name	Description	Min	Typ	Max	Unit
EXTCLK	External clock	24 [1]	48.000	48.050	MHz
Duty	EXTCLK clock duty	45	50	55	%
Jitter	EXTCLK clock jitter	–	–	1	%
Width	TRIGGER width	See “TRIGGER” on page 20.			
TR	Rise time	–	–	5	ns
TF	Fall time	–	–	5	ns

Note: 1. When DLL phase adjuster is disabled.

RESET_B

RESET_B is a control pulse for the hard reset. At the power- on period, RESET_B must be set at LOW, then must be set HIGH after the VDD power supply voltages are settled. The minimum RESET_B is required for the specific time to assert the initialization as mentioned below (see "Power Up Sequence" on page 23).

RESET_B initializes the internal PLL. All outputs are halted when RESET_B is asserted. Minimum RESET_B Assert Time is 30 EXTCLK cycles.

Table 14: Signal I/O Status During RESET_B

Name	Status
DATA_[23:0]_P	High-Z
DATA_[23:0]_N	High-Z
D_CLK_[5:0]_P	High-Z
D_CLK_[5:0]_N	High-Z
SDATA	Input state
PHY_STABLE	High-Z

TRIGGER

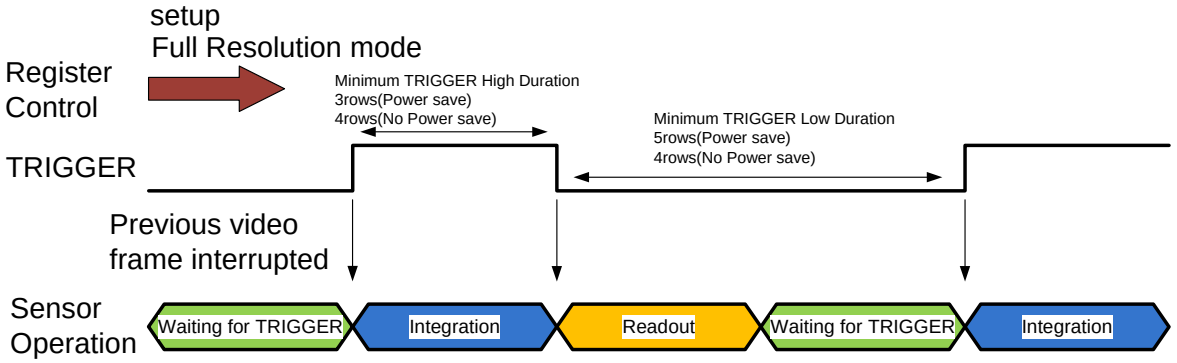
The TRIGGER signal controls the operation start timing. The roles of TRIGGER input are different in the video modes and the Full Resolution mode. In the Full Resolution mode, the TRIGGER rising edge determines the start of reset scan, which minimizes shutter lag. The TRIGGER falling edge determines the start of readout scan. On the other hand, the TRIGGER rising edge determines the start of readout timing in the video modes, so that the image sensor can synchronize to the camera system VD.

Table 15: Minimum External TRIGGER High Duration

Mode	Full Resolution (Power Save)	Full Resolution (No Power Save)	Video Mode
Minimum TRIGGER High Duration	3 rows	4 rows	10 clk
Minimum TRIGGER Low Duration	5 rows	4 rows	–

Note: If TRIGGER low duration is shorter than minimum TRIGGER low duration, the readout frame is corrupted. TRIGGER High duration in Full Resolution Mode must be a multiple of 1 row cycle.

Figure 7: TRIGGER Control in Full Resolution HD_60_3:2_SLV, HD_120_16:9_SLV Mode



TRIGGER high and low durations are strongly recommended to be set to the multiples of a row time. When a TRIGGER edge overlaps with an internal HD timing, it can cause fluctuation of integration or frame readout timing. Toggling TRIGGER at timings of multiples of the row duration provides identical margin between TRIGGER toggling to the internal HD, which avoids generating the fluctuation.

Figure 8: TRIGGER Timing Recommendation in Full Resolution HD_60_3:2_SLV, HD_120_16:9_SLV Mode

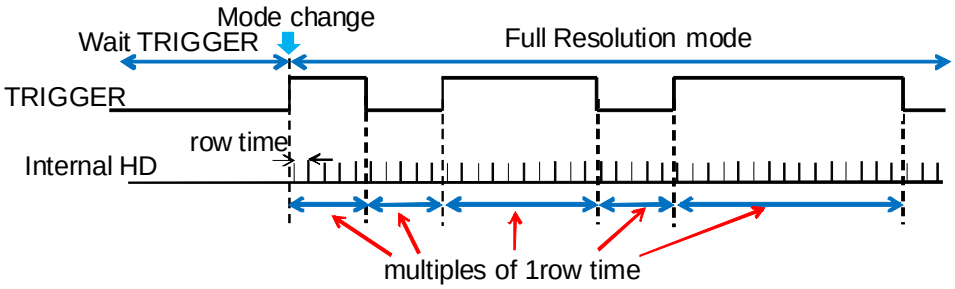


Figure 9: TRIGGER Timing and Internal HD in Full Resolution HD_60_3:2_SLV, HD_120_16:9_SLV Mode

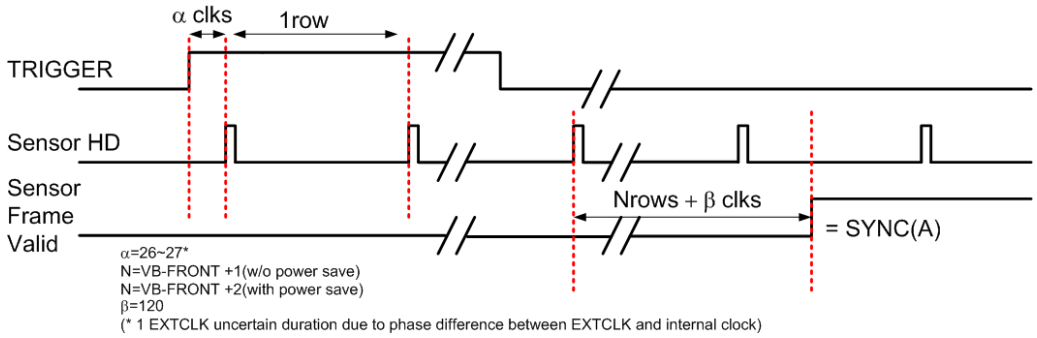


Figure 10: TRIGGER Control in Video Mode

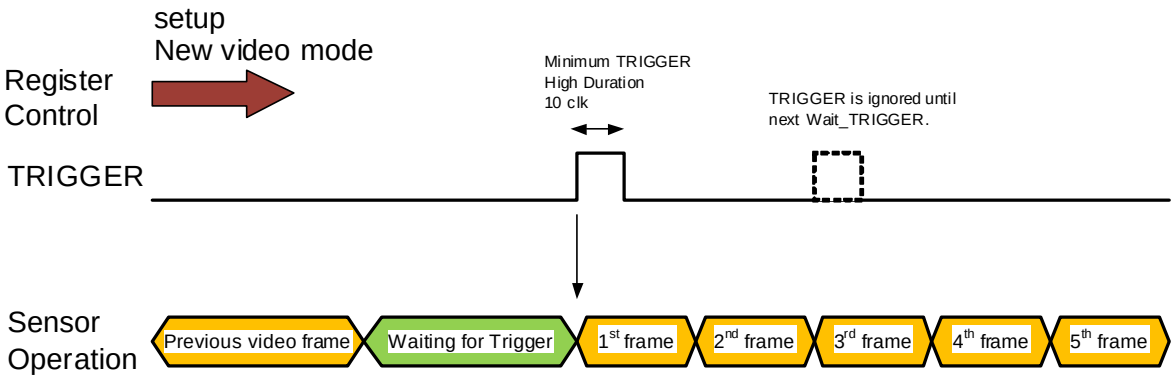
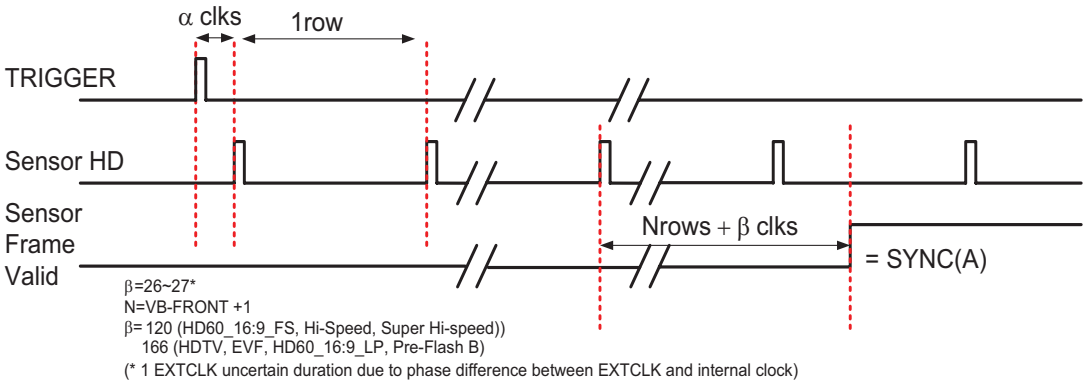


Figure 11: TRIGGER Timing and Internal HD in Video Mode



PHY_STABLE

When PHY_STABLE is HIGH, the HiSPi PHY transmitter output is stable. When the PHY_STABLE output is LOW, the sensor is in the power save mode and the differential data output is invalid.

Power Up and Down Sequences

To minimize supply current in power up and power down sequences, the power up and down sequences specified in this section are required. Also, the sensor needs setup time tpu5, tpu6, and tpu7 for internal logic initialization, PLL phase lock, and register default setup, respectively.

Power Up Sequence

Figure 12: Power Up Sequence

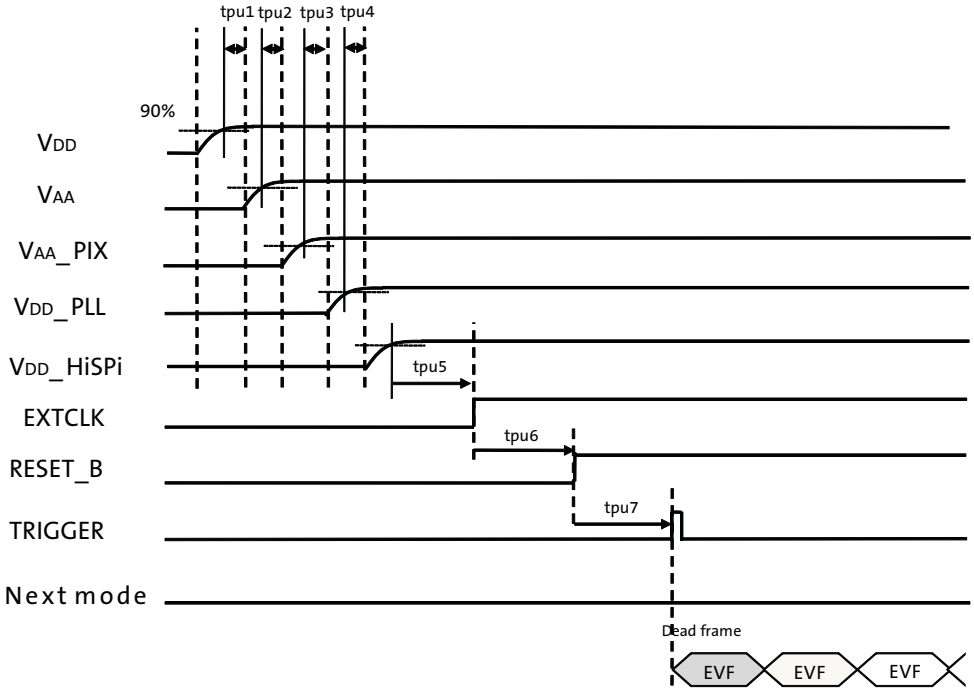


Table 16: Power-up Sequence Timing Parameters

Parameter	Min	Max
tpu1	0 ms[1]	–
tpu2	0 ms[1]	–
tpu3	0 ms[1]	
tpu4	0 ms[1]	–
tpu5	0.5 ms	–
tpu6	0.5 ms	–
tpu7	1.1 ms	–

Note: 1. Simultaneous power shut down is available; however, to avoid extra current, waiting for voltage of the previous power supply in the sequence to settle down is preferred.

Power Down Sequence

Figure 13: Power Down Sequence

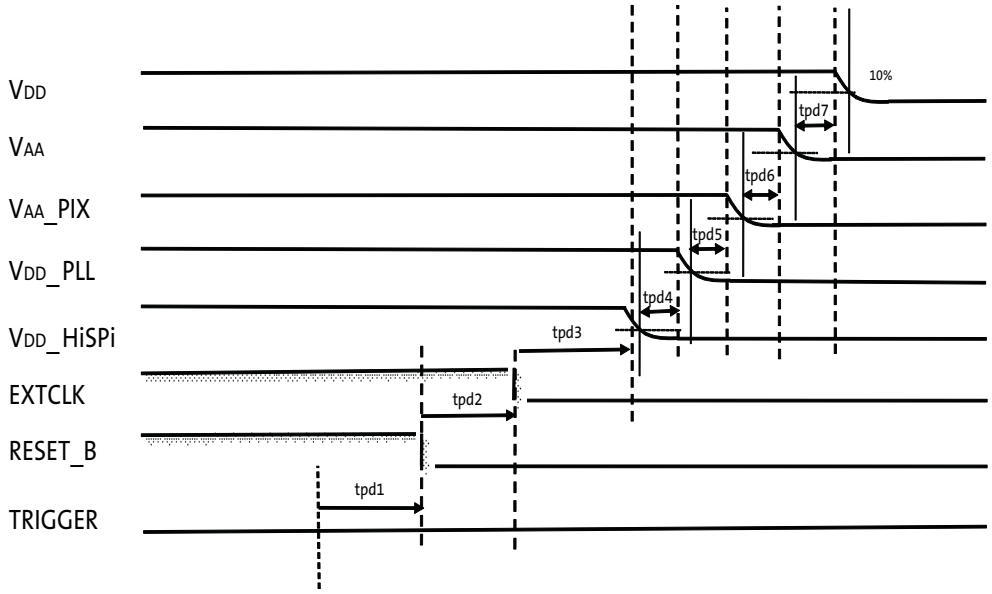


Table 17: Power Down Sequence Timing Parameters

Parameter	Min	Max
tpd1	0.5ms	–
tpd2	0.5ms	–
tpd3	0.5ms	–
tpd4	0ms[1]	–
tpd5	0ms[1]	–
tpd6	0ms[1]	–
tpd7	0ms[1]	–

Notes:
1. Simultaneous power shut down is available; however, to avoid extra current, wait for the voltage of the previous power supply in the sequence to settle down.
2. Register address 0x301A should be set to 0x10D0 once before RESET_B settles down.

AR1011HS HiSPi™ Video Interface (I/F)

HiSPi™(High Speed Serial Pixel) is Aptina's original simple logical layer protocol with low power consumption and high-speed interface, which is scalable to accommodate increasing sensor resolutions and high frame rates for advanced digital still cameras (DSC), digital video cameras (DVC), and digital single-lens reflex (DSLR) camera applications.

The interface calls for serial pixel data transmitter on multiple serial lanes. The number of data lanes will be determined by the desired frame rate, bit depth, maximum data rate, and sensor resolution for a particular design.

The HiSPi™ interface enables high bandwidth data transfer for both video and still images. It consists of both data and clock signaling that can be scaled to the required data transfer for an application.

The HiSPi™ interface specification defines the physical layer covering the transmission medium, electrical parameters, signaling and timing relationship between the clock lane and data lanes, the logical protocol layer covering data formats, and synchronization.

The HiSPi™ interface building block is a unidirectional differential serial interface with four data lanes and one double data rate (DDR) clock lane. The interface is scalable with multiple instantiations of this block. One clock for every four serial data lanes is provided for phase alignment across multiple lanes.

The AR1011HS video output I/F is designed based on HiSPi™ Rev. C Standard with several modifications for the AR1011HS-specific application. In this document, the name of HiSPi™ is used to differentiate from the Aptina standard HiSPi™ Rev.C

Basic Features

Following are the features of HiSPi™ in the AR1011HS

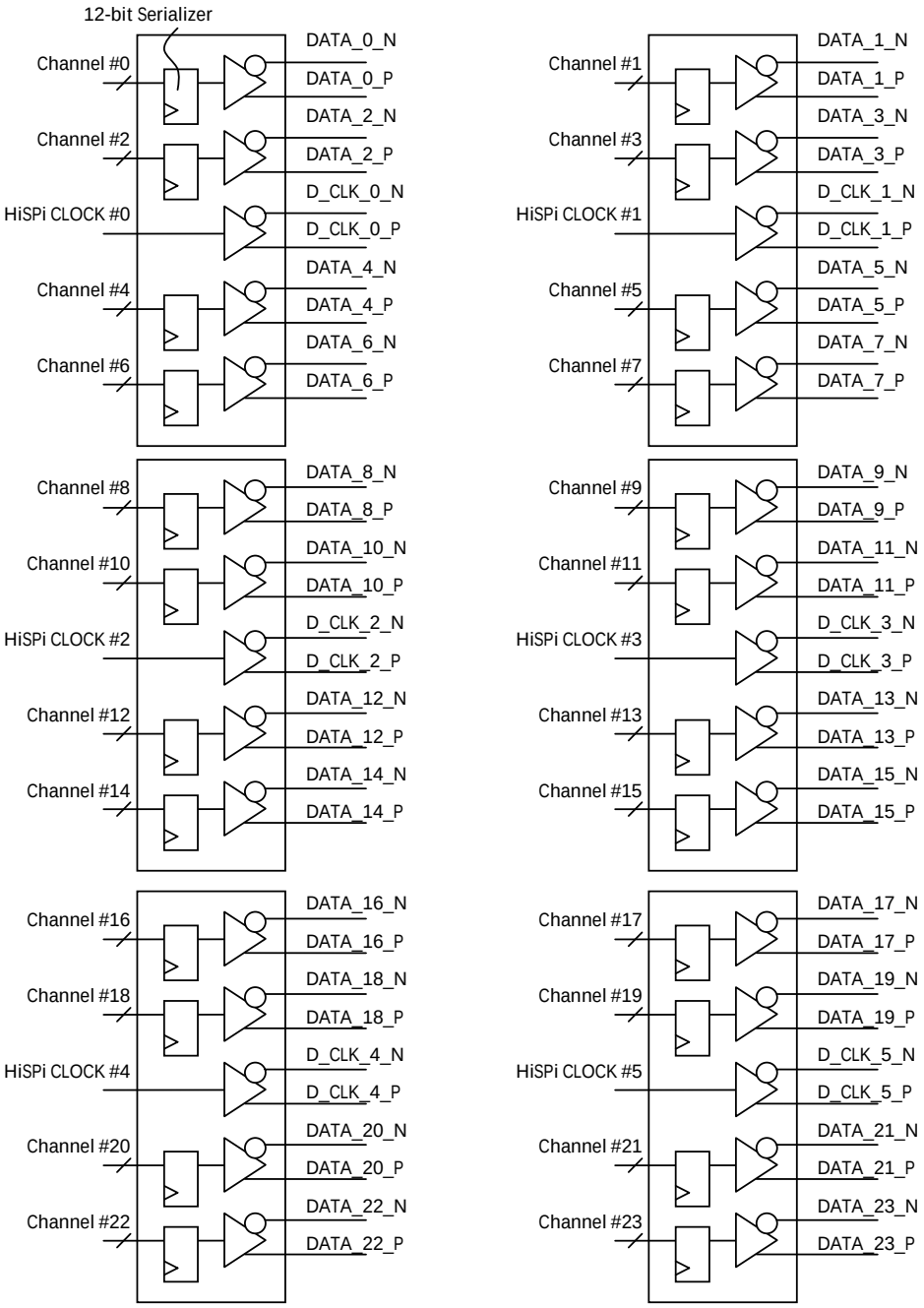
- A low voltage, low power consumption driver
- 12-bit data format only
- Data rate of 576 Mbps and 288 MHz DDR clock at 48 MHz EXTCLK
- 24 data lanes plus 6 clock lanes
- Embedded sync codes
- Each lane outputs individual pixel signals
- Output common voltage: 0.2V typical

Transmitter PHY Structure in the AR1011HS

The 24 data output lanes are laid out in the 6 physical blocks. One block corresponds to one PHY and each block consists of 4 data lanes and one clock lane. The output data is synchronized to a DDR clock in the same block. Latching data by the clock in the corresponding block is required to receiver.

Pixel data rate from each lane is identical to the EXTCLK frequency.

Figure 14: 24-Lane HiSPi™ Output



AC Specifications

The external master clock and output digital format of the AR1011HS are specified at EXTCLK and 12-bit pixel resolution, respectively. Therefore, the typical data clock frequency and data rate per lane are also specified at 6 x EXTCLK (DDR) and EXTCLK x 12 bps/Hz, respectively.

Figure 15: AC Parameters

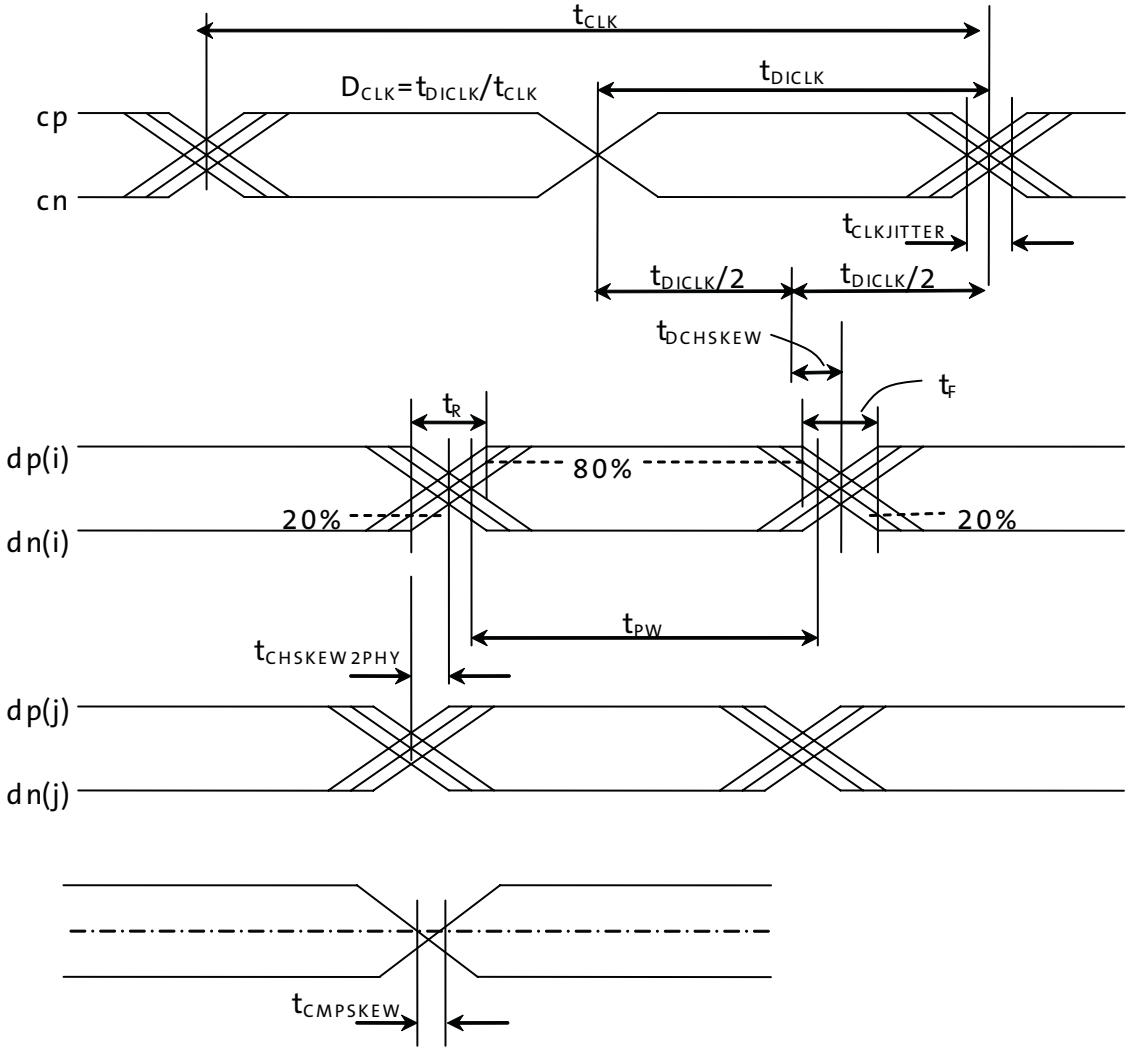


Table 18: HiSPi™ Basic AC Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data rate	$1/t_{DICLK}$	288(*1)	576	576.6	Mbps	Master clock 48 MHz and 12-bit output (*1)When EXTCLK reduced to 24 MHz. Need DLL disabled
Clock period	t_{CLK}		3.472		ns	DDR clock period
Data period	t_{DICLK}		1.736		ns	1/2 of DDR clock period t_{CLK}
Clock to data skew	$t_{DCHSKEW}$			±200	ps	DLL disabled
Data Eye width	t_{PW}	1490			ps	CLK 288 MHz, 576 Mbps. DLL disabled
Clock jitter	$t_{CLKJITTER}$	-	-	±140	ps	DLL disabled
Rise time	t_R	200	350	450	ps	100 Ω, 20% to 80%
Fall time	t_F	200	350	450	ps	100 Ω, 80% to 20%
Clock duty	D_{CLK}	45	50	55	%	DLL disabled
Data to data skew in any two PHY	$t_{CHSKEW2PHY}$	-	-	2	UI(*2)	DLL disabled, (*2) = t_{DICLK}
Complementary skew in differential pair	$t_{CMPSKEW}$	-	-	300	ps	DLL disabled

DC Specifications

Measurement Method

The measurements for CLOCK and all the data channels were observed with DATA using the single-ended scope probe as the differential and common-mode. DATA was set to the square wave in the HiSPi™ test pattern generator.

Figure 16: DC Parameters Transceiver

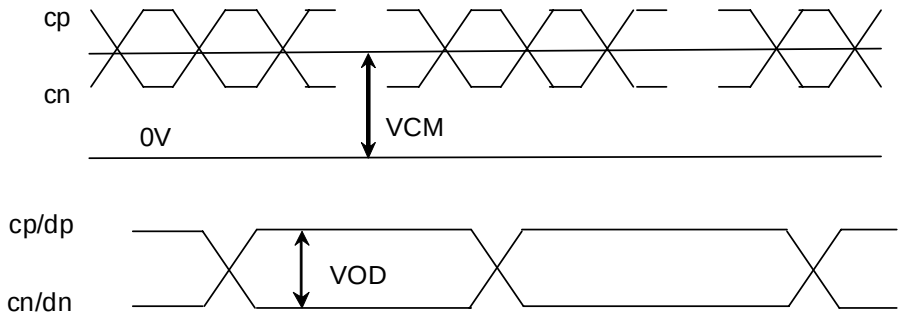


Table 19: HiSPi™ DC Performance

Symbol	Parameter	Actual Values			Unit	Conditions
		Min	Typ	Max		
V_{DD}_HiSPi	HiSPi™ power supply	0.35	0.4	0.45	V	
Vid	Input differential voltage	90(85Ω) 100(100Ω)		270(85Ω) 310(100Ω)	mV	Aptina refers to VOD
V_{ICM}	Input common mode range	150	200	245	mV	Aptina refers to V_{CM}
R_{IN}	Termination resistor	–	100	–	Ω	
DV_{ID}	V_{ID} interchannel matching	–20		20	mV	
DV_{ICM}	V_{CM} interchannel matching	–10		10	mV	
Output impedance		35	50	80	Ω	
Output impedance mismatch				20%		

DLL Timing Adjustment

Within the PHY there is a DLL connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

The DLL operation is guaranteed only at a specified data rate of 576 Mbps. The integrity of the serial data cannot be guaranteed if the DLL settings are changed while the PHYs are streaming.

Changing DLL settings in wait_trigger is recommended. If the DLL timing adjustment is not required, the data and clock lane delay settings must be set to a default code of 0x000 to reduce jitter and skew.

Figure 17: Block Diagram of DLL Timing Adjustment

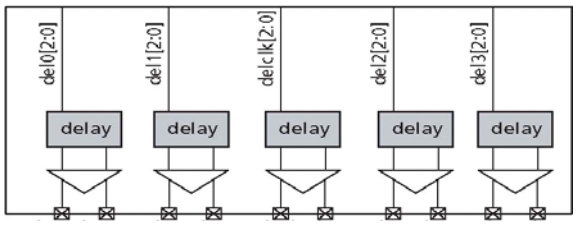


Figure 18: Delaying the clock_lane with Respect to data_lane

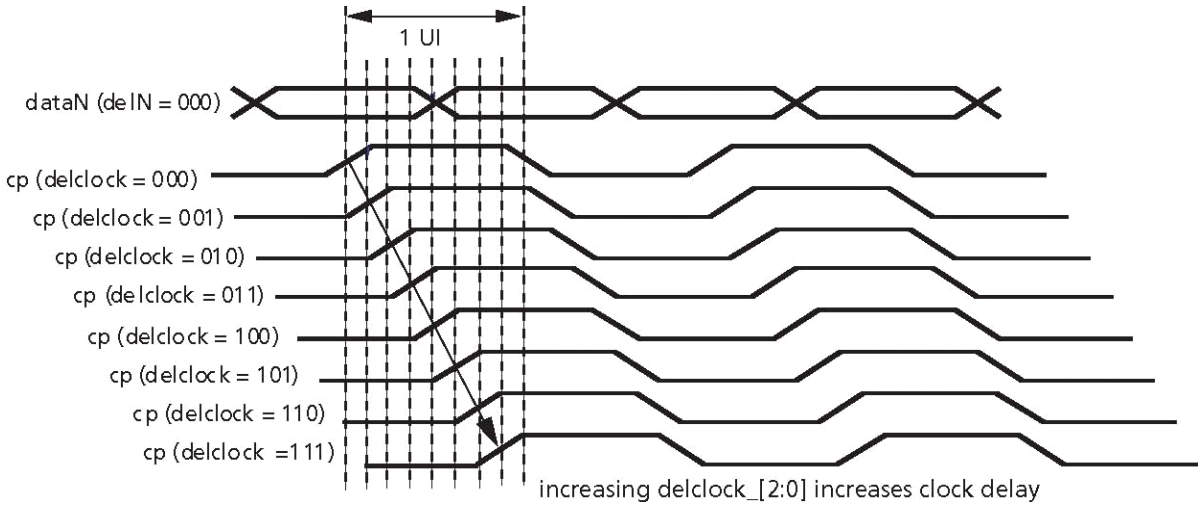


Figure 19: Delaying the data_lane with Respect to clock_lane

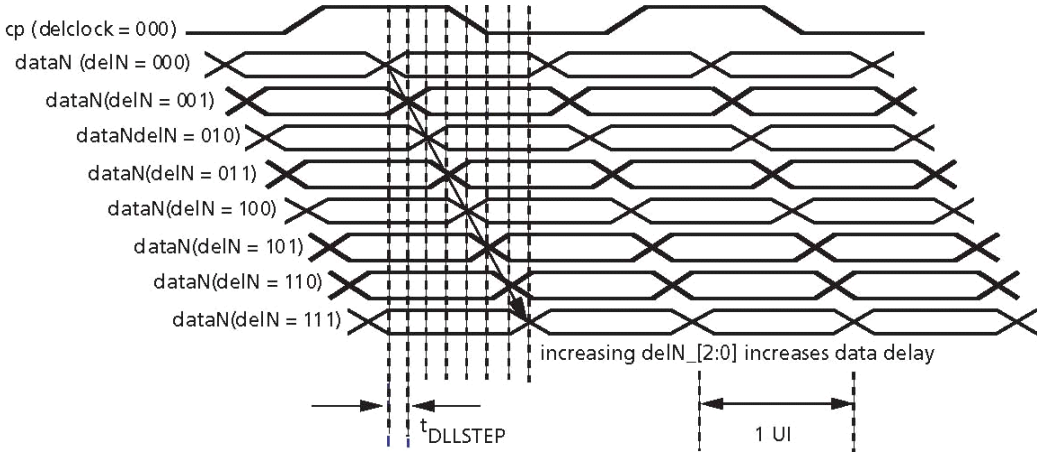


Table 20: DLL Timing Adjuster Control Register Setting

Name	Bit	Default	
del_data_lane0	2:0	0	Delay control for data lane #0
del_data_lane1	2:0	0	Delay control for data lane #1
del_data_lane2	2:0	0	Delay control for data lane #2
del_data_lane3	2:0	0	Delay control for data lane #3
del_data_lane4	2:0	0	Delay control for data lane #4
del_data_lane5	2:0	0	Delay control for data lane #5
del_data_lane6	2:0	0	Delay control for data lane #6
del_data_lane7	2:0	0	Delay control for data lane #7
del_data_lane8	2:0	0	Delay control for data lane #8
del_data_lane9	2:0	0	Delay control for data lane #9
del_data_lane10	2:0	0	Delay control for data lane #10
del_data_lane11	2:0	0	Delay control for data lane #11
del_data_lane12	2:0	0	Delay control for data lane #12
del_data_lane13	2:0	0	Delay control for data lane #13
del_data_lane14	2:0	0	Delay control for data lane #14
del_data_lane15	2:0	0	Delay control for data lane #15
del_data_lane16	2:0	0	Delay control for data lane #16
del_data_lane17	2:0	0	Delay control for data lane #17
del_data_lane18	2:0	0	Delay control for data lane #18
del_data_lane19	2:0	0	Delay control for data lane #19
del_data_lane20	2:0	0	Delay control for data lane #20
del_data_lane21	2:0	0	Delay control for data lane #21
del_data_lane22	2:0	0	Delay control for data lane #22
del_data_lane23	2:0	0	Delay control for data lane #23
del_clock_phy0	2:0	0	Delay control clock for HiSPi™ #0
del_clock_phy1	2:0	0	Delay control clock for HiSPi™ #1
del_clock_phy2	2:0	0	Delay control clock for HiSPi™ #2
del_clock_phy3	2:0	0	Delay control clock for HiSPi™ #3
del_clock_phy4	2:0	0	Delay control clock for HiSPi™ #4
del_clock_phy5	2:0	0	Delay control clock for HiSPi™ #5

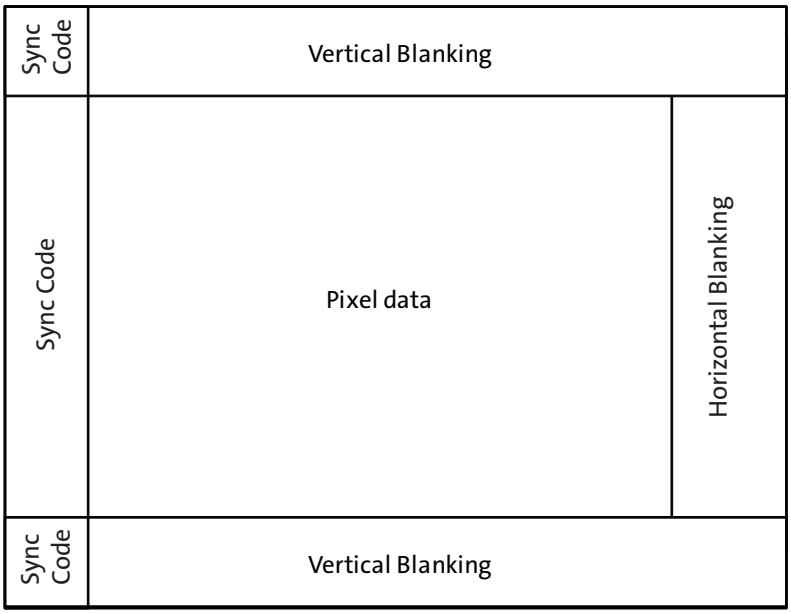
Protocol Layer

The protocol layer is positioned between the output data path of the sensor and the physical layer. The main functions of the protocol layer are generating sync codes, formatting pixel data, inserting horizontal/vertical blanking codes, and distributing pixel data over defined data lanes.

Protocol Fundamentals

Figure 20 illustrates the structure of a frame including sync code, active image, horizontal blanking, and vertical blanking, showing how data of a frame is transmitted across the HiSPi link.

Figure 20: Frame Structure for HiSPi™ Transmission



Synchronization Codes and Blanking Codes

Each line of an image frame is transmitted consecutively starting at row zero. A synchronization code (sync code) is added at the beginning of the line to alert the receiver. The active image pixel data and horizontal blanking word are transmitted after the synchronization code.

A line representing the vertical blanking will consist of the synchronization code followed by the vertical blanking words.

The sync code is a unique four-word code that is transmitted one-word-per-data-lane of the PHY, and is copied by every PHY in the link configuration. Being a unique data pattern, it can be detected by the receiver to locate the first data in an image line.

The transmitted clock of an individual PHY will have accurate control of the four data lanes. There will be minimal skew between the four data lanes.

The same transmitted clock will have less control of the data lanes in other PHYs. To minimize skew, each pair of four data lanes within a PHY should only use their transmitted clock. Also, each PHY will generate a SYNC code to compensate for any skew between PHYs.

The protocol layer will not transmit words that are all 1s or all 0s except as part of a sync code. However, a (word length) bit sequence that is all 1s or 0s might be transmitted on a serial data lane. For example, nine 1s at the end of one word can be followed by seven 1s at the start of the next.

During the blanking period, each lane will alternately transmit values of (pixel_widths) 'b011…111 and (pixel_widths) 'b100…000 (minimizing toggling of the link). Using a 12-bit word size as an example, the blanking data will result in either a stream of 23*1s including the 0xFFF sync code word in lane 0, or 23*0s including the 0x000 sync code word in lanes 2 and 4. Given that the protocol prevents any all 1s/0s word anywhere other than as part of a sync code, there will not be a stream of more than 22 bits without a transition in the active data part of the transmission. A concrete illustration of bit stream is shown in “Bit Order” on page 36.

The receiver should sync up with blanking code to align word boundary prior to detecting the sync code to avoid false sync code detection.

Figure 21: Blanking Code and Synchronization Code in a PHY (Case Data_0/2/4/6)

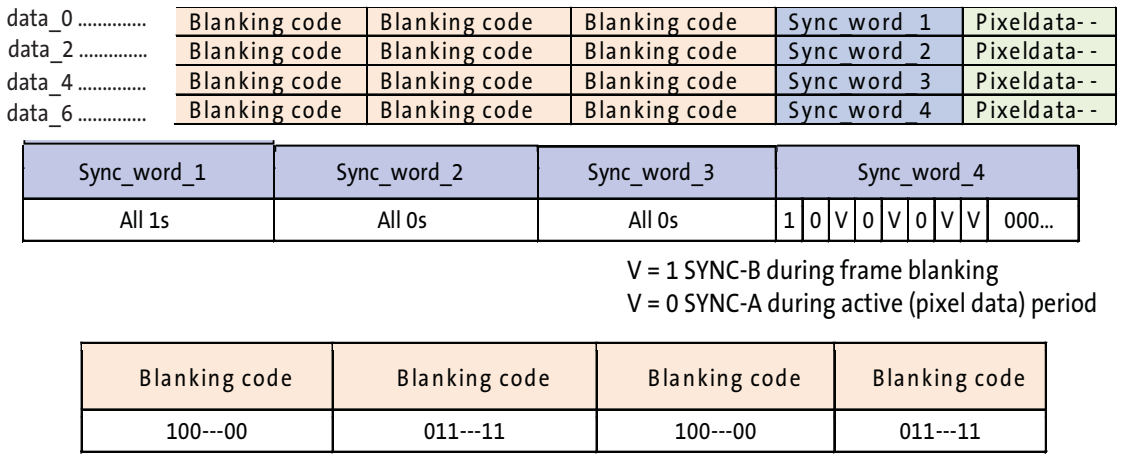


Table 21 illustrates the basic format of sync code. The code is transmitted from left to right on the line. This order is not affected by MSB first or LSB first selection.

Each "Word" has the same depth as the active image pixels. All 1 and all 0 values are unique to the sync code. The data from an active pixel will not be transmitted with these values. Table 22 on page 35 describes the sync code Word 4 for each word size preceding Active Data - SYNC (A) or Blanking Data- SYNC (B).

Table 21: Actual Binary Sync Code (Word 4)
SYNC(A) for Active Data and SYNC(B) for Blanking Data

Word Size	SYNC (A) Sync Code: Active Data	SYNC (B) Sync Code: Blanking Data
12-bit	`b1000 0000 0000	`b1010 1011 0000

Notes:
1. Sync code Word 1 (All 1s) is always transmitted on lane 0.
2. Sync code Word 2 (All 0s) is always transmitted on lane 2.
3. Sync code Word 3 (All 0s) is always transmitted on lane4.
4. Sync code Word 4 (10V0V0VV00...) is always transmitted on lane 6.

The format of the code allows the receiver to correct a single bit error in Word4 or a detection of 2 bit errors.

The protocol layer does not indicate the end of the active image data and the beginning of the horizontal blanking words in a transmitted line. The receiver must be configured to the length of the active pixel data.

Filler Codes

The synchronization code is four words. An optional filler code of "1" may be added after the sync code. When filler codes are enabled, the receiver must window the received image to eliminate the first 4 data words (columns per PHYs). In other words, if the interface is configured with 6 PHYs, the first 24 words (total columns) of a line will be filler data.

Change of filler code setting from a default value must be completed during the wait_trigger state after RESET_B release.

Table 22: Binary Representation of Filler Codes

Data Word Size	Filler Code
12- bit	'b0000 0000 0001

Figure 22: Sync Code Format with Extra Filler Codes

_0 - - - - -	Blanking code	Blanking code	Blanking code	Sync_word_1	...0001	Pixel data - -
_2 - - - - -	Blanking code	Blanking code	Blanking code	Sync_word_2	...0001	Pixel data - -
_4 - - - - -	Blanking code	Blanking code	Blanking code	Sync_word_3	...0001	Pixel data - -
_6 - - - - -	Blanking code	Blanking code	Blanking code	Sync_word_4	...0001	Pixel data - -

Table 23: Filler Code Control Register Setting

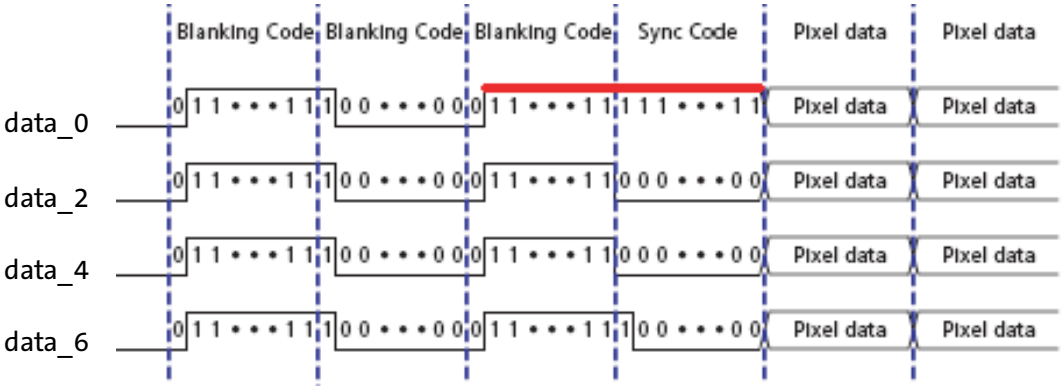
Name	Bit	Default	
vert_left_bar_en	0	0	0: filler is not embedded 1: filler is embedded

Bit Order

Pixel data may be transmitted MSB first or LSB first; it is a programmable option in the sensor. The Sync Codes, Filler Codes, and Blanking Codes are always transmitted MSB first.

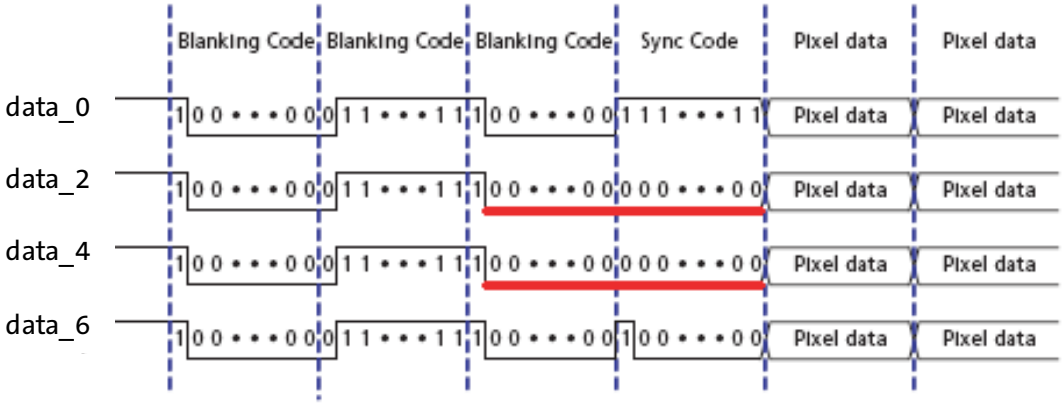
Change of bit order setting must be completed during the wait_trigger state after RESET_B release.

Figure 23: Sync Code Detection on PHY with 'b011...111 Word



23 consecutive 1s detected on lane0

Figure 24: Sync Code Detection on PHY with 'b100...000 Word



23 consecutive 1s detected on lane1, 2

Table 24: Bit Order Control Register Setting

Name	Bit	Default	
output_msb_first	0	1	0: LSB first 1: MSB first

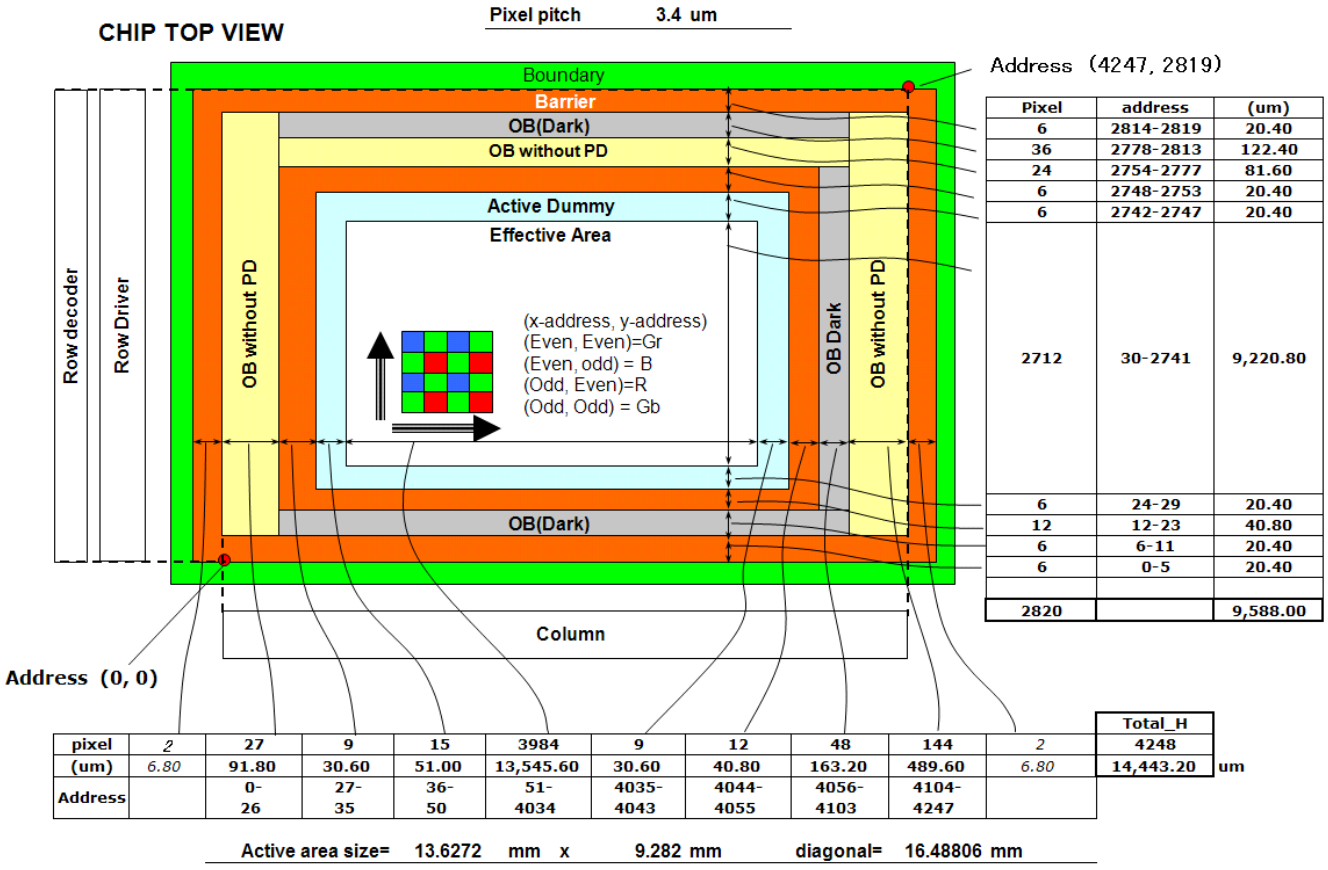
Pixel Readout

Pixel Array Configuration

The AR1011HS has a 3984 x 2712 effective pixel array, surrounded by active dummy column pixels at horizontal boundaries, and active dummy rows at vertical boundaries.

The 144 and 27 optically black (OB) columns without photodiode (PD) are located at the right side and left side, respectively. The 48 OB columns with PD are also implemented on the right side for dark offset compensation. 36 OB rows with PD and 24 OB rows without PD are located at the top of the array.

Figure 25: Pixel Array Configuration



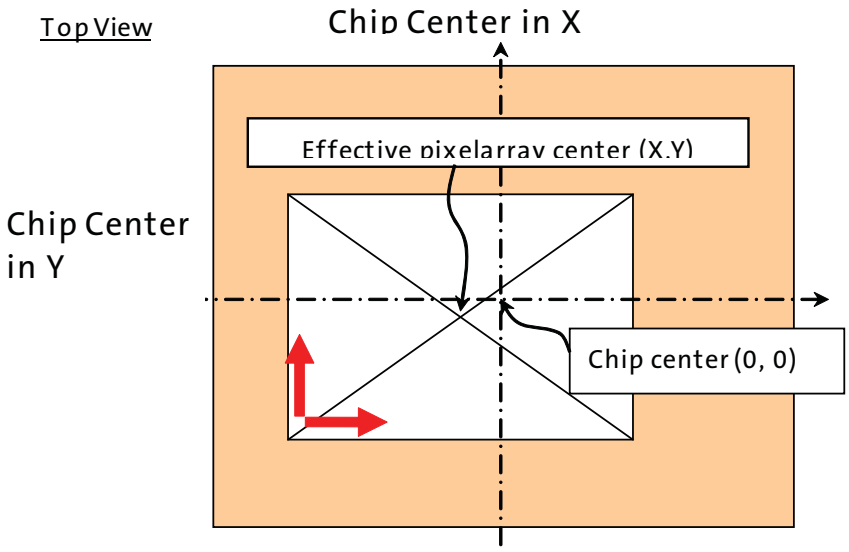
Pixel	address	(um)
6	2814-2819	20.40
36	2778-2813	122.40
24	2754-2777	81.60
6	2748-2753	20.40
6	2742-2747	20.40
2712	30-2741	9,220.80
6	24-29	20.40
12	12-23	40.80
6	6-11	20.40
6	0-5	20.40
2820		9,588.00

pixel	2	27	9	15	3984	9	12	48	144	2	Total_H
(um)	6.80	91.80	30.60	51.00	13,545.60	30.60	40.80	163.20	489.60	6.80	14,443.20 um
Address		0-26	27-35	36-50	51-4034	4035-4043	4044-4055	4056-4103	4104-4247		

Pixel Array Center Offset

The whole pixel array including OB pixels (4248 columns and 2820 rows) is located at the center of the sensor chip. Therefore, typical offset of the pixel array center is biased due to asymmetric placement of OB pixels. With the exception of mechanical variations of a package or chip location, a typical offset of the effective pixel array center is:
X = –275.4 µm and Y = –81.6 µm

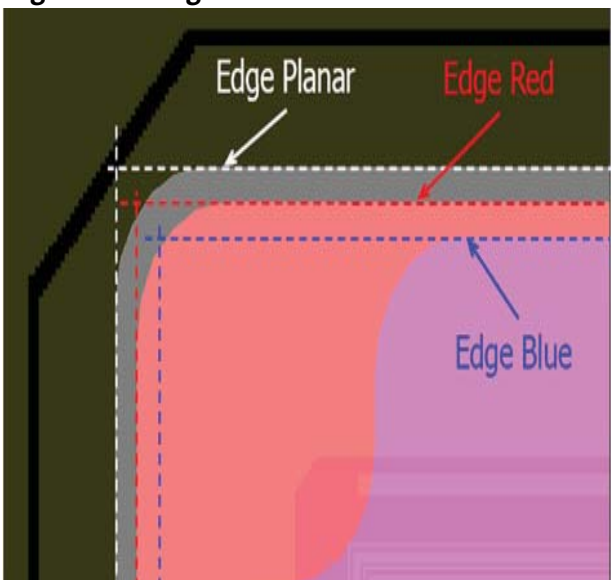
Figure 26: Chip Center and Effective Pixel Array Center



Light Block Edge

The light block edge follows the figure below when coordinates are defined with respect to Die Center (0,0) in µm.

Figure 27: Light Block Edge From Die Center



Upper Left Planar Corner
(-8711.545, 8178.745)

Upper Left Red Corner
(-8706.545, 8173.745)

Upper Left Blue Corner (notched):
(-8701.545, 8168.745)

Parallel Data Output

First, one row data is memorized in a column memory bank, then the data is scanned to be read out through the 24-lane HiSPi™. In the AR1011HS, the block readout scheme is implemented.

The column memory block is divided into 24 blocks, each having 180 column data and a HiSPi™ lane is assigned to the corresponding block. Data readout of one row is therefore completed in 180 EXTCLK cycles when the sensor is in full resolution mode.

The AR1011HS supports 3:1 column subresolution readout. In the 3:1 subresolution, the column data is reduced to 1/3; therefore, the data readout in one row will be completed in 60 EXTCLK cycles.

Figure 28: Data Lane and Column Block

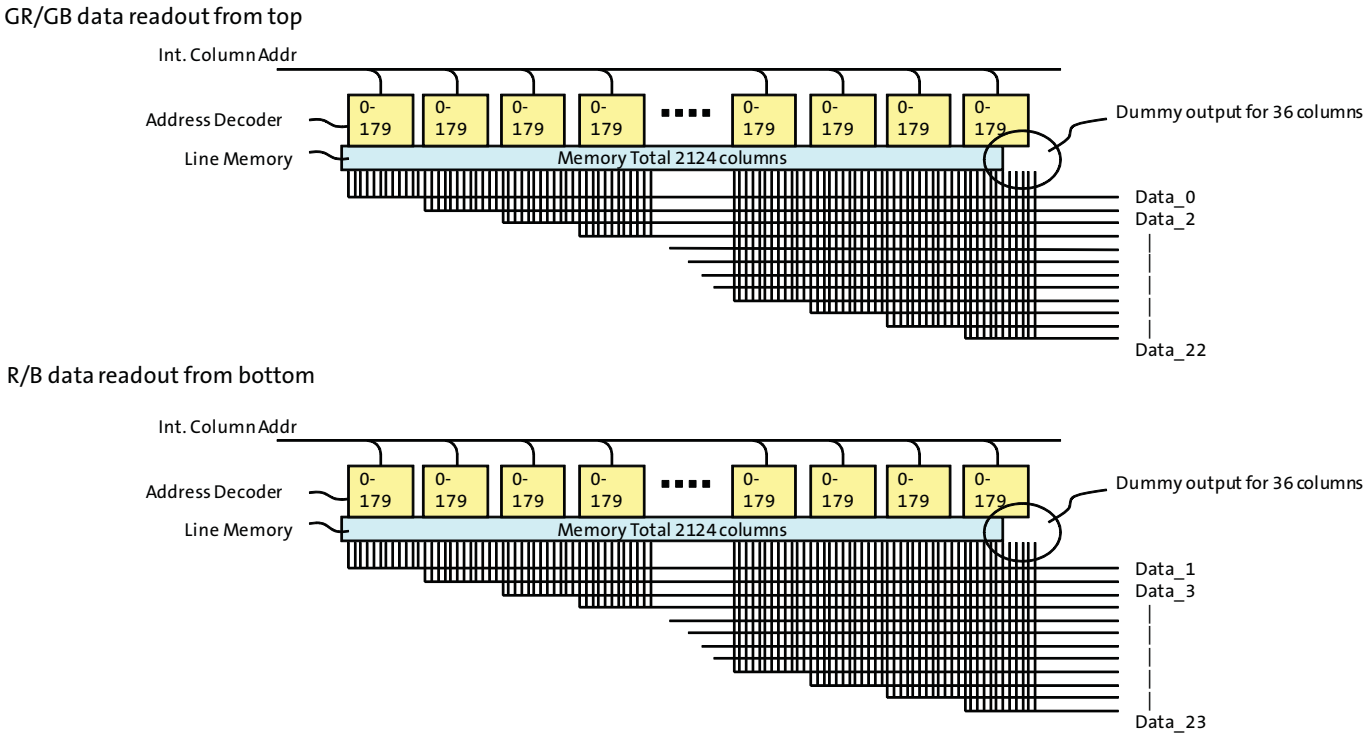


Figure 29: Data Output Stream in a Full-Column-Resolution Readout

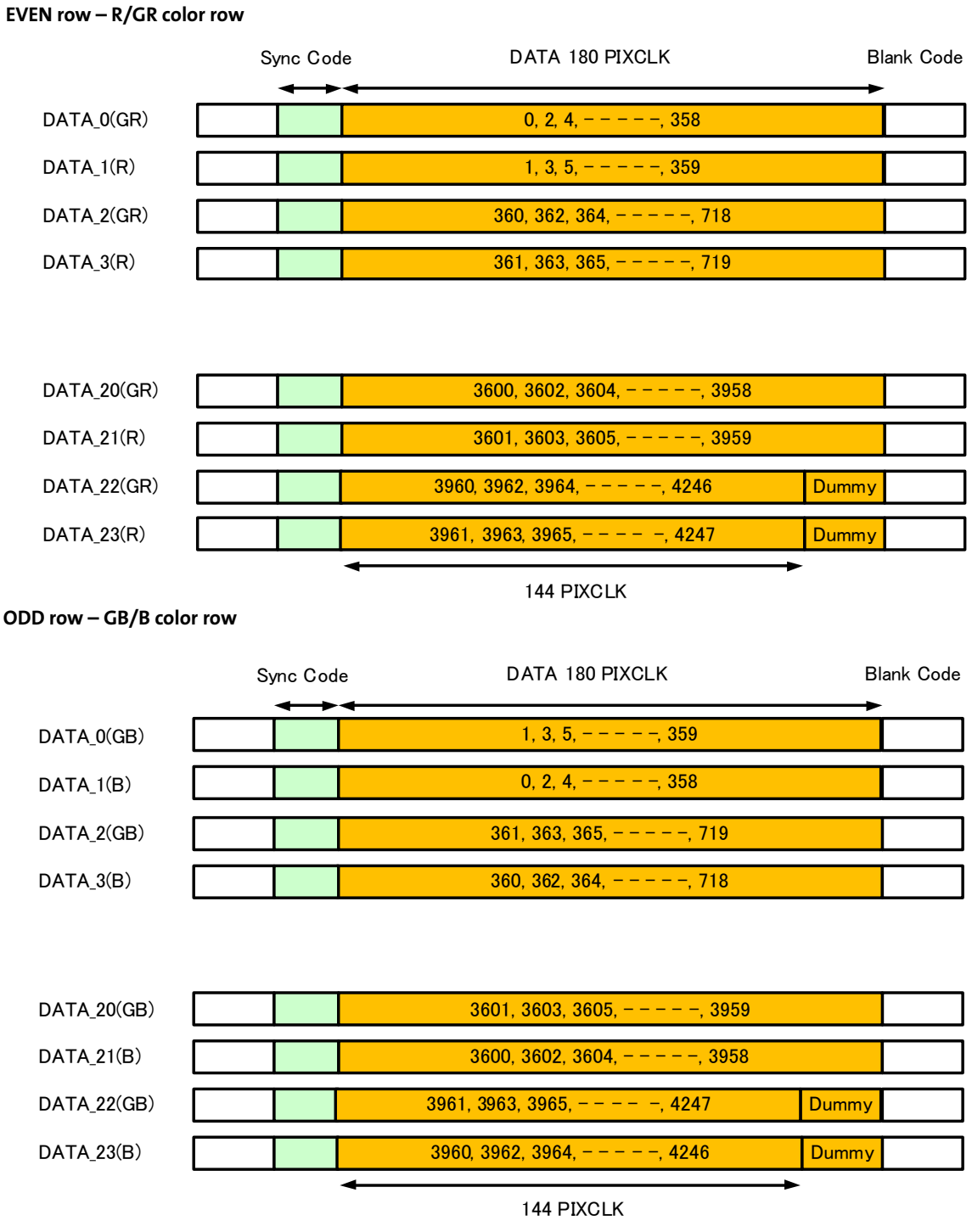
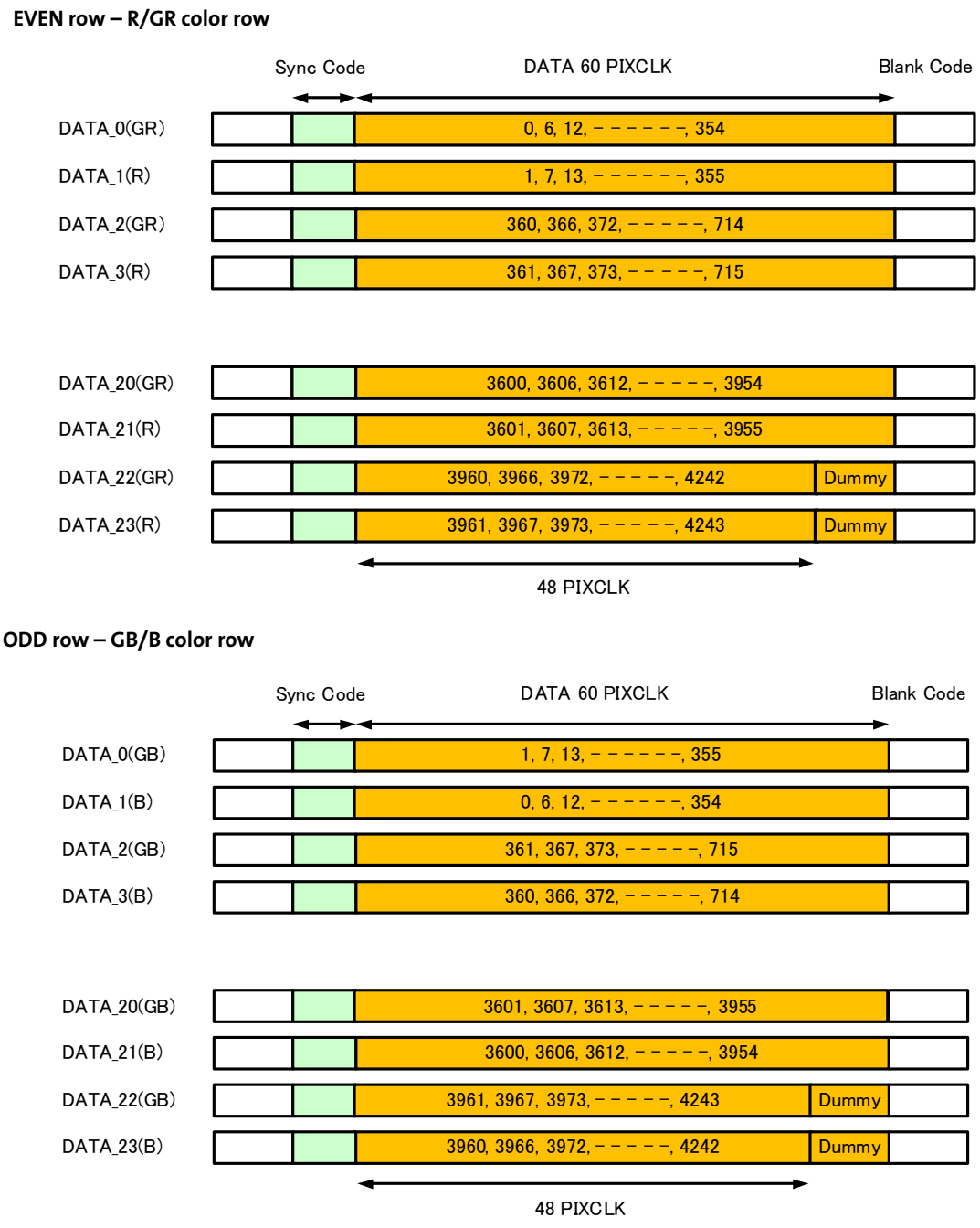


Figure 30: Data Output Stream in a 3:1 Column Subresolution Readout by Binning



Vertical Windowing

The AR1011HS supports vertically windowing readout with a serial register control. The window functions are summarized below.

- Effective pixel readout window in vertical address
- Top side OB rows with PD reading out the window in vertical address
- OB row without PD reading out the window in vertical address

Description of Subresolution Concept

The AR1011HS supports subresolution readout:

- Horizontal subresolution: 1:1 (full resolution), 3:1 binning
- Vertical subresolution: 1:1 (full resolution), 2:1 binning
- Vertical skipping: defined for each mode
- Binning performs averaging not summing

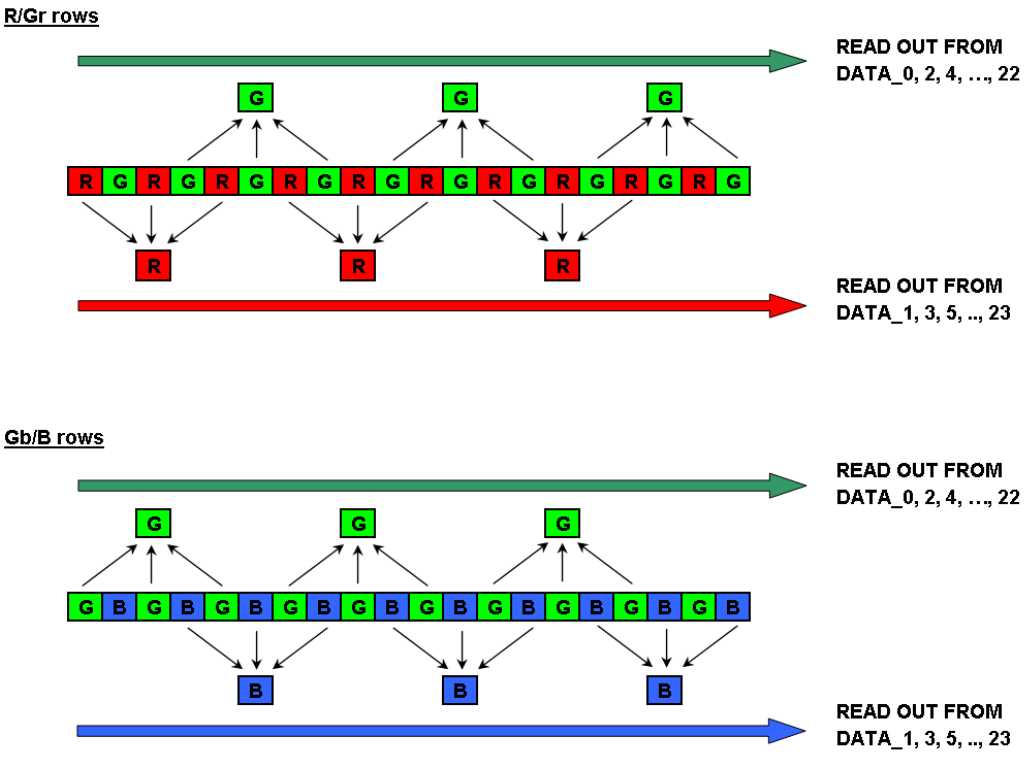
Vertical Subresolution

The vertical subresolution scheme is specified individually for each operation mode and described in “Readout Mode Control” on page 46.

Horizontal Subresolution

Only the 3:1 binning is supported for Horizontal subresolution. Figure 31 shows the 3:1 horizontal binning scheme used in the various operating modes defined in the AR1011HS.

Figure 31: Horizontal 3:1 Binning Scheme



Nesting Scan

To match the1/80 sec frame readout time requirement, a unique row addressing feature called “Nesting Scan” is introduced in the AR1011HS.

Nesting Scan

In the Nesting Scan scheme, the two adjacent rows of the same color are read out then two adjacent rows in another color plane follow. When referring to row address sequence, the operation is as shown as:

Row #0, #2, #1, #3,…, '2n', 2(n+1)', '2n+1', '2(n+1)+1', …

By using this scheme, a faster pixel readout performance is realized. On the other hand, the Nesting Scan image output requires a special signal decoding with a backend processor. Also, it results in some constraints in the minimum shutter time that will be described in “Sensor Control” on page 70.

Internal Address Operation and Data Output

Figure 32 shows the row readout sequence in Full Resolution Readout Mode, HD60_3:2_SLV, HD120_16:9_SLV, HD_60_16:9_LP, and HD_60_16:9_FS mode.

Figure 32: Nesting Scan in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV, HD_60_16:9_LP, HD_60_16:9_FS Readout Mode

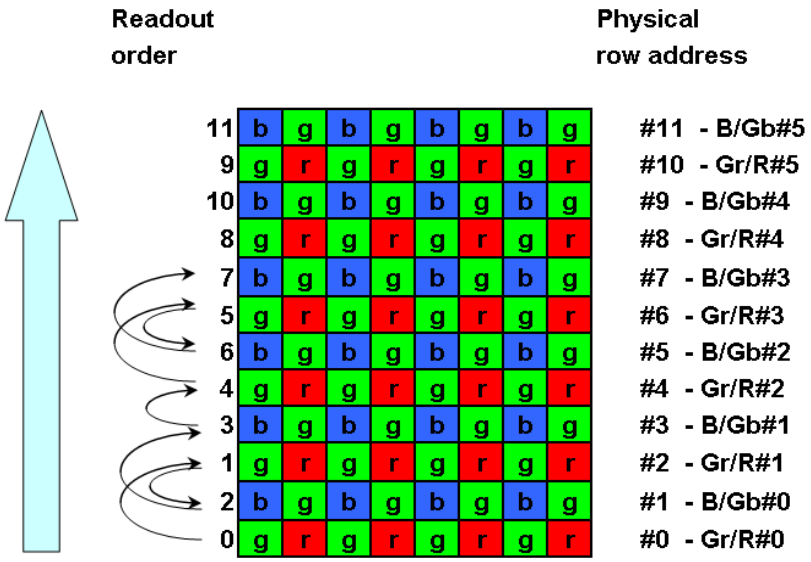
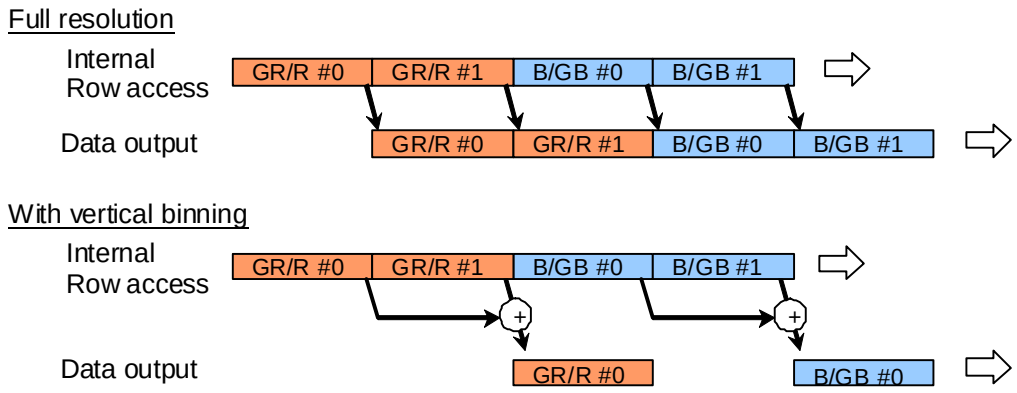


Figure 33 on page 44 shows two cases of data output sequence in Full Resolution and vertical binning modes, respectively.

When Full Resolution Readout Mode is chosen, the data output sequence is identical to the internal row addressing. On the other hand, when the vertical binning is enabled, the two continuous rows of the same color are mixed and read out. Therefore, the data output sequence from the image sensor becomes similar to that of usual readout sequence with Bayer color pixel arrangement.

Figure 33: Row Data Output Sequence

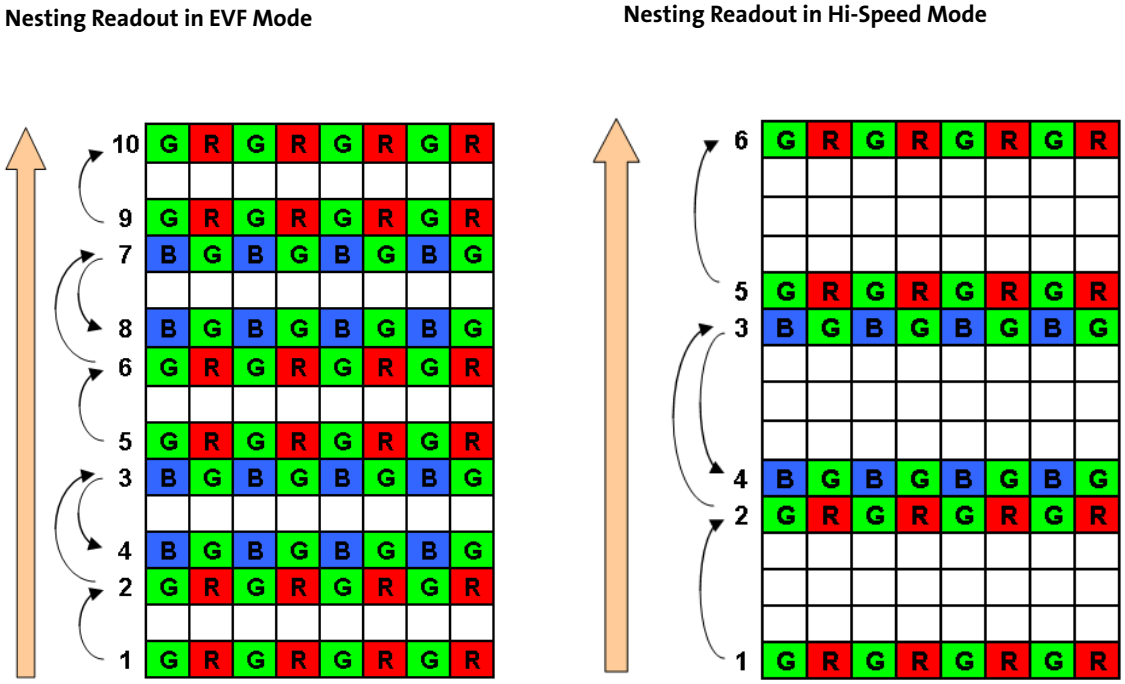


Nesting Scan in Skip Modes

When the two physically adjacent rows are read out, the Nesting Scan scheme is applied in operating modes having vertical skip readout, which include EVF Mode and Hi-Speed Mode.

For usual skip readout with constant number of skipped rows in Pre-Flash A Mode, Pre-Flash B Mode, and Super Hi-Speed mode, no Nesting Scan scheme is applied, reading out rows identically to the physical order.

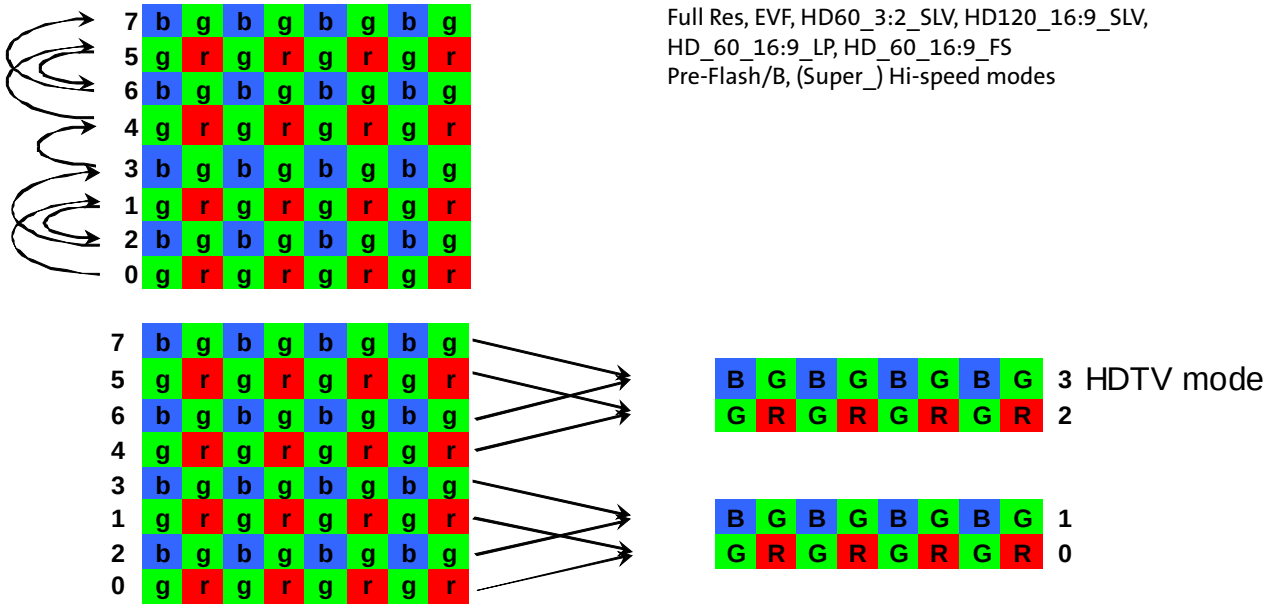
Figure 34: Nesting Scan in EVF Mode and Hi-Speed Mode



OB Without PD and OB Black Row Readout Order

All Ref Rows (OB without PD rows) are read out regardless of operation modes in the AR1011HS. Vertical skip is neglected during Ref row readout. On the other hand, vertical binning is performed for REF and OB rows, as well as for active rows in HDTV mode. Figure 36 shows the vertical readout sequence of REF and OB rows.

Figure 35: REF and OB Readout



Readout Mode Control

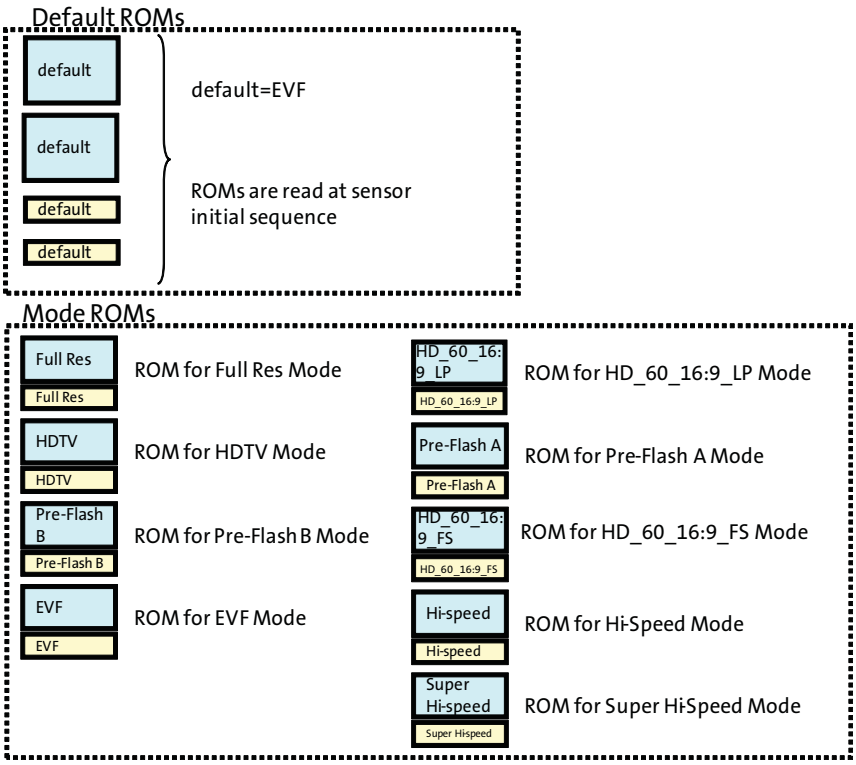
Mode Control Concept in the AR1011HS

Multiple ROM Structure

To achieve the fast mode change named “context mode switching,” the multiple ROM structure is implemented, and the ROM minimizes the registers that have to be rewritten when the mode changes. In addition to a default ROM for the default setting at power up or hard reset, multiple register sets are prepared in the individual ROMs. The user can change the operating mode only by writing a macro control register for the mode change instead of rewriting all the related registers.

EVF Mode is set up in the default ROM.

Figure 36: Multiple ROM Structure

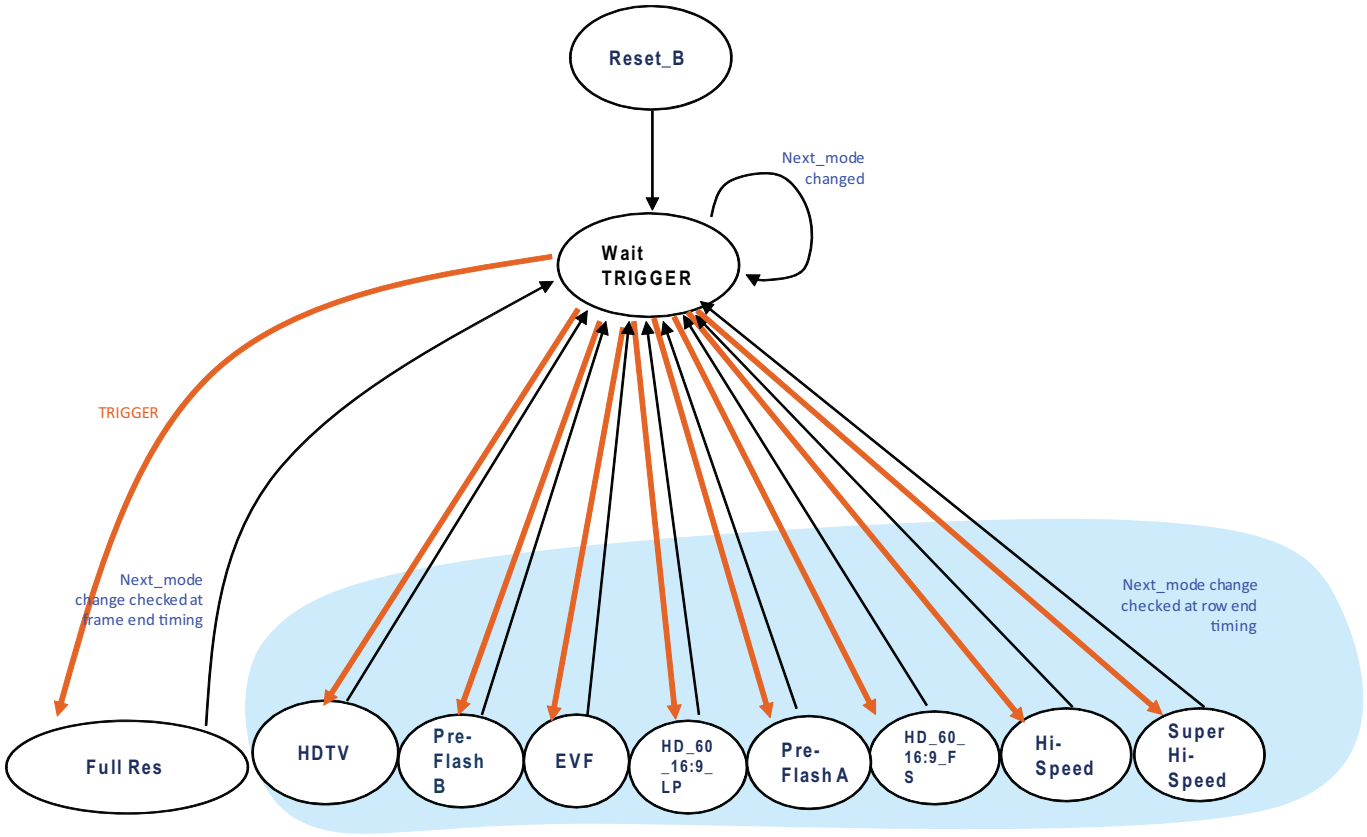


Mode Transition

In addition to the multiple ROM structures, the AR1011HS has a unique feature that enables a very short shutter release lag in Full Resolution image capturing.

- During a video mode, when the user changes the register 'next_mode', the AR1011HS immediately stops reading and gets into the Wait Trigger state.
- During Full Resolution Mode, when the user changes the register 'next_mode', the AR1011HS goes to Wait Trigger after readout of the current frame.
- When a rising edge of the TRIGGER pulse is detected, the AR1011HS starts the light integration when Full Resolution Mode is chosen.
- When a rising edge of the TRIGGER pulse is detected, the AR1011HS starts readout the captured image when a video mode is chosen.
- Setting up a new mode requires the time for internal ROM readout (200 µs at EXTCLK = 48 MHz) and the time for optional registers writing
- TRIGGER is edge-sensitive.

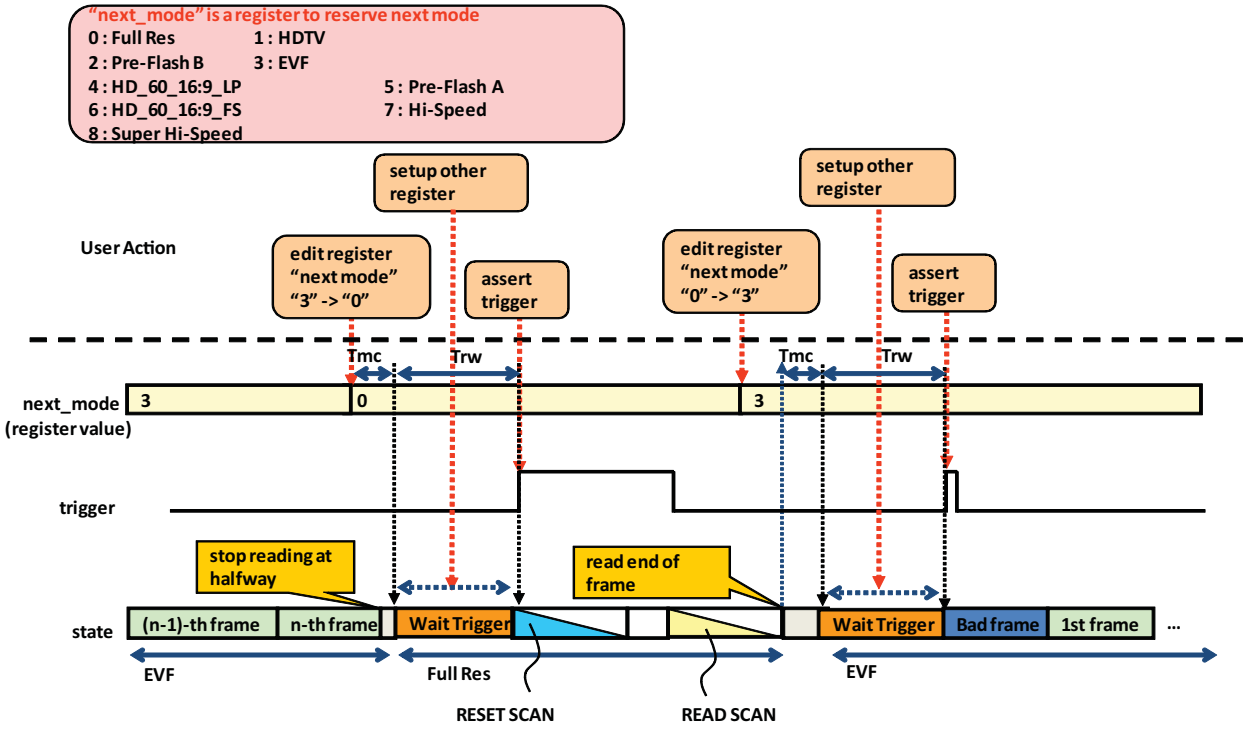
Figure 37: State Control



Note: Full Resolution mode reads out only once without changing Next_mode register. The other modes keep reading continuously until changing Next_mode register.

Mode Change Sequence (Example: EVF to Full Resolution to EVF)

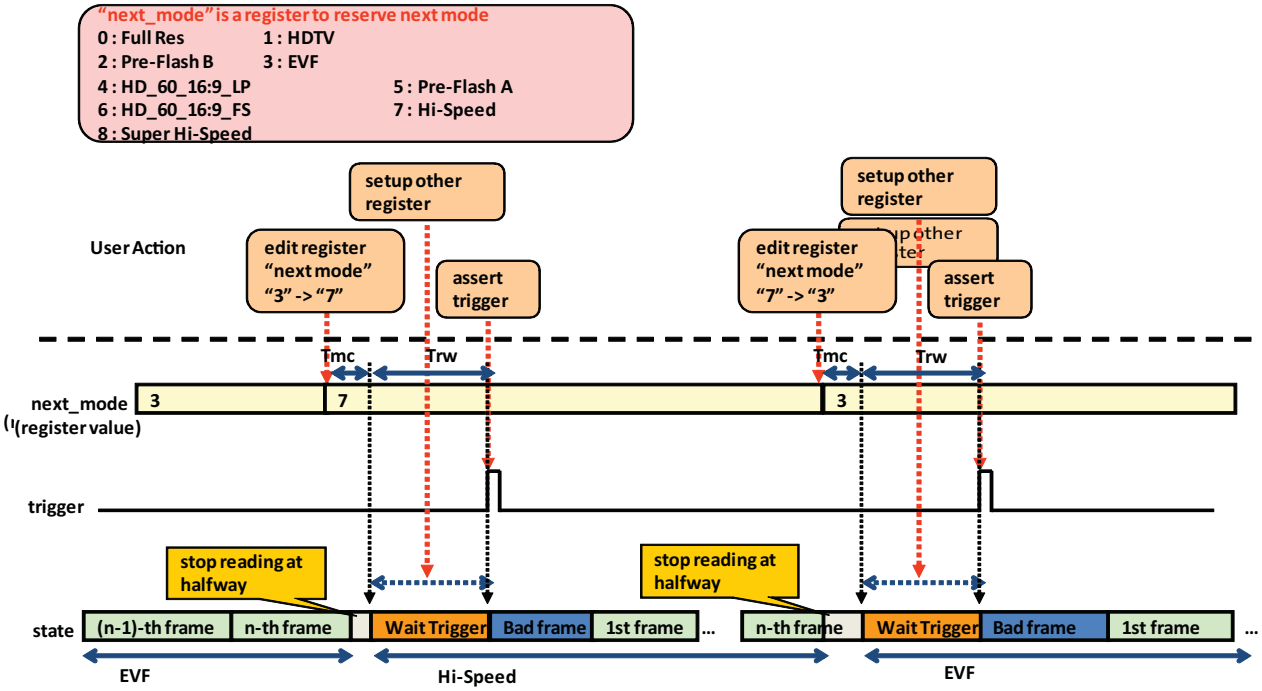
Figure 38: Mode Change Sequence from EVF to Full Resolution to EVF



Notes:
1. Tmc ≥ 200 µs at EXTCLK = 48 MHz (during this period, additional register read/write must be prohibited)
2. Trw ≥ 0 µs (Trw can be 0 µs when additional register write and its reflection to next frame is not needed.)
3. All registers can be written to any time except Tmc and 300µs from a frame end at EXTCLK = 48 MHz as described in "Sensor Control Register Update Timing" on page 71.

Mode Change Sequence (Example: EVF to Hi-Speed to EVF)

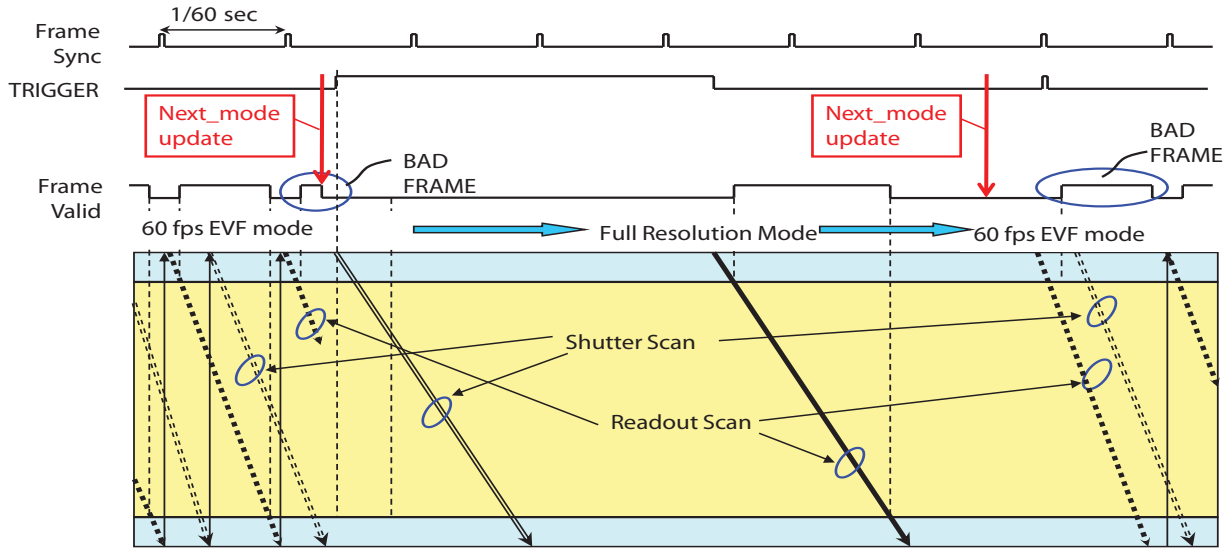
Figure 39: Mode Change Sequence from EVF to Hi-Speed to EVF



Notes:
1. Tmc ≥ 200 µs at EXTCLK = 48 MHz (during this period, additional register read/write must be prohibited)
2. Trw ≥ 0 µs (Trw can be 0 µs when additional register write and its reflection to next frame is not needed.)
3. All registers can be written to any time except Tmc and 300µs from a frame end at EXTCLK = 48 MHz as described in "Sensor Control Register Update Timing" on page 71.

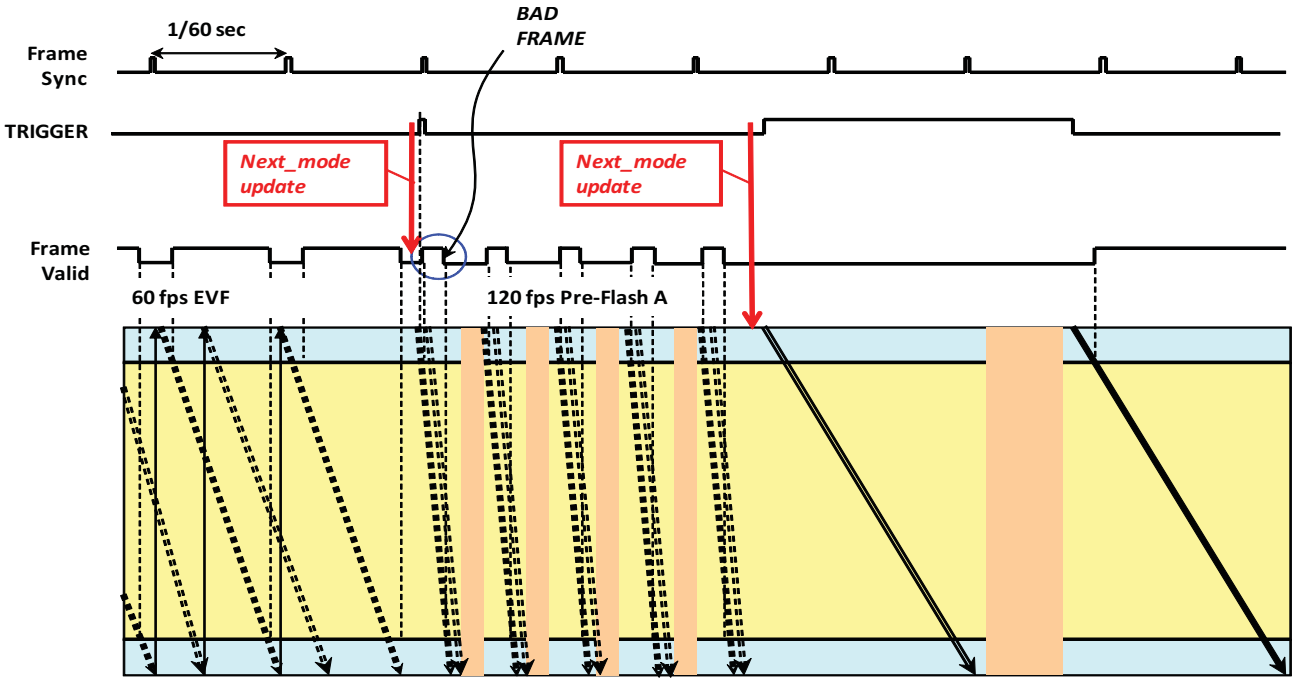
Mode Change Example - From EVF Mode to Full Resolution Mode

Figure 40: Mode Change Sequence and Internal Operation, from EVF to Full Resolution



Mode Change Example - From EVF Mode to Full Resolution Mode via Pre-Flash A Mode

Figure 41: Mode Change Sequence and Internal Operation, from EVF to Full Resolution via Pre-Flash A



Consecutive Full Resolution Mode

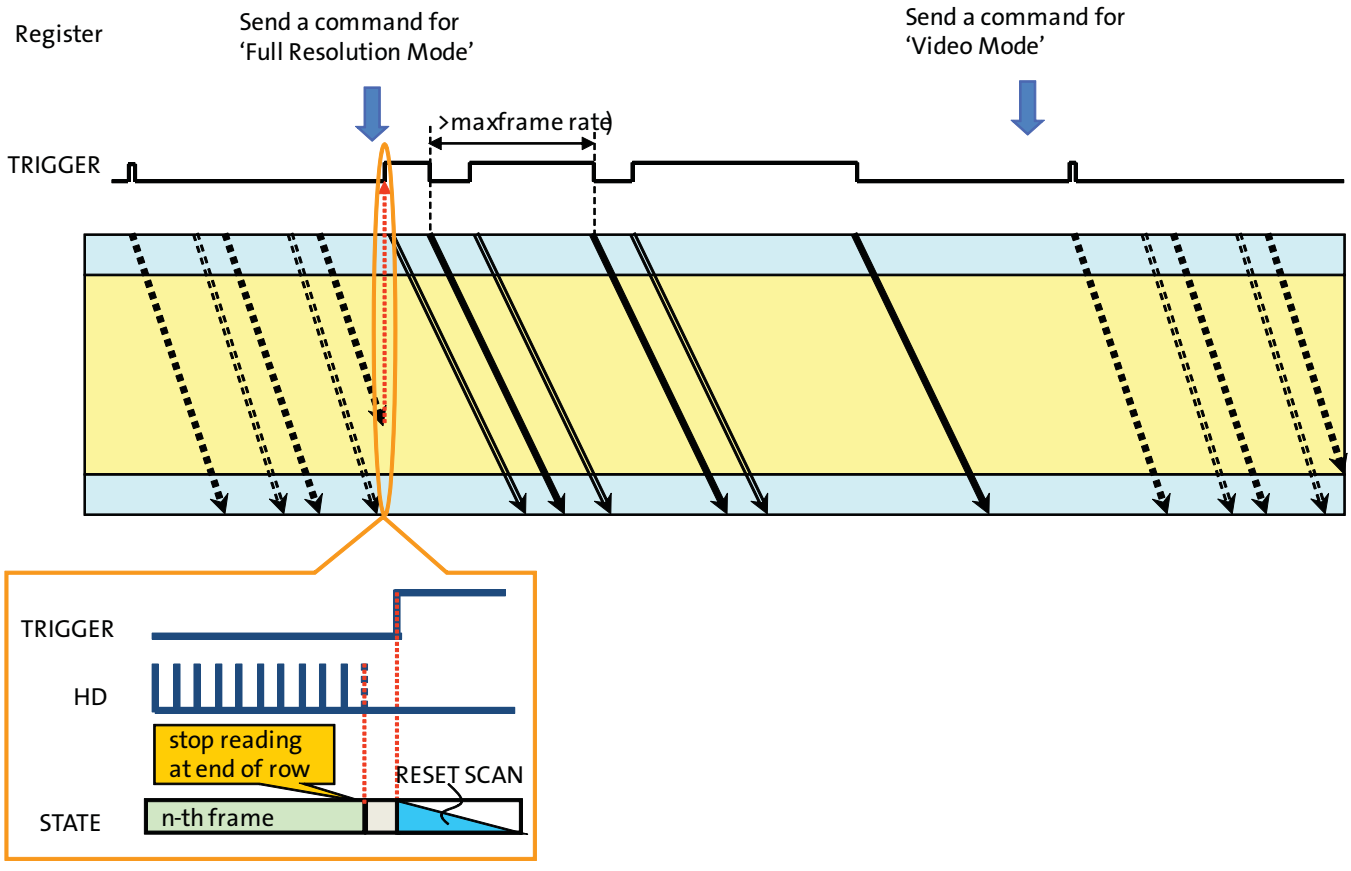
Features

- Supports the consecutive full resolution imaging at the maximum frame rate (60 fps with full resolution) as long as the integration time is shorter than the frame period
- Exposure time can be changed in an individual frame
- No bad frames appear in any integration time changes
- Simple control by TRIGGER input only
- No limitations on the number of consecutive frames

TRIGGER Control for Consecutive Full Resolution Imaging

- The command to change operation mode to a full resolution image capturing is sent and the video mode is stopped at the current row end, the sensor is getting into the 'waiting TRIGGER' status.
- Integration (Shutter scan) starts when TRIGGER rising edge is detected. Internal HD will also be restarted with a latency of 26-27 clocks following the TRIGGER rise. Then the image data readout starts when TRIGGER falling edge is detected and latched by the internal HD pulse (See “TRIGGER” on page 20).
- Once Read scan starts, the sensor gets into the waiting state to latch the next TRIGGER rise.
- Until the read scan is completed, the next TRIGGER falling edge (read start) cannot be accepted.

Figure 42: Consecutive Full Resolution Mode



Seamless Frame Rate / Integration Time Change

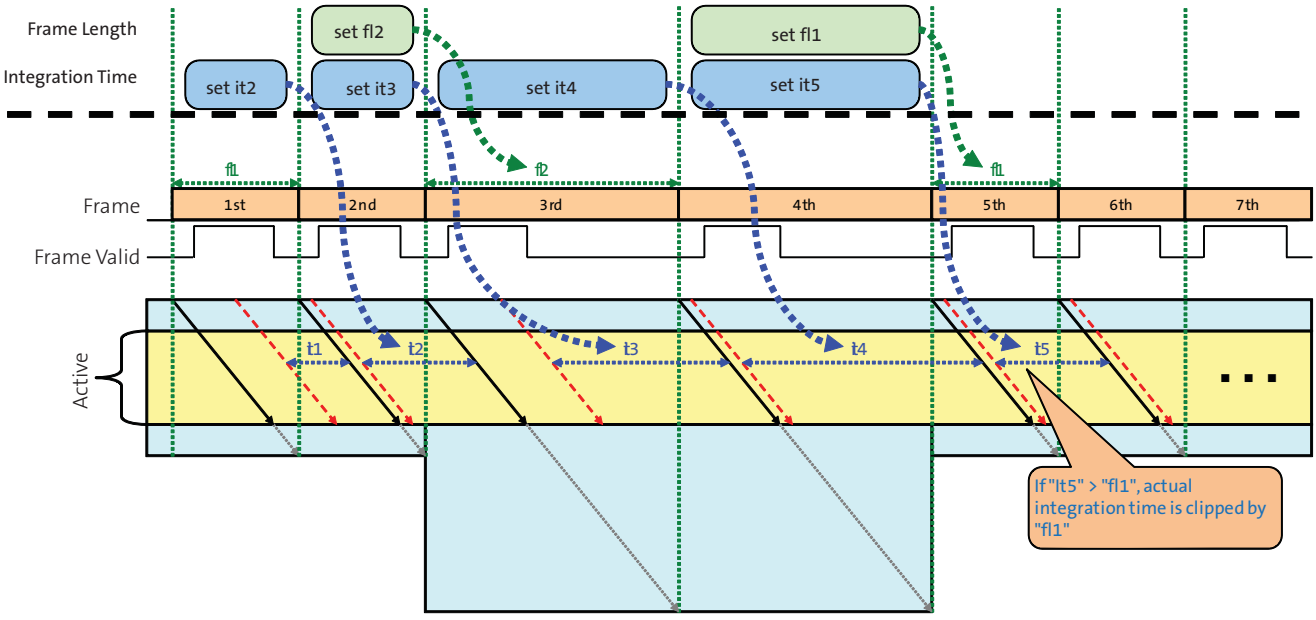
Features

- The video frame rate varies between 60 fps and 30 fps as a special feature.
- Seamless frame rate change available.
- This operation is suitable for the video modes where the AR1011HS is operating as a master device.
- No extra offset time is required when the frame rate changes. Therefore, when the frame rate is changed, such as 120 fps to 60 fps to 120 fps, Vertical Sync timing will be back to the original timing of the previous 120 fps operation.

Control

- Both 'Coarse_integration_time' and 'Frame_length_lines' registers are updated within a frame for seamless frame rate change.
- If 'Coarse_integration_time' is set larger than 'Frame line length', the integration time is clipped at the same value of 'Frame line length'.
- A new frame rate or new integration time will be reflected from the second frame counting from the frame when the registers are initially set.

Figure 43: Seamless Frame Rate / Integration Time Change

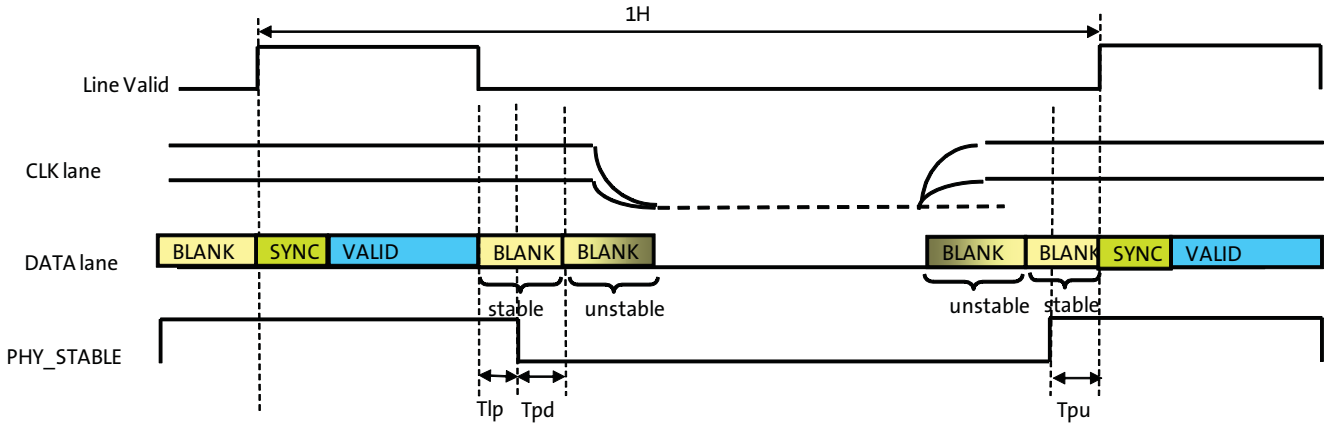


Power Save

HiSPi™ CLK/DATA lanes can be powered down during H-blanking in HDTV, HD_60_16:9_LP, and HD_60_16:9_FS, EVF, Pre-Flash A, and Pre-Flash B modes when power save mode is enabled. HiSPi clock is kept for at least 22 EXTCLK after LV turning OFF, and activated 5 EXTCLK earlier than LV turning ON. Horizontal blanking in Full Resolution, Hi-Speed, and Super Hi-Speed modes is too short for the power save control sequence so that selecting power save control does not affect any operation in these modes.

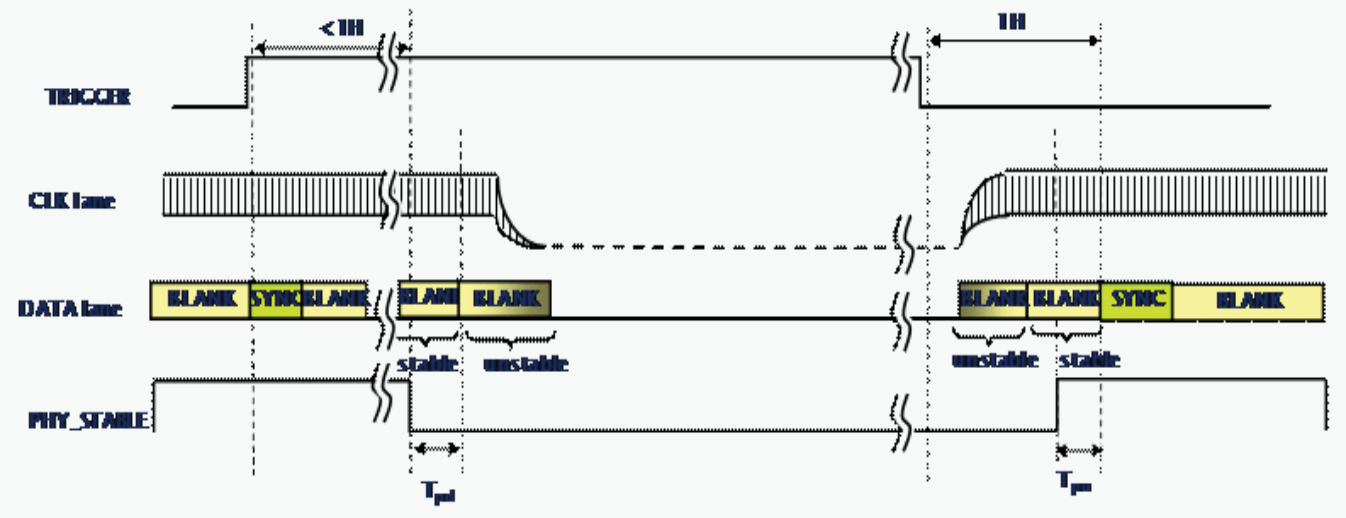
HiSPi™ CLK/DATA lanes are powered down during long integration when power save mode is enabled in Full Resolution mode. This feature is valid only in Full Resolution mode.

Figure 44: Power Save in HDTV, HD_60_16:9_LP, and HD_60_16:9_FS mode, EVF, Pre-Flash A, and Pre-Flash B Modes



Notes:
1. Tpd ≥ 5 EXTCLK duration
2. Tpu ≥ 5 EXTCLK duration
3. Tlp ≥ 17 EXTCLK duration

Figure 45: Power Save in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV Modes



Notes:
1. Tpd ≥ 5 EXTCLK duration
2. Tpu ≥ 5 EXTCLK duration

Power save capability is selectable by register. See “Power Save Control” on page 77.

Note: Power save is not applicable when TRIGGER is asserted HIGH while the previous frame is read out. In this case, the frame is operated without power saving.

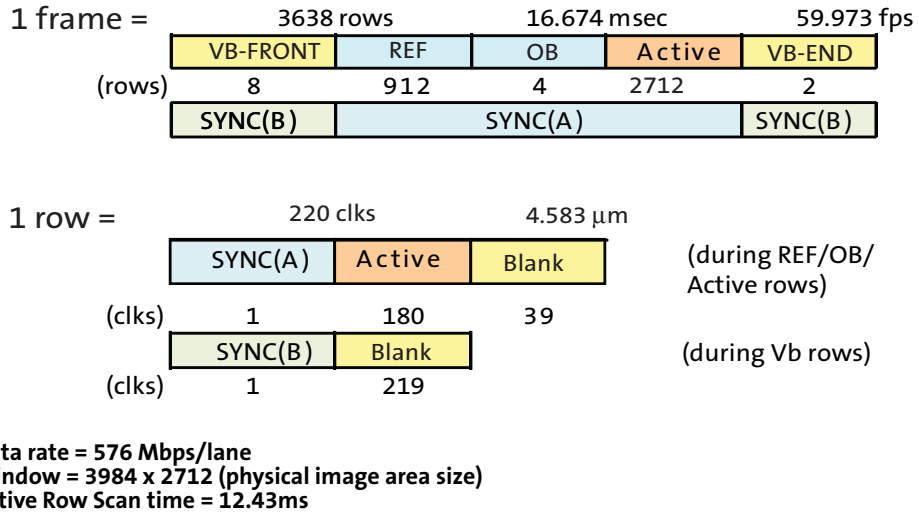
Bad Frame Readout

The first frame in the video modes is always a bad frame. The bad frame can be masked. See the section “Mask Bad Frame” on page 77.

Full Resolution Mode Operation Timing

- External frame sync with TRIGGER
- Full resolution readout
- 48 MHz, Frame readout time (Active area) 596640 clk, 1/80.4505 sec = 12.43 msec
- 59.94 fps operation with a period of TRIGGER fall edge of 3640 rows

Figure 46: Full Resolution Mode Frame Timing



Data rate = 576 Mbps/lane
Window = 3984 x 2712 (physical image area size)
Active Row Scan time = 12.43ms

Figure 47: HD_120_16:9_SLV Mode Frame Timing

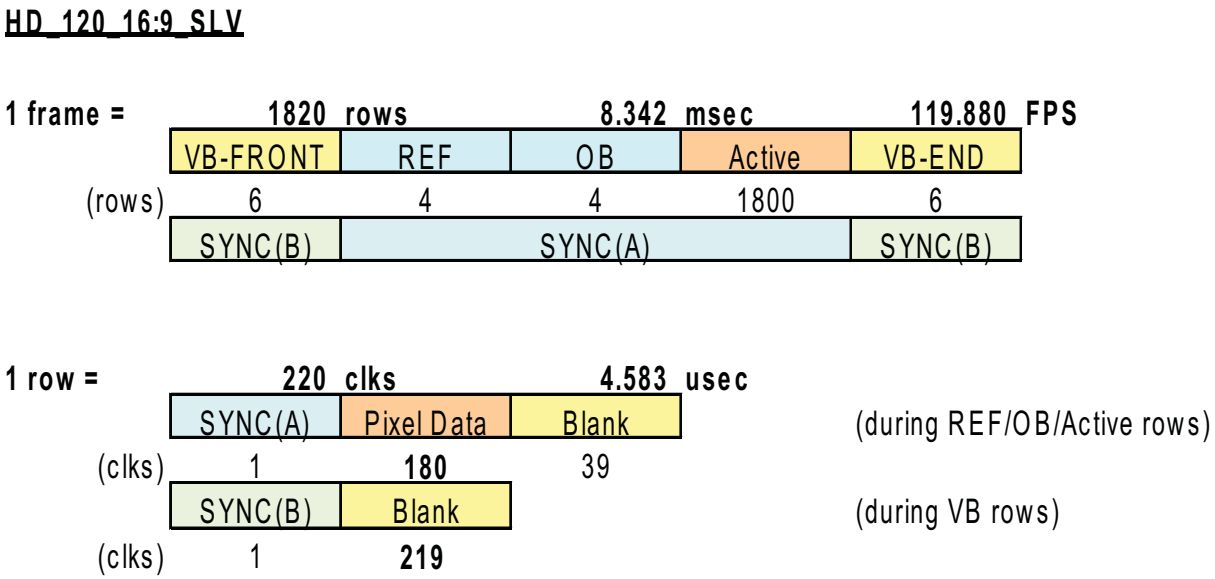
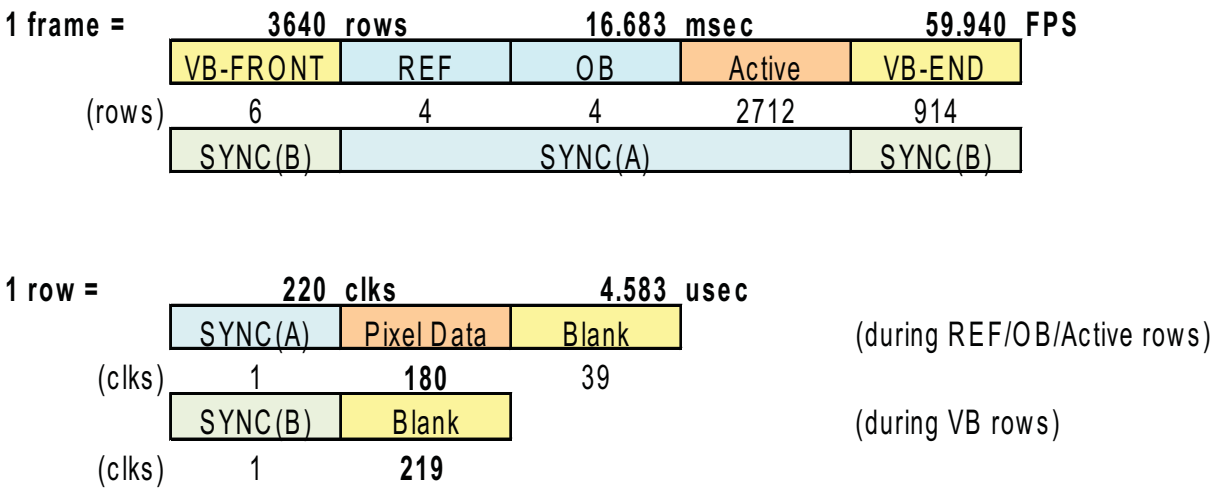


Figure 48: HD_60_3:2_SLV Mode Frame Timing

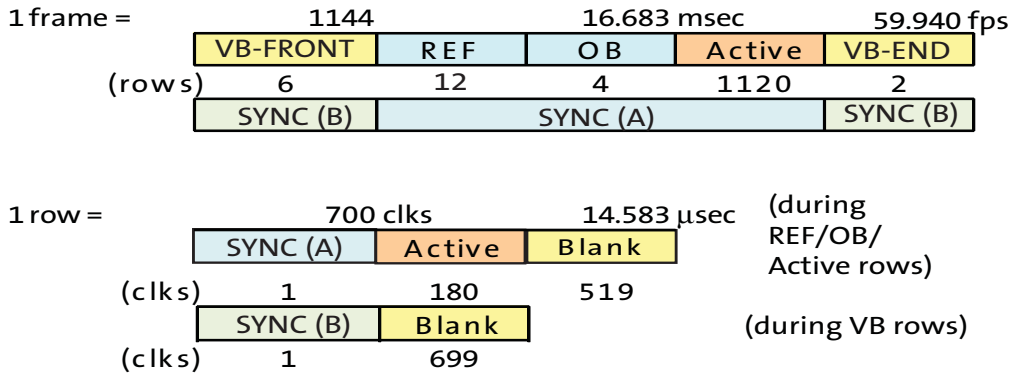


Video Modes

HDTV Mode

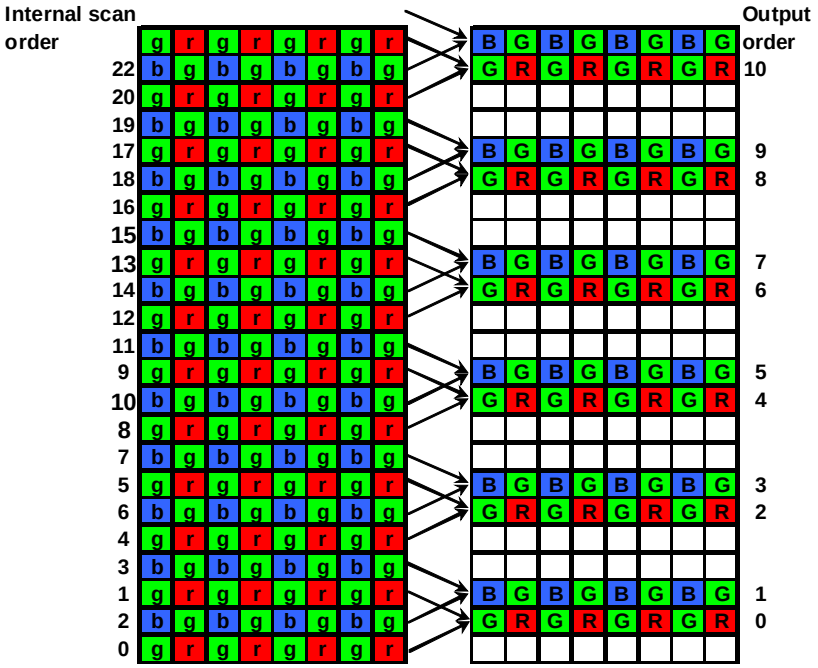
- Vertical windowing 2240 rows
- 48 MHz, 800800 clk/frame, 59.94 FPS
- Vertical: binning
- Horizontal: Full

Figure 49: HDTV Mode Frame Timing



Data rate = 576 Mbps/lane
Window = 3984 x 2240 (physical image area size)
Scan time = 16.33 ms

Figure 50: HDTV Mode Subresolution Scheme

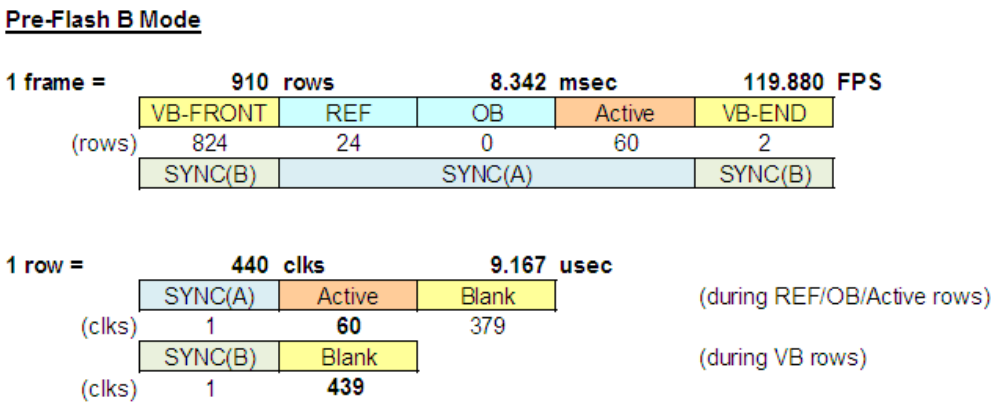


Capital G, R, B show corresponding color pixel positions resulting from the subresolution operation.

Pre-Flash B Mode

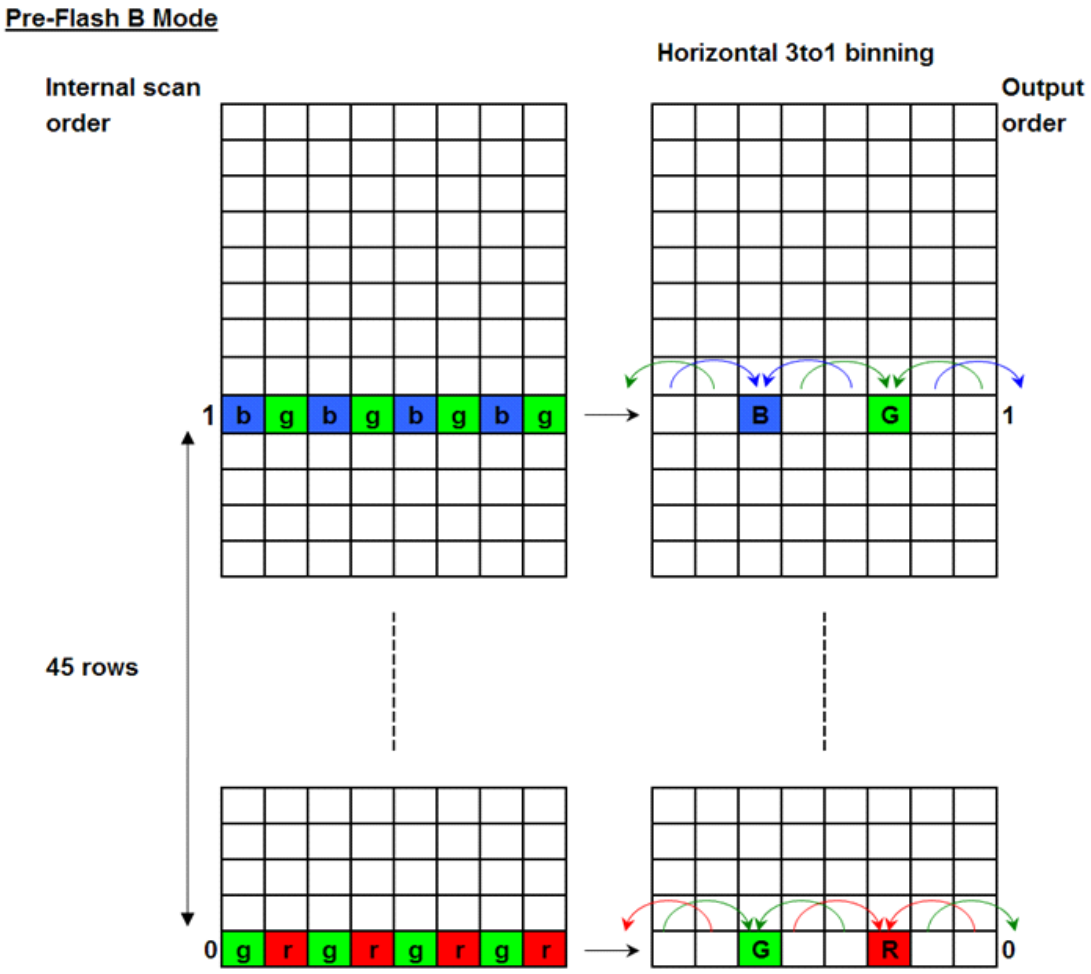
- Scan whole image area
- 48 MHz, 400400 clk/frame, 119.88 fps
- Vertical: 1/45 skipping
- Horizontal: binning

Figure 51: Pre-Flash B Mode Frame Timing



Data rate = 576 Mbps/lane
Window = 3984 x 2656 (physical image area size)
Scan time =0.55 ms

Figure 52: Pre-Flash B Mode Subresolution Scheme



EVF Mode

- Scan whole image area
- 48 MHz, 800800 clk/frame, 59.94 fps
- Vertical: 2/3 skipping
- Horizontal: Full

Figure 53: EVF Mode Frame Timing

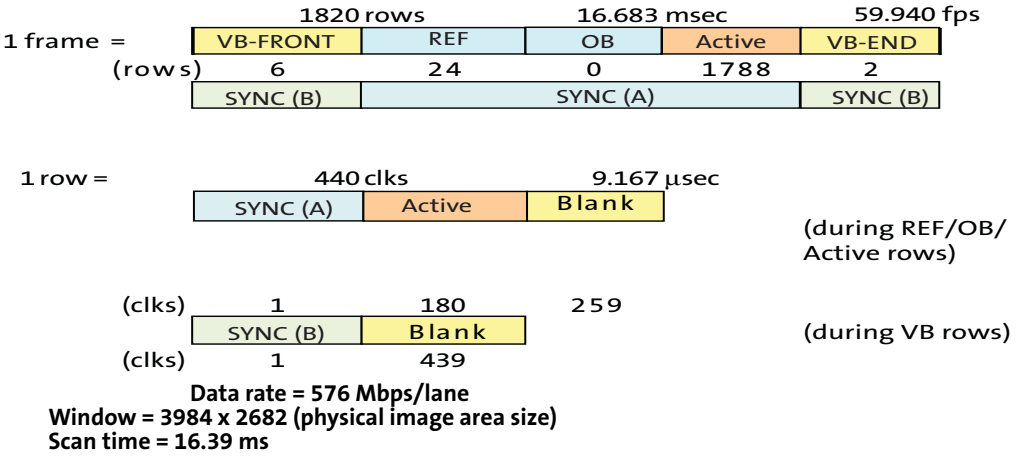
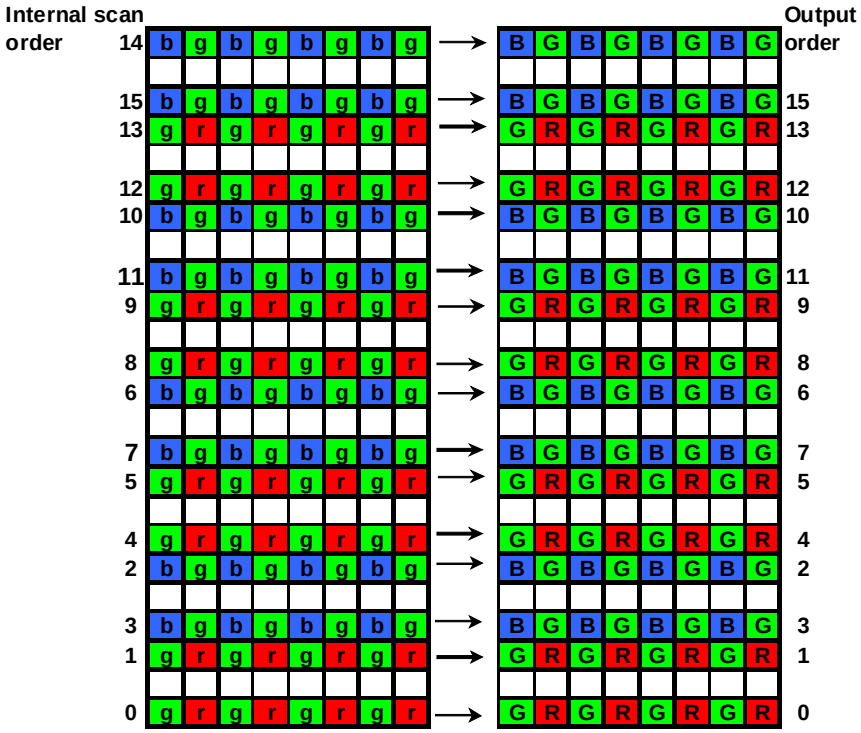


Figure 54: EVF Mode Subresolution Scheme

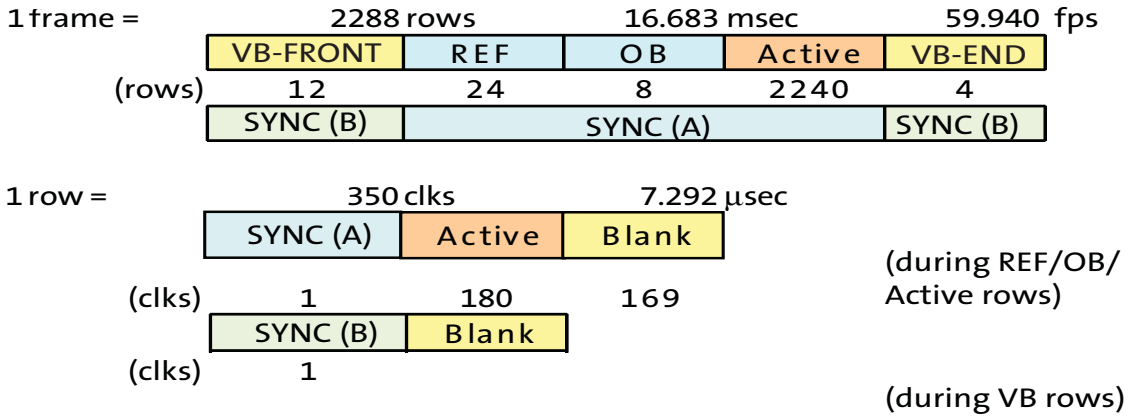


Capital G, R, B correspond to the color pixel positions resulting from the operation. Because there is no binning or skipping, GBR positions are identical with that of the physical pixel.

HD_60_16:9_LP Mode

- Vertical windowing by 2240 rows
- 48 MHz, 800800 clk/frame, 59.940 fps

Figure 55: HD_60_16:9_LP Mode Frame Timing



Data rate = 576 Mbps/lane
Window = 3984 x 2240 (physical image area size)
Scan time = 16.33 ms

Pre-Flash A Mode

- Scan whole image area
- 48 MHz, 400400 clk/frame, 119.88 fps
- Vertical: 1/15 skipping
- Horizontal: binning

Figure 56: Pre-Flash A Mode Frame Timing

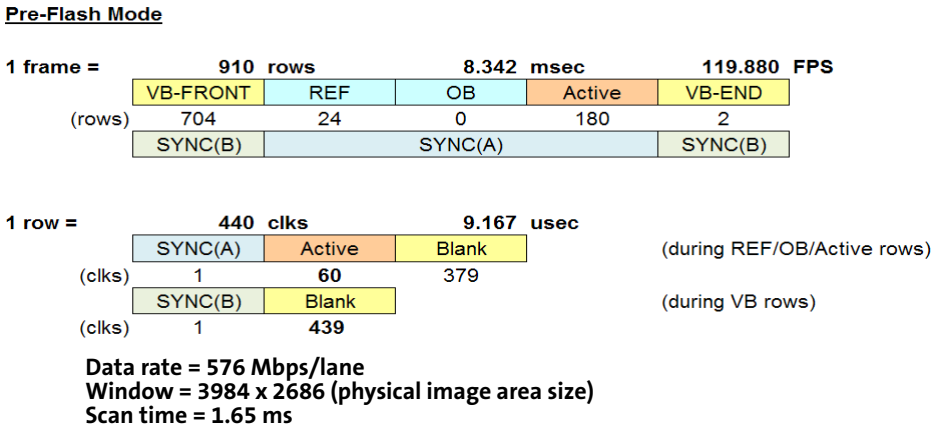
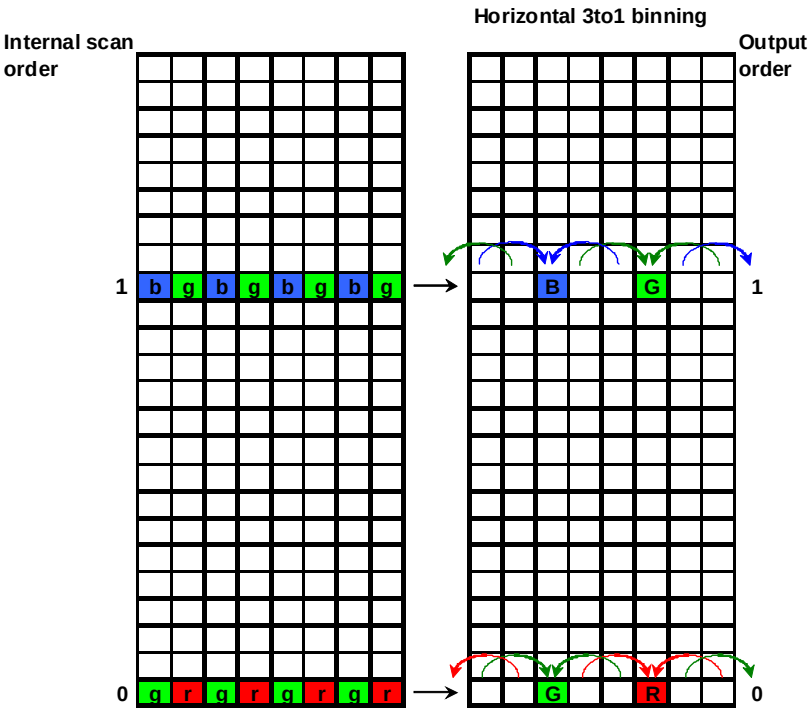


Figure 57: Pre-Flash A Mode Subresolution Scheme

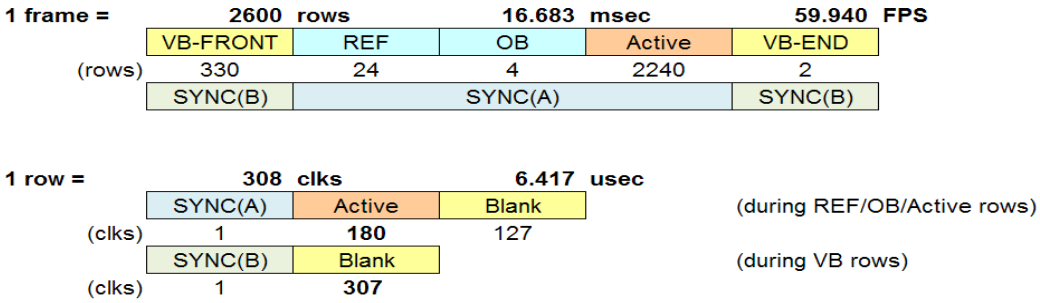


Capital G, R, B correspond to the color pixel positions resulting from the operation.

HD_60_16:9_FS Mode

- Vertical windowing by 2240 rows
- 48 MHz, 800800 clk/frame, 59.94 fps

Figure 58: HD_60_16:9_FS Mode Frame Timing

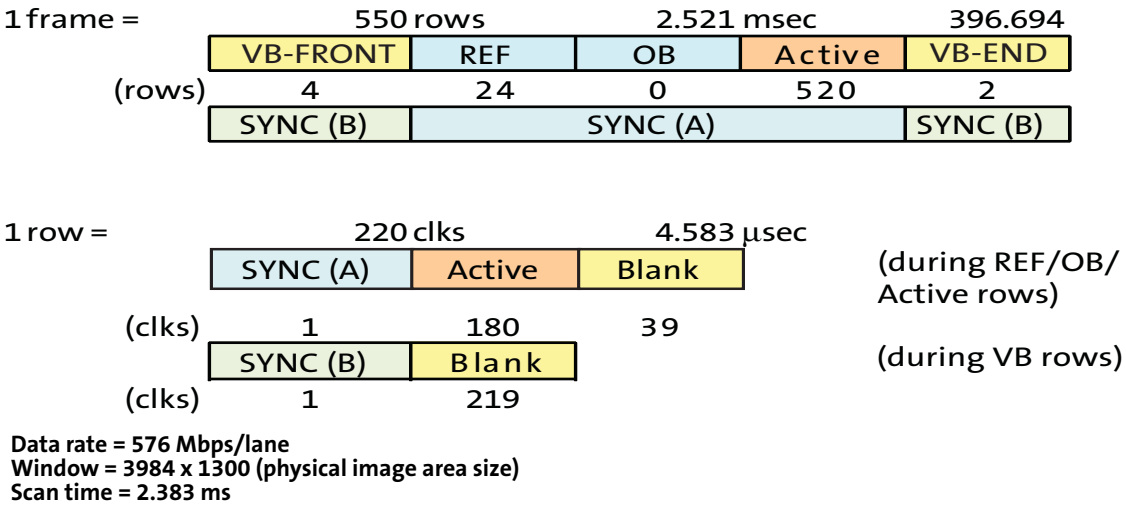


Data rate = 576 Mbps/lane
Window = 3984 x 2240 (physical image area size)
Scan time = 14.37 ms

Hi-Speed Mode

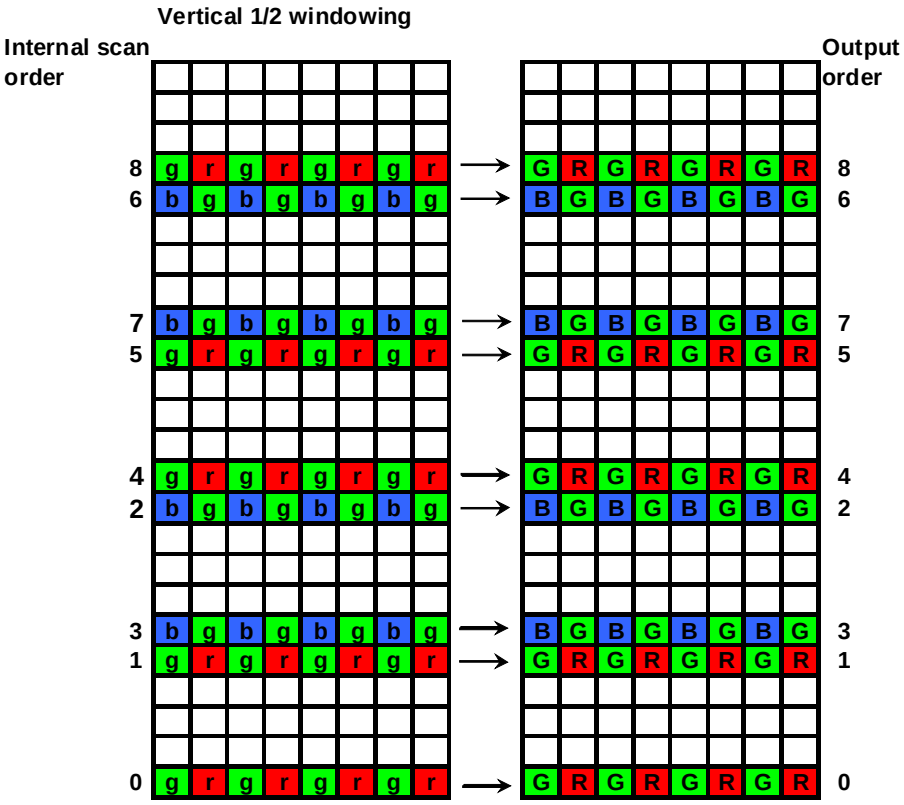
- 1/2 Vertical windowing
- 48 MHz, 121000 clk/frame, 396.69 fps
- Vertical: 2/5 skipping
- Horizontal: Full

Figure 59: Hi-Speed Mode Frame Timing



Data rate = 576 Mbps/lane
Window = 3984 x 1300 (physical image area size)
Scan time = 2.383 ms

Figure 60: Hi-Speed Video Mode Subresolution Scheme



Capital G, R, B correspond to the color pixel positions resulting from the operation. Because there is no binning or skipping, GBR positions are identical to that of the physical pixel.

Super Hi-Speed Mode

- 1/4 vertical windowing
- 48 MHz, 40040 clk/frame, 1198.80 fps
- Vertical: 1/5 skipping
- Horizontal: Full

Figure 61: Super Hi-Speed Mode Frame Timing

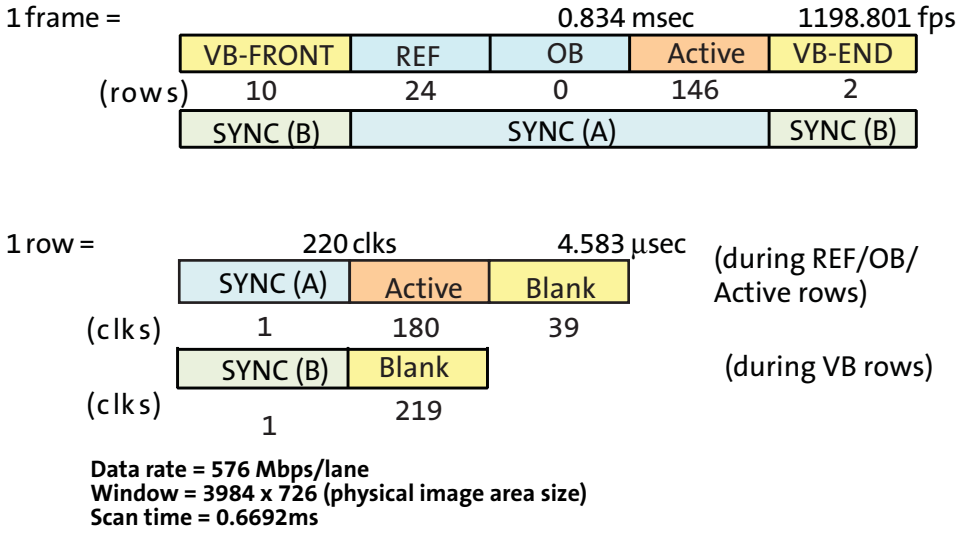
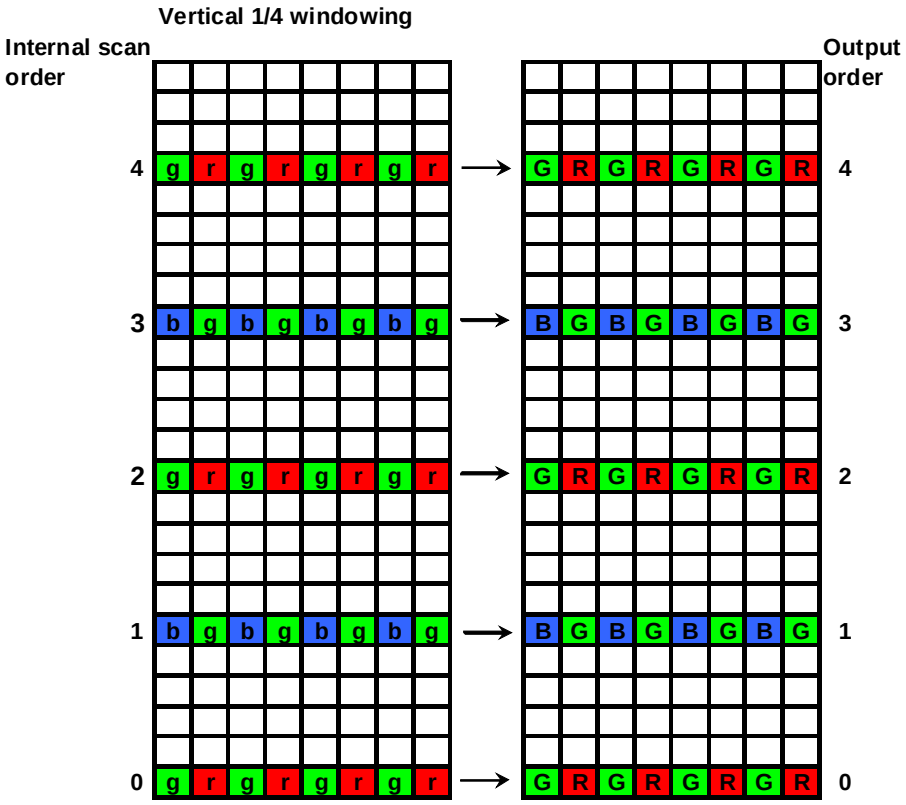


Figure 62: Super Hi-Speed Video Mode Subresolution Scheme



Capital G, R, B correspond to the color pixel positions resulting from the operation. Because there is no binning or skipping, GBR positions are identical to that of the physical pixel.

Frame Structure

The first frame after power on does not have the sync code for blanking.

SYNC(B) does not appear during power save of integration in Full Resolution Mode.

Figure 63: Frame Structure in a Sequence Video to Full Resolution to Video

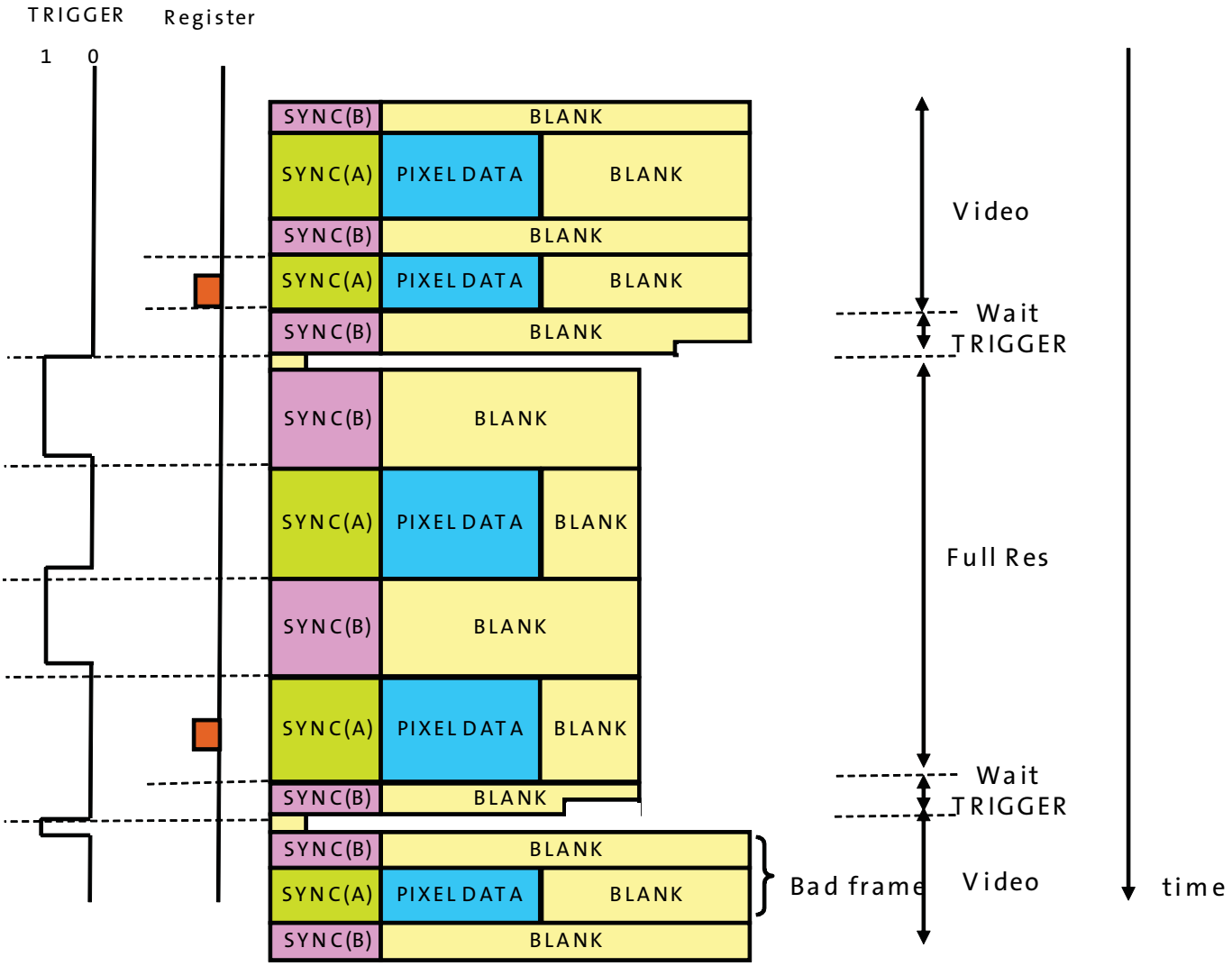
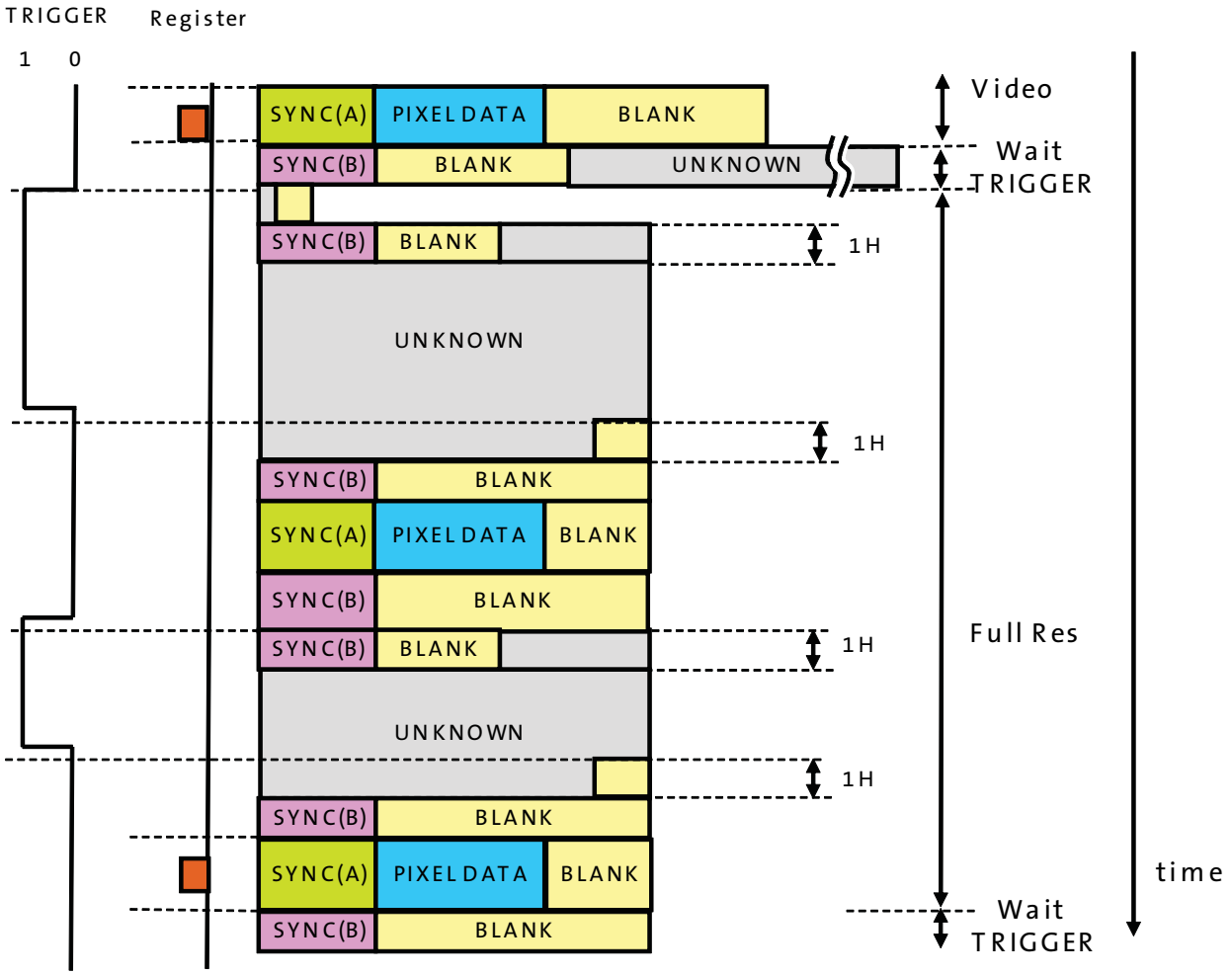


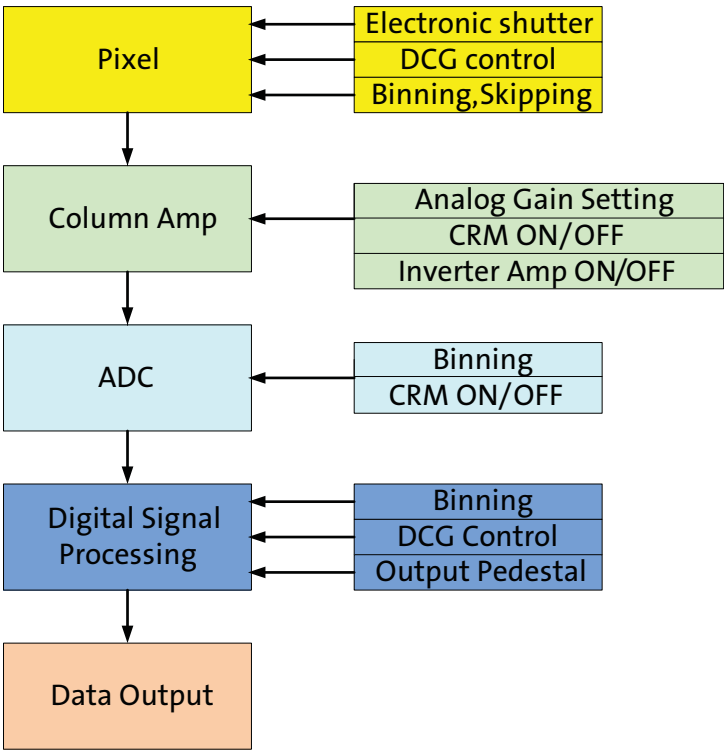
Figure 64: Frame Structure in Full Resolution Mode with Power Save



Sensor Control

Sensor Control Block Diagram and Pulses

Figure 65: Sensor Control Block Diagram and Pulse



Sensor Control Register Update Timing

Gain Update Timing

Figure 66 and Figure 67 show Gain and all Frame Sync update registers update timing.

Any other update timing registers are not affected. During 300ms from a frame end at EXTCLK = 48 MHz, all registers read/write must be prohibited.

Figure 66: Gain Update Timing in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV Modes

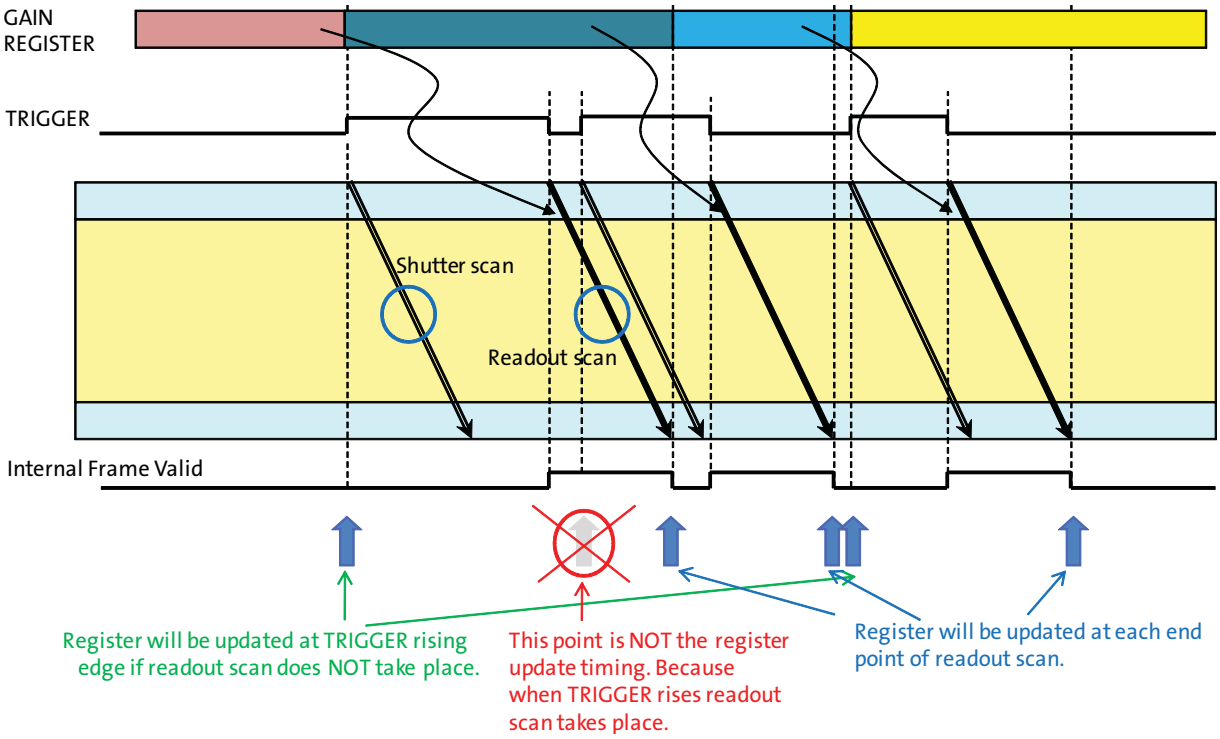
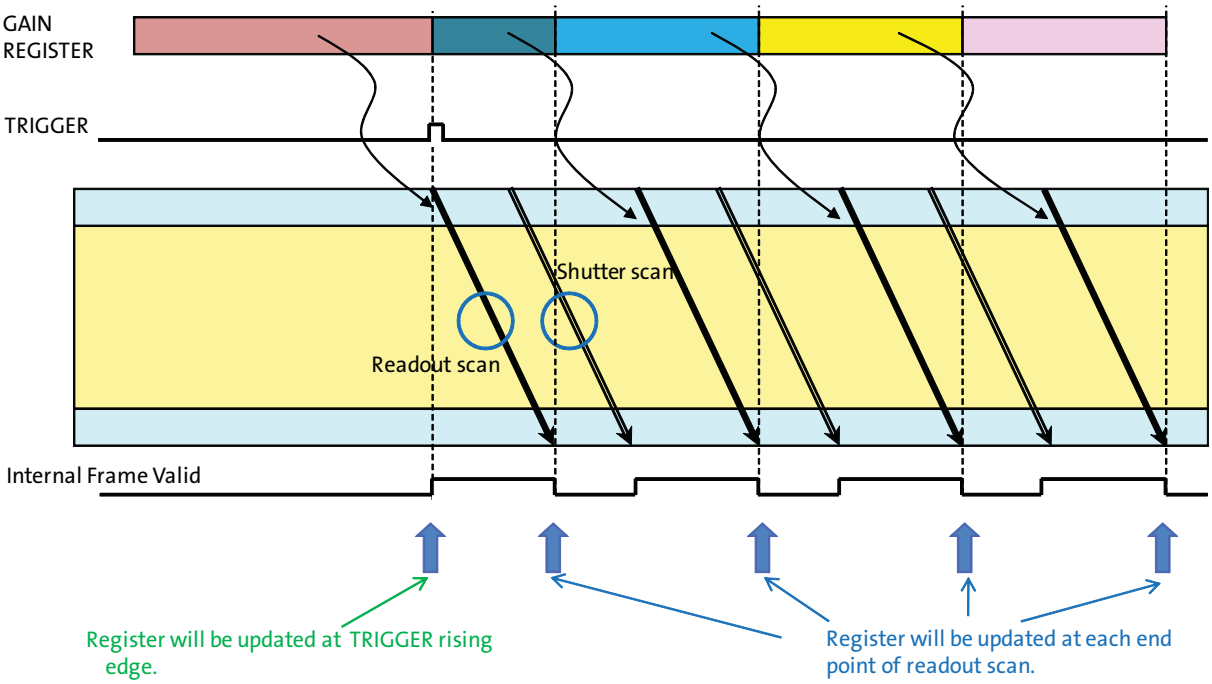


Figure 67: Gain Update Timing in Video Modes



Pixel Sensitivity Control

Integration Time Control

The integration time in video mode is programmed by the electronic shutter control value in the register. Exposure time is set by:

Min(Coarse_integration_time or Frame_length_lines - n)
x *row time (of current operating mode)* + t_{OFFSET}

Note: For *n*, see Table 26, "Minimum Coarse_integration_time and Integration Time In Video Modes," on page 74

On the other hand, integration time in Full resolution mode is determined by a pulse width of the external TRIGGER input.

Table 25: Electrical Shutter Control Register Setting

Name	Bit	Default	Description
Coarse_integration_time	15:0	0x3E7	The exposure time, the time between when the rolling shutter resets a row and that row is read out, in rows.
Frame_length_lines	15:0	0x71C	The number of lines per frame including all output data such as the dark rows, vertical blanks, and so on.

Figure 68: Integration Time Update Timing in Video Modes

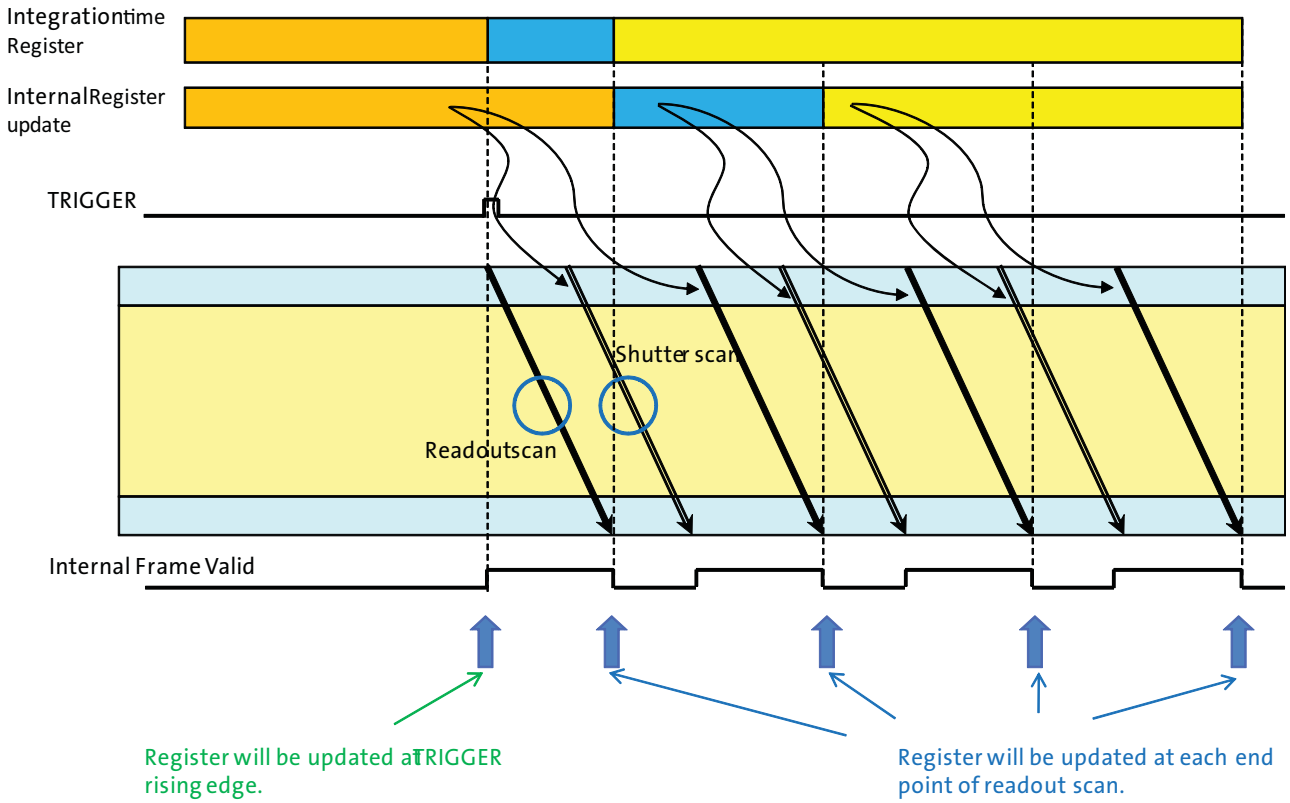


Table 26: Minimum Coarse_integration_time and Integration Time In Video Modes

Mode	Minimum coarse_integration_time	Maximum coarse_integration_time	^{t}OFFSET	Minimum Integration Time
	Register Value	Register Value	Time (µs)	Time (µs)
HDTV	3	frame_length_lines – 2	~0.2	43.95
Pre-flash B	5	frame_length_lines – 3	~0.2	46.03
EVF	5	frame_length_lines – 3	~0.2	46.03
HD_60_16:9_LP	5	frame_length_lines – 3	~0.2	36.66
Pre-Flash A	5	frame_length_lines – 3	~0.2	46.03
HD60_16:9_FS	5	frame_length_lines – 3	~0.2	32.28
Hi-Speed	5	frame_length_lines – 3	~0.2	23.12
Super Hi-Speed	5	frame_length_lines – 3	~0.2	23.12

Dual Conversion Gain (DCG) Control

Table 27: DCG Control Register Setting

Name	Bit	Default	
DCG_hi enable	0	0	0: Low CG 1: High CG
DCG_gain_code_greenR	2:0	0	0: 1x (0.25x step) 7: 2.75x
DCG_gain_code_red	2:0	0	0: 1x (0.25x step) 7: 2.75x
DCG_gain_code_blue	2:0	0	0: 1x (0.25x step) 7: 2.75x
DCG_gain_code_greenB	2:0	0	0: 1x (0.25x step) 7: 2.75x

The default is the low gain setting.

Analog Gain Control

Table 28: Analog Gain Control Register Setting

Name	Bit	Default	
Analog_gain_code_greenR	2:0	0	0: 1x 1: 2x 3: 4x 7: 8x 2, 4, 5, 6: prohibited
Analog_gain_code_red	2:0		
Analog_gain_code_blue	2:0		
Analog_gain_code_greenB	2:0		

Output Pedestal

Manual offset control is applicable when the user needs to change output pedestal levels from default values. Manual offset registers are frame sync registers and update timing of the pedestal level is identical to that of gain control registers.

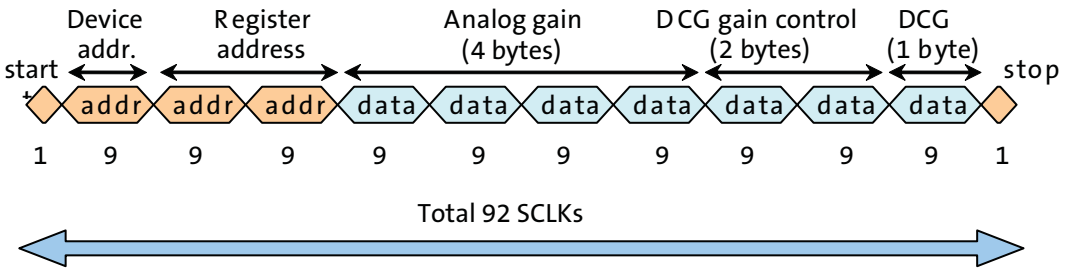
Table 29: Output Pedestal Control Register Setting

Name	Bits	Default	
Gr manual offset control	11:0	0x100	0~4095
Gb manual offset control			
R manual offset control			
B manual offset control			

Gain Change with Serial Data Chain Mode of the Two-Wire Serial I/F

Gain control registers are mapped serially. Updating all gain registers takes 92 SCLKs in sequential write mode of the two-wire serial I/F.

Figure 69: Serial Data Chain for All Gain Settings



Context Mode Control - Next Mode

When the next_mode register is updated during readout in full resolution mode, the AR1011HS goes through the frame readout, then the internal register values will immediately be overwritten with the default values defined for the corresponding mode. In rest modes, the AR1011HS stops the current operation at the end of the present row duration when the next_mode register is updated, then the internal register values will be immediately overwritten.

When internal register overwrite is completed in 200 µsec after next_mode input (at EXTCLK = 48 MHz), the AR1011HS will get into the wait TRIGGER state until TRIGGER rise input. The Next_mode register control enables a quick operating mode change; thus it is referred to as context mode change.

Table 30: Operating Mode Control Register

Name	Bit	Default	
next_mode	3:0	3	0: Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV 1: HDTV 2: Pre-Flash B 3: EVF 4: HD_60_16:9_LP 5: Pre-Flash A 6: HD_60_16:9_FS 7: Hi-Speed 8: Super Hi-Speed 9-15: Prohibited

During the wait trigger state, a user can send additional commands, such as analog gain, DCG control, and DCG setting.

Using the sequential write feature of the AR1011HS two-wire serial I/F protocol, setting up analog gain, DCG control, and DCG takes 92 SCLK duration.

The next_mode register cannot be a part of the sequential write. The next_mode register must be written by a single write.

PHY_STABLE Control

Table 31: PHY_STABLE Control Register Setting

Name	Bit	Default	
Phy_stable_control	1:0	0	0: Outputs PHY_STABLE
			1: Reserved for test
			2, 3: Output 0

Note: Phy_stable_control is asynchronous.

Power Save Control

Table 32: Power Save Control Register Setting

Name	Bit	Default	
Power_save_enable	0	1	0: Power save disable 1: Power save enable

Note: Power_save_enable is asynchronous.

Mask Bad Frame

Table 33: Mask Bad Frame Register Setting

Name	Bit	Default	
Mask_bad_frames	0	0	0: Bad frame is read out 1: Bad frame is not read out

Note: Mask_bad_frame does not affect data output for a bad frame when next_mode is asserted in a video mode. When next_mode is asserted during the video mode, read-out of the frame stops immediately at the next horizontal blanking. In this case, the next frame will be a bad frame; however, data readout for the frame has already started and masking the frame is not available.

Inverter Amp Function

In the signal chain, a boost amplifier called “Inverter Amp” is implemented between the column amplifier and the column ADC. Enabling the Inverter Amp makes signal settling faster, which reduces row banding and column FPN while extra current is required. When the customer prefers to save power consumption rather than reduce the noise, the Inverter Amp can be disabled using a register setting so that the signal bypasses the Inverter Amp and the bias current in the Inverter Amp is completely stopped.

CRM Function

CRM is a special function to reduce visible column FPN and column PRNU (photo response nonuniformity). Offset variation and gain variation between column signal circuits result in column FPN and column PRNU. Enabling CRM randomizes the column FPN or PRNU by changing the connection to the column circuit row by row in a random manner, which suppresses the visual structural noise pattern.

Vtx Pulsing Function

In order to suppress the generation of blooming defects under long exposure conditions, a VTX pulsing function is implemented. The VTX pulsing function is valid for Full Resolution mode only.

When VTX pulsing is enabled, the pixel transfer gate is driven with a pulse train having a high level of intermediate voltage during long integration periods.

The periodic intermediate pulse generates an overflow drain path beneath the TX gate (from the photodiode to the floating diffusion inside a pixel), thus preventing the excess charge from overflowing to the adjacent pixels. In this way, the blooming defect can be suppressed.

The VTX pulsing operation begins when the shutter scan is completed, then continues until TRIGGER fall assertion, namely readout scan start. Enabling the VTX pulse register doesn't affect sensor operation when the integration time is shorter than the shutter scan time of 1/60sec, or in any video mode.

The VTX pulsing operation begins when the shutter scan is completed then continues until TRIGGER fall assertion, namely readout scan start. Enabling the VTX pulse register doesn't affect sensor operation when the integration time is shorter than the shutter scan time of 1/60sec, or in any video mode.

Two-Wire Serial Register Interface

The two-wire serial interface bus enables the read/write access to the status and control registers in the sensor.

The interface protocol acts as either of master or slave where the master can control more than one slave device. The sensor two-wire interface acts as a slave device as well. When the sensor is in a slave mode, the outside master device generates a serial clock (SCLK) that is an input to the sensor and is used to synchronize the sensor to the master device for the data transfers. The data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW- the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocol described in this chapter allows the slave device to drive SCLK LOW; the sensor uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

- A (repeated) start condition
- A slave address/data direction byte
- An(a no-) acknowledge bit
- A message byte
- A stop condition

The bus is idle when both SCLK and SDATA are HIGH. The bus control is initiated by a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition, and this is known as a 'repeated start' or 'restart' condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a write, and a "1" indicates a read. The slave addresses used by the sensor are 0x20 (write address) and 0x21 (read address).

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical read or write sequence begins when a master generates a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

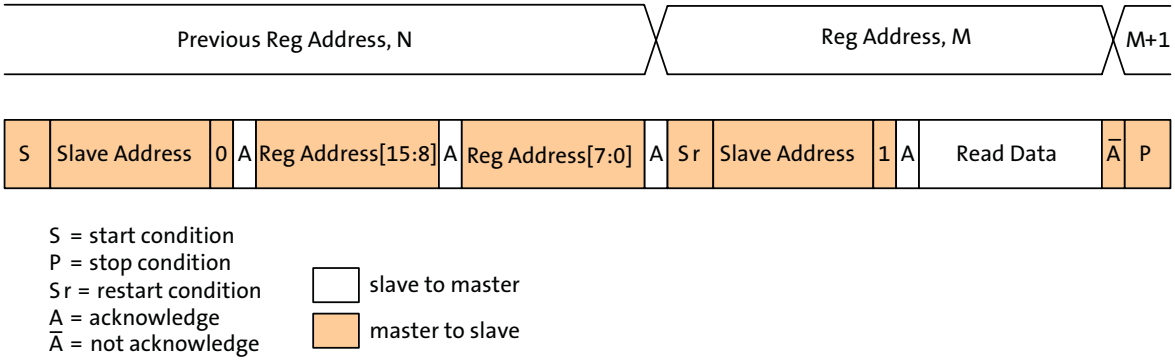
If the request is a write, the master then transfers the 16-bit register address to which a write should take place. This transfer takes place as a two 8-bit sequence and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. After the 8-bit code has been transferred, the slave internal register address is incremented automatically, so that the next 8 bits are written to the next register address. The master stops writing by generating a (re)start or stop condition.

If the request is a read, the master sends the 8-bit code to write the slave address/data direction byte and 16-bit register address, just as in the write request. The master then generates a (re)start condition and an 8-bit read slave address/data direction byte, and clocks out the register data, 8-bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single Read from Random Location

This sequence (Figure 70) starts with a dummy write to the 16-bit address that is to be used for the read. The master terminates the write by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the read by generating a no-acknowledge bit followed by a stop condition. Figure 70 shows how the internal register address maintained by the sensor is loaded and incremented as the sequence proceeds.

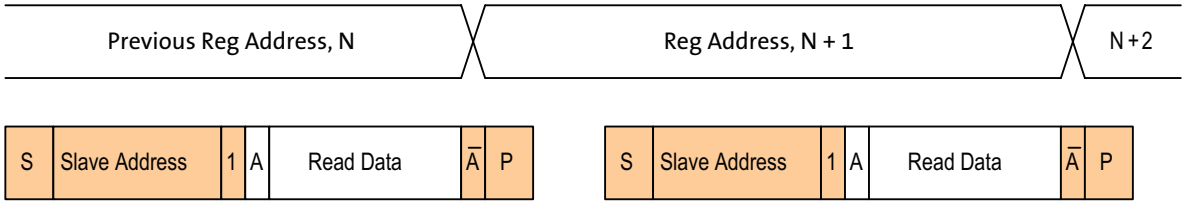
Figure 70: Single Read from Random Location



Single Read from Current Location

This sequence (Figure 71) performs a read using the current value of the sensor internal register address. The master terminates the read by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent read sequences.

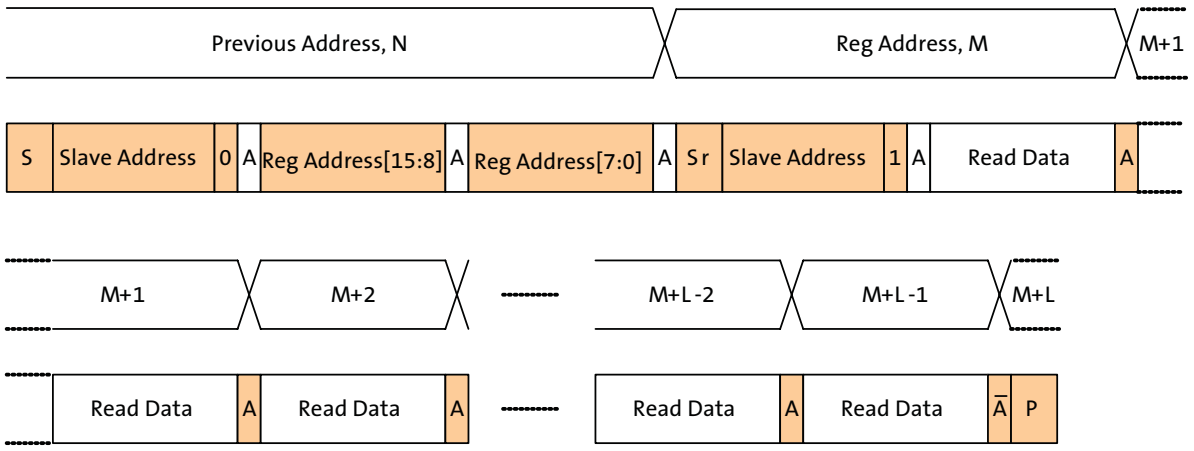
Figure 71: Single Read from Current Location



Sequential Read, Start from Random Location

This sequence (Figure 72) starts in the same way as the single read from random location. Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit, and continues to perform byte reads until L bytes are read.

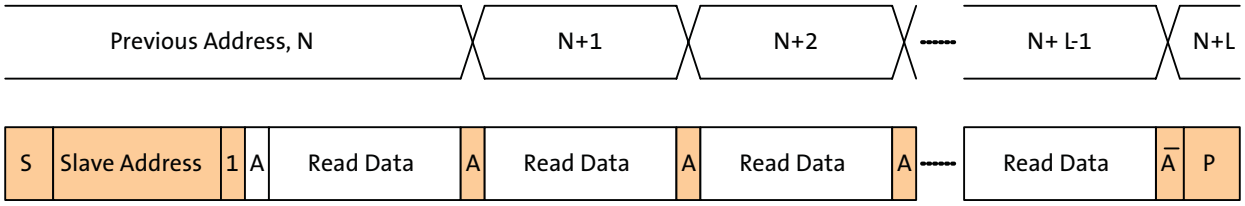
Figure 72: Sequential Read, Start from Random Location



Sequential Read, Start from Current Location

This sequence (Figure 73) starts in the same way as the single read from current location. Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit, and continues to perform byte reads until L bytes have been read.

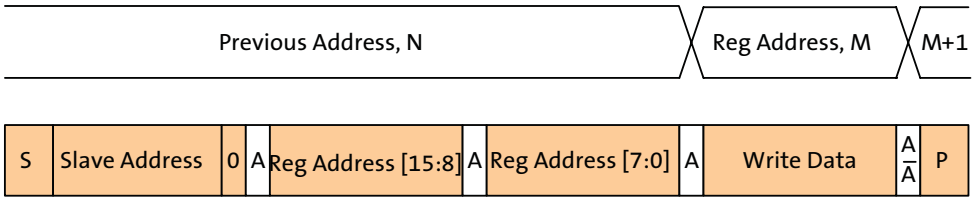
Figure 73: Sequential Read, Start from Current Location



Single Write to Random Location

This sequence (Figure 74) begins with the master generating a start condition. The slave address/data direction byte signals a write and is followed by the high then low bytes of the register address that is to be written. The master follows this with the byte of write data. The write is terminated by the master generating a stop condition.

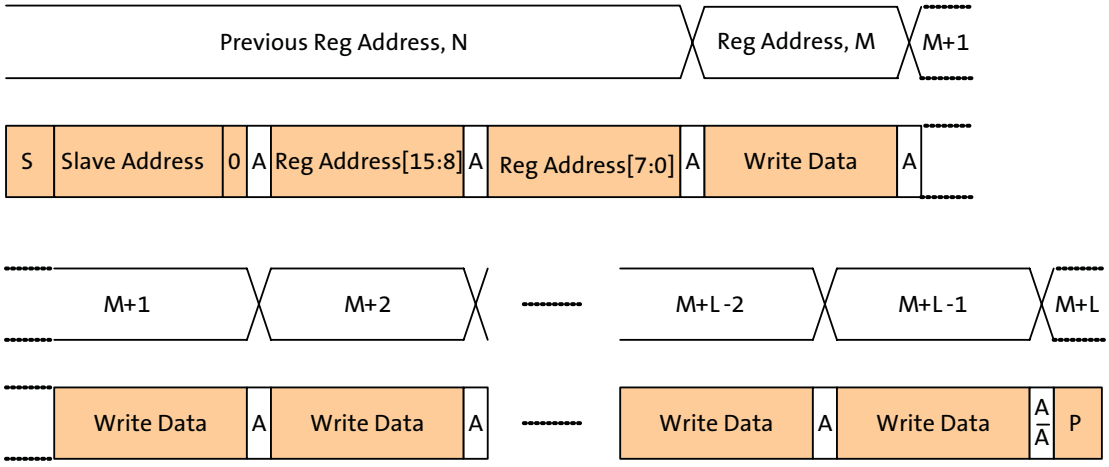
Figure 74: Single Write to Random Location



Sequential Write, Start at Random Location

This sequence (Figure 75) starts in the same way as the single write to random location (Figure 74). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit, and continues to perform byte writes until L bytes have been written. The write is terminated by the master generating a stop condition.

Figure 75: Sequential Write, Start at Random Location



Electrical Specifications

SCLK: Max 400 kHz

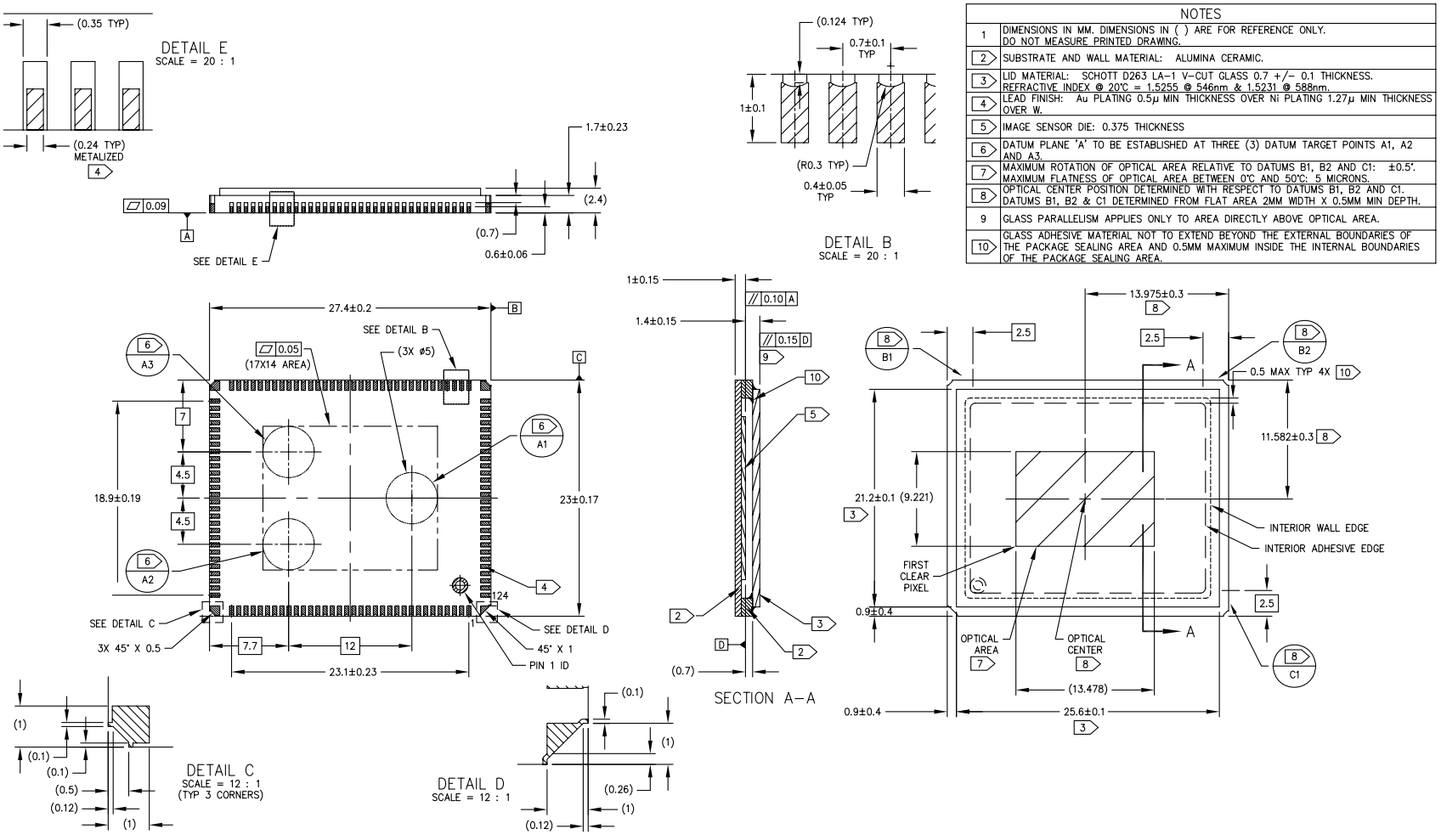
Input pull up resistance: 1.5 kΩ

Mechanical Specification

Package

The image sensor chip is assembled in 124-pin ceramic leadless chip carrier (CLCC) package as shown in Figure 76 on page 84.

Figure 76: Package Schematic

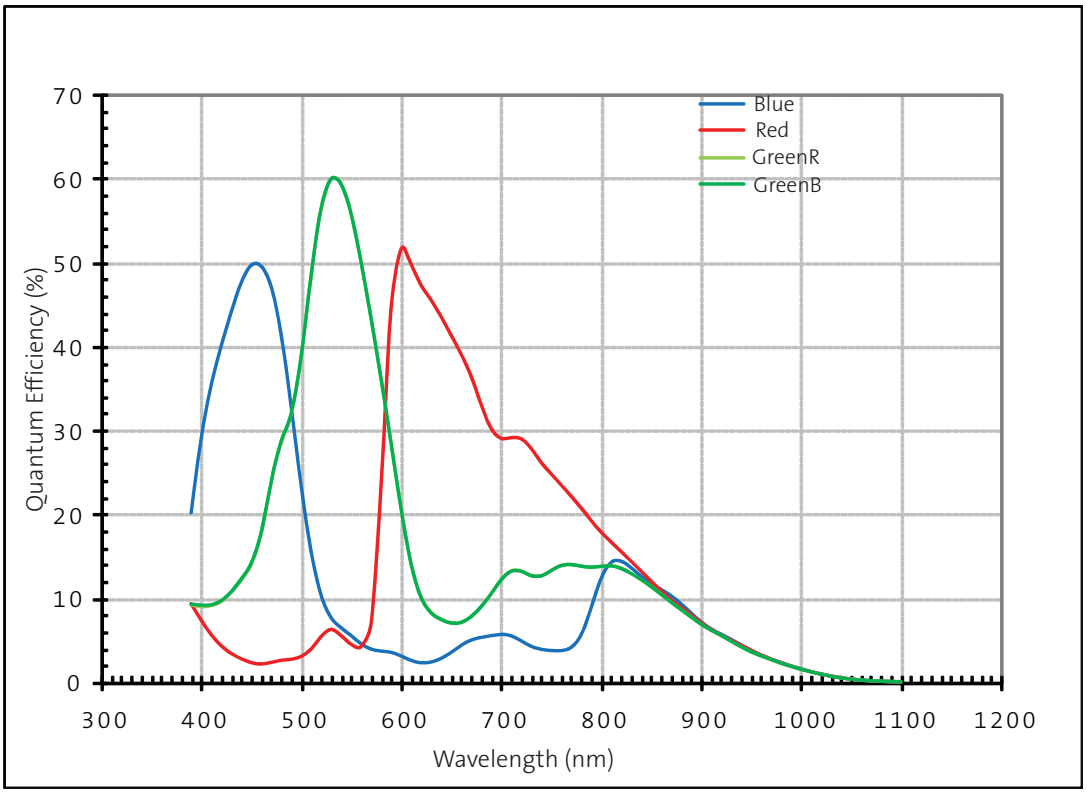


Note: Magnification of this diagram is not to scale.

1 Pixel Performance

1.1 Quantum Efficiency

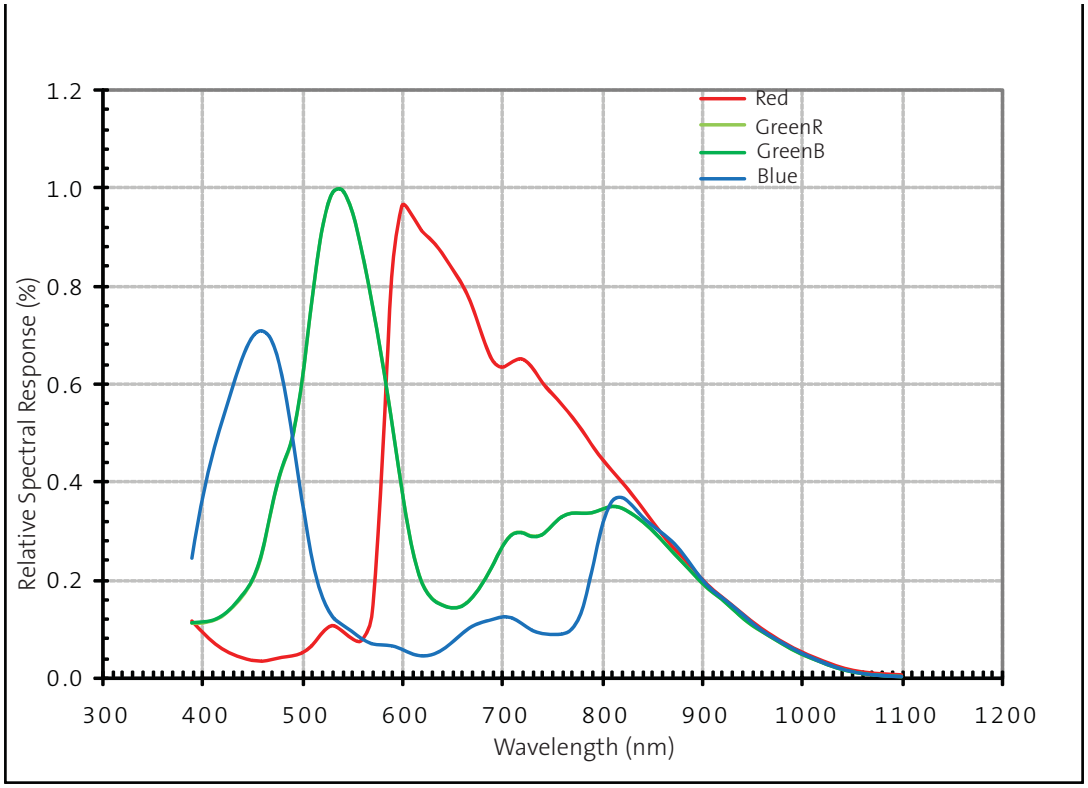
Figure 77: Quantum Efficiency



Note: This QE data was taken by wafer probing

Spectral Response

Figure 78: Relative Spectral Response



Note: This spectral response was taken by wafer probing

Revision HIstory

Rev. C 6/17/13

- Updated to Production
- Applied updated Aptina template
- Updated “Mode Transition” on page 47

Rev. B 2/4/13

- Updated “Features” on page 1
- Changed titleof Table 2 from “Key Specifications” to Table 2, “Key Performance Parameters,” on page 1 and updated
- Removed Table 3, “Key Performance Parameters” from page 3 (duplicated Table2)
- Updated Table 3, “Operating Modes,” on page 9
- Added “Block Diagram” on page 10
- Added “Signal Descriptions” on page 15
- Added “HiSPi™Output Equivalent Circuit” on page 17
- Moved Table 11, Max Power Consumption without HiSPi™ Power Save with Typical Power Supply Voltages at 30°C and Table 12, Max Power Consumption without HiSPi™ Power Save and Inverter Amp OFF with Typical Power Supply Voltages at 30°C to new section, “Power Consumption Estimate” on page 18
- Changed EVF C to EVF in Figure 12: “Power Up Sequence,” on page 23
- Added “DLL Timing Adjustment” on page 30
- Updated title of Figure 32: “Nesting Scan in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV, HD_60_16:9_LP, HD_60_16:9_FS Readout Mode,” on page 43
- Updated title of Figure 34: “Nesting Scan in EVF Mode and Hi-Speed Mode,” on page 44
- Updated Figure 35: “REF and OB Readout,” on page 45
- Added “Multiple ROM Structure” on page 46
- Updated “Mode Transition” on page 47
- Updated Figure 37: “State Control,” on page 47
- Updated “Mode Change Sequence (Example: EVF to Full Resolution to EVF)” on page 48
- Updated “Mode Change Sequence (Example: EVF to Hi-Speed to EVF)” on page 49
- Updated “Mode Change Example - From EVF Mode to Full Resolution Mode via Pre-Flash A Mode” on page 50
- Updated Figure 44: “Power Save in HDTV, HD_60_16:9_LP, and HD_60_16:9_FS mode, EVF, Pre-Flash A, and Pre-Flash B Modes,” on page 53
- Updated Figure 45: “Power Save in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV Modes,” on page 54
- Added Figure 47: “HD_120_16:9_SLV Mode Frame Timing,” on page 55
- Added Figure 48: “HD_60_3:2_SLV Mode Frame Timing,” on page 56
- Updated Figure 53: “EVF Mode Frame Timing,” on page 60
- Updated Figure 54: “EVF Mode Subresolution Scheme,” on page 60
- Updated “HD_60_16:9_LP Mode” on page 61, including Figure 55: “HD_60_16:9_LP Mode Frame Timing,” on page 61
- Updated “Pre-Flash A Mode” on page 62, including Figure 56, Pre-Flash A Mode Frame Timing and Figure 57: “Pre-Flash A Mode Subresolution Scheme,” on page 62
- Updated “HD_60_16:9_FS Mode” on page 63, including Figure 58: “HD_60_16:9_FS Mode Frame Timing,” on page 63

- Added “Sensor Control Block Diagram and Pulses” on page 70
- Updated Figure 66: “Gain Update Timing in Full Resolution, HD60_3:2_SLV, HD120_16:9_SLV Modes,” on page 71
- Added “Pixel Sensitivity Control” on page 73
- Updated Table 30, Operating Mode Control Register
- Added “Inverter Amp Function” on page 77
- Added “CRM Function” on page 77
- Added “Vtx Pulsing Function” on page 78
- Removed Figure 66,”Cover Glass Spectral Transmission (0.15 mm Thickness”

Rev. A, Preliminary 10/4/12

- Initial release

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