AR0331 Register Reference

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

AR0331 Register Reference

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Introduction

This reference document describes the AR0331 registers. Summary and detailed information are presented in separate sections:

- “Register Lists and Default Values” on page 5
- “Detailed Register Descriptions” on page 17

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the AR0331 data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to “1.”

Register Lists and Default Values

Table 1 below lists sensor registers and their default values. Table 2 on page 13 lists sensor registers and their descriptions.

Locations that are shown as “Reserved” should not be accessed. The default read values of these registers are subject to change.

Caution **The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.**

Note: Green1 (G1) to corresponds to greenR or Gr; green2 (G2) corresponds to greenB or Gb.

Manufacturer-Specific Registers

Table 1: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R9216 (R0x2400)	altm_control	0000 0000 00dd dddd	3 (0x0003)
R9232 (R0x2410)	altm_power_gain	0000 0000 00dd dddd	16 (0x0010)
R9234 (R0x2412)	altm_power_offset	0000 0000 00dd dddd	16 (0x0010)
R9248 (R0x2420)	altm_fsharp_v	0000 0000 000d dddd	19 (0x0013)
R9250 (R0x2422)	altm_stats_ex_win_x_start	0000 dddd dddd dddd	0 (0x0000)
R9252 (R0x2424)	altm_stats_ex_win_width	0000 dddd dddd dddd	0 (0x0000)
R9254 (R0x2426)	altm_stats_ex_win_y_start	0000 dddd dddd dddd	0 (0x0000)
R9256 (R0x2428)	altm_stats_ex_win_height	0000 dddd dddd dddd	0 (0x0000)
R9272 (R0x2438)	altm_control_min_factor	0000 0000 dddd dddd	16 (0x0010)
R9274 (R0x243A)	altm_control_max_factor	0000 0000 dddd dddd	32 (0x0020)
R9276 (R0x243C)	altm_control_dark_floor	dddd dddd dddd dddd	0 (0x0000)
R9278 (R0x243E)	altm_control_bright_floor	dddd dddd dddd dddd	512 (0x0200)
R9280 (R0x2440)	altm_control_damper	0000 0000 0ddd dddd	2 (0x0002)
R9282 (R0x2442)	altm_control_key_k0	0000 0000 dddd dddd	128 (0x0080)
R9284 (R0x2444)	altm_control_key_k01_lo	dddd dddd dddd dddd	0 (0x0000)
R9286 (R0x2446)	altm_control_key_k01_hi	0000 0000 dddd dddd	4 (0x0004)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R9296 (R0x2450)	altm_out_pedestal	0000 dddd dddd dddd	0 (0x0000)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	9730 (0x2602)
R12290 (R0x3002)	y_addr_start	0000 0ddd dddd dddd	228 (0x00E4)
R12292 (R0x3004)	x_addr_start	0000 dddd dddd dddd	6 (0x0006)
R12294 (R0x3006)	y_addr_end	0000 0ddd dddd dddd	1315 (0x0523)
R12296 (R0x3008)	x_addr_end	0000 dddd dddd dddd	1933 (0x078D)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	1125 (0x0465)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd dddd	1100 (0x044C)
R12302 (R0x300E)	revision_number	dddd dddd	32 (0x20)
R12304 (R0x3010)	lock_control	dddd dddd dddd dddd	48879 (0xBEEF)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	88 (0x0058)
R12316 (R0x301C)	mode_select_	0000 000d	0 (0x00)
R12317 (R0x301D)	image_orientation_	0000 00dd	0 (0x00)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	168 (0x00A8)
R12321 (R0x3021)	software_reset_	0000 000d	0 (0x00)
R12326 (R0x3026)	gpi_status	???? ???? ???? ????	25856 (0x6500)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 000d dddd	6 (0x0006)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	4 (0x0004)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	66 (0x0042)
R12342 (R0x3036)	op_pix_clk_div	0000 0000 000d dddd	12 (0x000C)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12344 (R0x3038)	op_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R12346 (R0x303A)	frame_count	dddd dddd dddd dddd	65535 (0xFFFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12350 (R0x303E)	line_length_pck_cb	dddd dddd dddd dddd	1100 (0x044C)
R12352 (R0x3040)	read_mode	dddd dddd ddd0 0000	0 (0x0000)
R12354 (R0x3042)	extra_delay	dddd dddd dddd dddd	0 (0x0000)
R12358 (R0x3046)	flash	??d0 000d d0dd dddd	0 (0x0000)
R12360 (R0x3048)	flash2	dddd dddd dddd dddd	256 (0x0100)
R12374 (R0x3056)	green1_gain	0000 0ddd dddd dddd	128 (0x0080)
R12376 (R0x3058)	blue_gain	0000 0ddd dddd dddd	128 (0x0080)
R12378 (R0x305A)	red_gain	0000 0ddd dddd dddd	128 (0x0080)
R12380 (R0x305C)	green2_gain	0000 0ddd dddd dddd	128 (0x0080)
R12382 (R0x305E)	global_gain	0000 0ddd dddd dddd	128 (0x0080)
R12384 (R0x3060)	analog_gain	00dd dddd 00dd dddd	1542 (0x0606)
R12388 (R0x3064)	smia_test	000d dddd d0d0 dddd	6402 (0x1902)
R12398 (R0x306E)	datapath_select	dddd dddd 000d 00dd	36880 (0x9010)
R12400 (R0x3070)	test_pattern_mode	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12418 (R0x3082)	operation_mode_ctrl	0000 0000 0000 dddd	8 (0x0008)
R12420 (R0x3084)	operation_mode_ctrl_cb	0000 0000 0000 dddd	9 (0x0009)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12424 (R0x3088)	seq_ctrl_port	?d00 00dd dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 dddd dddd dddd	66 (0x0042)
R12428 (R0x308C)	y_addr_start_cb	0000 0ddd dddd dddd	4 (0x0004)
R12430 (R0x308E)	x_addr_end_cb	0000 dddd dddd dddd	1993 (0x07C9)
R12432 (R0x3090)	y_addr_end_cb	0000 0ddd dddd dddd	1539 (0x0603)
R12442 (R0x309A)	ratio_actual_t1_t2	0000 0??? ???? ????	0 (0x0000)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0000 0ddd	1 (0x0001)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	1548 (0x060C)
R12462 (R0x30AE)	x_odd_inc_cb	0000 0000 0000 0ddd	5 (0x0005)
R12464 (R0x30B0)	digital_test	ddd0 0000 d000 00d0	0 (0x0000)
R12466 (R0x30B2)	tempsens_data	0000 00dd dddd dddd	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	dddd dddd dddd dddd	0 (0x0000)
R12470 (R0x30B6)	spare_0x30b6	dddd dddd dddd dddd	0 (0x0000)
R12472 (R0x30B8)	spare_0x30b8	dddd dddd dddd dddd	0 (0x0000)
R12474 (R0x30BA)	digital_ctrl	0000 0ddd ddd0 dddd	2028 (0x07EC)
R12476 (R0x30BC)	green1_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12478 (R0x30BE)	blue_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12480 (R0x30C0)	red_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12482 (R0x30C2)	green2_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12484 (R0x30C4)	global_gain_cb	0000 0ddd dddd dddd	128 (0x0080)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12486 (R0x30C6)	tempsens_calib1	dddd dddd dddd dddd	291 (0x0123)
R12488 (R0x30C8)	tempsens_calib2	dddd dddd dddd dddd	17767 (0x4567)
R12490 (R0x30CA)	tempsens_calib3	dddd dddd dddd dddd	35243 (0x89AB)
R12492 (R0x30CC)	tempsens_calib4	dddd dddd dddd dddd	52719 (0xCDEF)
R12494 (R0x30CE)	grr_control1	0000 0000 dddd 0d0d	0 (0x0000)
R12496 (R0x30D0)	grr_control2	0000 0000 dddd dddd	5 (0x0005)
R12498 (R0x30D2)	grr_control3	dddd dddd dddd dddd	4 (0x0004)
R12506 (R0x30DA)	grr_control4	dddd dddd dddd dddd	10 (0x000A)
R12542 (R0x30FE)	noise_pedestal	0000 dddd dddd dddd	0 (0x0000
R12608 (R0x3140)	ae_roi_x_start_offset	0000 dddd dddd ddd0	0 (0x0000)
R12610 (R0x3142)	ae_roi_y_start_offset	0000 0ddd dddd ddd0	0 (0x0000)
R12612 (R0x3144)	ae_roi_x_size	0000 dddd dddd ddd0	2052 (0x0804)
R12614 (R0x3146)	ae_roi_y_size	0000 0ddd dddd ddd0	1556 (0x0614)
R12616 (R0x3148)	ae_hist_begin_perc	dddd dddd dddd dddd	0 (0x0000)
R12618 (R0x314A)	ae_hist_end_perc	dddd dddd dddd dddd	65535 (0xFFFF)
R12620 (R0x314C)	ae_hist_div	dddd dddd dddd dddd	256 (0x0100)
R12622 (R0x314E)	ae_norm_width_min	dddd dddd dddd dddd	32 (0x0020)
R12624 (R0x3150)	ae_mean_h	???? ???? ???? ????	0 (0x0000)
R12626 (R0x3152)	ae_mean_l	???? ???? ???? ????	0 (0x0000)
R12628 (R0x3154)	ae_hist_begin_h	???? ???? ???? ????	0 (0x0000)
R12630 (R0x3156)	ae_hist_begin_l	???? ???? ???? ????	0 (0x0000)
R12632 (R0x3158)	ae_hist_end_h	???? ???? ???? ????	0 (0x0000)
R12634 (R0x315A)	ae_hist_end_l	???? ???? ???? ????	0 (0x0000)
R12636 (R0x315C)	ae_hist_end_mean_h	???? ???? ???? ????	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12638 (R0x315E)	ae_hist_end_mean_l	???? ???? ???? ????	0 (0x0000)
R12640 (R0x3160)	ae_perc_low_end	???? ???? ???? ????	0 (0x0000)
R12642 (R0x3162)	ae_norm_abs_dev	???? ???? ???? ????	0 (0x0000)
R12672 (R0x3180)	delta_dk_control	dddd ddd0 dddd dddd	32905 (0x8089)
R12682 (R0x318A)	hdr_mc_ctrl1	0000 dddd dddd dddd	3600 (0x0E10)
R12684 (R0x318C)	hdr_mc_ctrl2	dddd 0000 0000 0ddd	49153 (0xC001)
R12686 (R0x318E)	hdr_mc_ctrl3	dddd 0000 0000 0000	0 (0x0000)
R12688 (R0x3190)	hdr_mc_ctrl4	ddd0 0000 0000 0000	0 (0x0000)
R12690 (R0x3192)	hdr_mc_ctrl5	000d dddd dddd dddd	1024 (0x0400)
R12692 (R0x3194)	hdr_mc_ctrl6	0000 dddd dddd dddd	3000 (0x0BB8)
R12694 (R0x3196)	hdr_mc_ctrl7	0000 dddd dddd dddd	3500 (0x0DAC)
R12696 (R0x3198)	hdr_mc_ctrl8	0ddd dddd dddd dddd	1566 (0x061E)
R12702 (R0x319E)	hdr_mc_ctrl9	dddd dddd dddd dddd	20544 (0x5040)
R12706 (R0x31A2)	hdr_mc_ctrl11	0000 dddd dddd dddd	3000 (0x0BB8)
R12716 (R0x31AC)	data_format_bits	000d dddd 000d dddd	4108 (0x100C)
R12718 (R0x31AE)	serial_format	0000 00dd 0000 0ddd	772 (0x0304)
R12736 (R0x31C0)	hispi_timing	dddd dddd dddd dddd	32768 (0x8000)
R12738 (R0x31C2)	hispi_blanking	dddd dddd dddd dddd	65535 (0xFFFF)
R12740 (R0x31C4)	hispi_sync_patt	dddd dddd dddd dddd	62805 (0xF555)
R12742 (R0x31C6)	hispi_control_status	??dd dddd dddd dddd	32768 (0x8000)
R12744 (R0x31C8)	hispi_crc_0	???? ???? ???? ????	0 (0x0000)
R12746 (R0x31CA)	hispi_crc_1	???? ???? ???? ????	0 (0x0000)
R12748 (R0x31CC)	hispi_crc_2	???? ???? ???? ????	0 (0x0000)
R12750 (R0x31CE)	hispi_crc_3	???? ???? ???? ????	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12752 (R0x31D0)	companding	0000 0000 0000 000d	1 (0x0001)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R127568 (R0x31E0)	pix_def_id	0000 00d0 0000 0000	512 (0x0200)
R12776 (R0x31E8)	horizontal_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 dddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 dddd dddd dddd	0 (0x0000)
R12788 (R0x31F4)	fuse_id1	dddd dddd dddd dddd	0 (0x0000)
R12790 (R0x31F6)	fuse_id2	dddd dddd dddd dddd	0 (0x0000)
R12792 (R0x31F8)	fuse_id3	dddd dddd dddd dddd	0 (0x0000)
R12794 (R0x31FA)	fuse_id4	dddd dddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	cci_ids	dddd dddd dddd dddd	12320 (0x3020)
R12800 (R0x3200)	adacd_control	0000 0000 0000 00dd	2 (0x0002)
R12802 (R0x3202)	adacd_noise_model1	0000 00dd dddd dddd	160 (0x00A0)
R12810 (R0x320A)	adacd_pedestal	0000 dddd dddd dddd	0 (0x0000)
R13824 (R0x3600)	p_gr_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13826 (R0x3602)	p_gr_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13828 (R0x3604)	p_gr_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13830 (R0x3606)	p_gr_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13832 (R0x3608)	p_gr_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13834 (R0x360A)	p_rd_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13836 (R0x360C)	p_rd_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13838 (R0x360E)	p_rd_p0q2	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13840 (R0x3610)	p_rd_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13842 (R0x3612)	p_rd_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13844 (R0x3614)	p_bl_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13846 (R0x3616)	p_bl_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13848 (R0x3618)	p_bl_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13850 (R0x361A)	p_bl_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13852 (R0x361C)	p_bl_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13854 (R0x361E)	p_gb_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13856 (R0x3620)	p_gb_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13858 (R0x3622)	p_gb_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13860 (R0x3624)	p_gb_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13862 (R0x3626)	p_gb_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13888 (R0x3640)	p_gr_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13890 (R0x3642)	p_gr_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13892 (R0x3644)	p_gr_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13894 (R0x3646)	p_gr_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13896 (R0x3648)	p_gr_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13898 (R0x364A)	p_rd_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13900 (R0x364C)	p_rd_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13902 (R0x364E)	p_rd_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13904 (R0x3650)	p_rd_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13906 (R0x3652)	p_rd_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13908 (R0x3654)	p_bl_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13910 (R0x3656)	p_bl_p1q1	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13912 (R0x3658)	p_bl_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13914 (R0x365A)	p_bl_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13916 (R0x365C)	p_bl_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13918 (R0x365E)	p_gb_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13920 (R0x3660)	p_gb_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13922 (R0x3662)	p_gb_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13924 (R0x3664)	p_gb_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13926 (R0x3666)	p_gb_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13952 (R0x3680)	p_gr_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13954 (R0x3682)	p_gr_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13956 (R0x3684)	p_gr_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13958 (R0x3686)	p_gr_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13960 (R0x3688)	p_gr_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13962 (R0x368A)	p_rd_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13964 (R0x368C)	p_rd_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13966 (R0x368E)	p_rd_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13968 (R0x3690)	p_rd_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13970 (R0x3692)	p_rd_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13972 (R0x3694)	p_bl_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13974 (R0x3696)	p_bl_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13976 (R0x3698)	p_bl_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13978 (R0x369A)	p_bl_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13980 (R0x369C)	p_bl_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13982 (R0x369E)	p_gb_p2q0	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13984 (R0x36A0)	p_gb_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13986 (R0x36A2)	p_gb_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13988 (R0x36A4)	p_gb_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13990 (R0x36A6)	p_gb_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14016 (R0x36C0)	p_gr_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14018 (R0x36C2)	p_gr_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14020 (R0x36C4)	p_gr_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14022 (R0x36C6)	p_gr_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14024 (R0x36C8)	p_gr_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14026 (R0x36CA)	p_rd_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14028 (R0x36CC)	p_rd_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14030 (R0x36CE)	p_rd_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14032 (R0x36D0)	p_rd_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14034 (R0x36D2)	p_rd_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14036 (R0x36D4)	p_bl_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14038 (R0x36D6)	p_bl_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14040 (R0x36D8)	p_bl_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14042 (R0x36DA)	p_bl_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14044 (R0x36DC)	p_bl_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14046 (R0x36DE)	p_gb_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14048 (R0x36E0)	p_gb_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14050 (R0x36E2)	p_gb_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14052 (R0x36E4)	p_gb_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14054 (R0x36E6)	p_gb_p3q4	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14080 (R0x3700)	p_gr_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14082 (R0x3702)	p_gr_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14084 (R0x3704)	p_gr_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14086 (R0x3706)	p_gr_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14088 (R0x3708)	p_gr_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14090 (R0x370A)	p_rd_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14092 (R0x370C)	p_rd_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14094 (R0x370E)	p_rd_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14096 (R0x3710)	p_rd_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14098 (R0x3712)	p_rd_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14100 (R0x3714)	p_bl_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14102 (R0x3716)	p_bl_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14104 (R0x3718)	p_bl_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14106 (R0x371A)	p_bl_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14108 (R0x371C)	p_bl_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14110 (R0x371E)	p_gb_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14112 (R0x3720)	p_gb_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14114 (R0x3722)	p_gb_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14116 (R0x3724)	p_gb_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14118 (R0x3726)	p_gb_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14208 (R0x3780)	poly_sc_enable	d000 0000 0000 0000	0 (0x0000)
R14210 (R0x3782)	poly_origin_c	0000 dddd dddd dddd	2652 (0x0A5C)
R14212 (R0x3784)	poly_origin_r	0000 0ddd dddd dddd	865 (0x0361)
R14272 (R0x37C0)	p_gr_q5	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14274 (R0x37C2)	p_rd_q5	dddd dddd dddd dddd	0 (0x0000)
R14276 (R0x37C4)	p_bl_q5	dddd dddd dddd dddd	0 (0x0000)
R14278 (R0x37C6)	p_gb_q5	dddd dddd dddd dddd	0 (0x0000)
R16082 (R0x3ED2)	dac_ld_6_7	dddd dddd dddd dddd	48966 (0xBF46)

Detailed Register Descriptions

Manufacturer-Specific Registers

Table 2: Manufacturer-Specific Register Description
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
9216 R0x2400	15:0	0x0003	altm_control (R/W)	N	N
	15:6	X	Reserved		
	5:2	0x0000	Reserved		
	1	0x0001	altm_control_enable 0: Adaptive Local Tone Mapping Disabled. 1: Adaptive Local Tone Mapping Enabled.	N	N
	0	0x0001	altm_bypass 0: Data goes through Adaptive Local Tone Mapping block. 1: Data does not go through the Adaptive Local Tone Mapping block.	N	Y
9232 R0x2410	15:0	0x0010	altm_power_gain	N	N
	Controls brightness of highlight regions of image. Legal values: [0, 127]				
9234 R0x2412	15:0	0x0010	altm_power_offset	N	N
	Controls brightness of low light regions of image. Legal values: [0, 63]				
9248 R0x2420	15:0	0x0013	altm_fsharp_v (R/W)	N	N
	Controls strength of ALTM sharpening function. Legal values: [0, 63].				
9250 R0x2422	15:0	0x0000	altm_stats_ex_win_x_start (R/W)	N	N
	First column of the exclusion window for ALTM stats. Legal values: [0, 4095].				
9252 R0x2424	15:0	0x0000	altm_stats_ex_win_width (R/W)	N	N
	Width of the exclusion window for ALTM stats. Legal values: [0, 4095].				
9254 R0x2426	15:0	0x0000	altm_stats_ex_win_y_start (R/W)	N	N
	First row of the exclusion window for ALTM stats. Legal values: [0, 4095].				
9256 R0x2428	15:0	0x0000	altm_stats_ex_win_height (R/W)	N	N
	Height of the exclusion window for ALTM stats. Legal values: [0, 4095].				
9272 R0x2438	15:0	0x0010	altm_control_min_factor (R/W)	N	N
	Adjustment factor applied to minimum illuminant Lmin Legal values: [0, 255].				
9274 R0x243A	15:0	0x0020	altm_control_max_factor (R/W)	N	N
	Adjustment factor applied to maximum illuminant Lmin Legal values: [0, 255].				
9276 R0x243C	15:0	0x0000	altm_control_dark_floor (R/W)	N	N
	Floor value for calculation of minimum illuminant Lmin Legal values: [0, 65535].				
9278 R0x243E	15:0	0x0200	altm_control_bright_floor (R/W)	N	N
	Floor value for calculation of maximum illuminant Lmin Legal values: [0, 65535].				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
9280 R0x2440	15:0	0x0002	altm_control_damper (R/W)	N	N
	Damping factor for L_{min} and L_{max} value changes Legal values: [0, 64].				
9282 R0x2442	15:0	0x0080	altm_control_key_k0 (R/W)	N	N
	Parameter k0 to calculate the key that control brightness of the tone mapped image Legal values: [0, 255].				
9284 R0x2444	15:0	0x0000	altm_control_key_k01_lo (R/W)	N	N
	Parameter k0*k1 to calculate the key that controls brightness of the tone mapped image Legal values: [0, 65535].				
9286 R0x2446	15:0	0x0004	altm_control_key_k01_hi (R/W)	N	N
	Parameter k0*k1 to calculate the key that controls brightness of the tone mapped image k01 = altm_control_key_k01_hi * 2^16 + altm_control_key_k01_lo Legal values: [0, 255].				
9296 R0x2450	15:0	0x0000	altm_out_pedestal (R/W)	N	N
	Pedestal added to the output of ALTM Legal values: [0, 4095].				
12288 R0x3000	15:0	0x2602	chip_version_reg (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].				
12290 R0x3002	15:0	0x00E4	y_addr_start (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				
12292 R0x3004	15:0	0x0006	x_addr_start (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.				
12294 R0x3006	15:0	0x0523	y_addr_end (R/W)	Y	YM
	The last row of visible pixels to be read out.				
12296 R0x3008	15:0	0x078D	x_addr_end (R/W)	Y	N
	The last column of visible pixels to be read out.				
12298 R0x300A	15:0	0x0465	frame_length_lines (R/W)	Y	YM
	The number of complete lines (rows) in the frame timing. This includes visible lines and vertical blanking lines.				
12300 R0x300C	15:0	0x044C	line_length_pck (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Only even values are allowed.				
12302 R0x300E	7:0	0x20	revision_number (R/W)	N	N
12304 R0x3010	15:0	0xBEEF	lock_control (R/W)	N	N
	This register protects the mirror mode select (register read mode). When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed, otherwise these values are locked.				
12306 R0x3012	15:0	0x0010	coarse_integration_time (R/W)	Y	N
	Integration time specified in multiples of line_length_pck_.				
12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N
	Coarse integration time in context B.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12314 R0x301A	15:0	0x0058	reset_register (R/W)	N	Y
	15	0x0000	Reserved		
	14:13	X	Reserved		
	12	0x0000	smia_serialiser_dis 0: HiSPi Interface Enabled. 1: HiSPi interface Disabled.	N	N
	11	0x0000	forced_pll_on 0: PLL will be powered down when the sensor is in standby (low power mode). 1: PLL will be enabled even when the sensor is in standby.	N	N
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	gpi_en 0: the primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER input is powered down and cannot be used. 1: the input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0000	parallel_en 0: The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N
	6	0x0001	drive_pins 0: The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the enabling and use of the pad OUTPUT_ENABLE_N) 1: The parallel data interface is driven. This bit is “do not care” unless bit[7]=1.	N	N
	5	0x0000	Reserved		
	4	X	Reserved		
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	stream 1: Places the sensor in streaming mode. 0: Places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12314 R0x301A	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	Y
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y
	Controls the operation of the sensor. For details see the bit field descriptions.				
12316 R0x301C	7:0	0x00	mode_select_ (R/W)	Y	N
	This bit is an alias of R0x301A-B[2].				
12317 R0x301D	7:0	0x00	image_orientation_ (R/W)	Y	YM
	7:2	X	Reserved		
	1	0x00	vert_flip This bit is an alias of R0x3040[15].	Y	YM
	0	0x00	horiz_mirror This bit is an alias of R0x3040[14].	Y	YM
12318 R0x301E	15:0	0x00A8	data_pedestal (R/W)	N	Y
	Constant offset that is added to pixel values at the end of datapath (after all corrections).				
12321 R0x3021	7:0	0x00	software_reset_ (R/W)	N	Y
	This bit is an alias of R0x301A-B[0].				
12326 R0x3026	15:0	0x6500	gpi_status (RO)	N	N
	15:3	RO	Reserved		
	2	RO	Reserved		
	1	RO	Reserved		
	0	RO	Reserved		
	Reflects the status of the input pins: TRIGGER(2), OUTPUT_ENABLE_N(1), SADDR(0). Upper bits are hardwired to a constant.				
12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N
	Bits [6:4] of this register define the phase of the output pixclk. 2 sets of values are correct: a) 000, 010, 100, 110 => 0 delay (DOUT changes on rising edge of pixclk). b) 001, 011, 101, 111 => 1/2 clk delay (DOUT changes on falling edge of pixclk).				
12330 R0x302A	15:0	0x0006	vt_pix_clk_div (R/W)	N	N
	Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL).				
12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N
	sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL).				
12334 R0x302E	15:0	0x0004	pre_pll_clk_div (R/W)	N	N
	PLL input pre-divider value				
12336 R0x3030	15:0	0x0042	pll_multiplier (R/W)	N	N
	PLL_MULTIPLIER				
12342 R0x3036	15:0	0x000C	op_pix_clk_div (R/W)	N	Y
	Clock divisor applied to the output system clock to generate the output pixel clock.				
12344 R0x3038	15:0	0x0001	op_sys_clk_div (R/W)	N	Y
	Clock divisor applied to PLL output clock to generate output system clock. Read-only.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12346 R0x303A	15:0	0xFFFF	frame_count (R/W)	N	N
	Counts the number of output frames. At the startup is initialized to 0xFFFF.				
12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N
	15:2	X	Reserved		
	1	RO	standby_status This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].	N	N
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N
12350 R0x303E	15:0	0x044C	line_length_pck_cb (R/W)	Y	N
	Line length in context B. The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Only even values are allowed. For smooth operation this would be the same value as LINE_LENGTH_PCK (0x300C).				
12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ (+1) is read out of the sensor first. This register can only be changed when streaming is disabled	Y	YM
	14	0x0000	horiz_mirror 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ (+1) is read out of the sensor first. This register can only be changed when streaming is disabled	Y	YM
	13	0x0000	read_mode_col_bin Column binning mode in context A. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	12	0x0000	read_mode_row_bin Analog row binning control in context A. Use when row-wise skipping is enabled by setting y_odd_inc. The y_addr_start must be an even number when using row binning.	Y	N
	11	0x0000	read_mode_col_bin_cb Column binning mode in context B. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	10	0x0000	read_mode_row_bin_cb Analog row binning control for context B. Use when row-wise skipping is enabled by setting y_odd_inc. The y_addr_start must be an even number when using row binning.	Y	N
	9:6	X	Reserved		
	5	0x0000	read_mode_col_sum Column sum mode. Pixel values are summed in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	4:0	X	Reserved		

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12354 R0x3042	15:0	0x0000	extra_delay (R/W)	Y	N
	The last row in the frame is extended by the number of the sensor core clock periods specified here. The extra_delay must be configured to an even value. This register can be used to fine-tune the sensor maximum frame-rate.				
12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N
	13:9	X	Reserved		
	8	0x0000	en_flash Enables the flash. The flash is asserted when an integration (either T1 or T2) is ongoing.	Y	Y
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	6	X	Reserved		
	5:3	0x0000	xenon_frames_enable 0: Xenon flash disabled. 1-6: Number of frames with Xenon flash. 7: Xenon flash enable for all frames.	N	N
	2:0	0x0000	xenon_frames_delay XENON_FRAMES_DELAY[2:0]: Number of the frames before the first time Xenon flash is actuated.	Y	N
	See bit fields for definition od flash and Xenon Flash control.				
12360 R0x3048	15:0	0x0100	flash2 (R/W)	N	N
	Xenon flash pulse width in clock periods.				
12374 R0x3056	15:0	0x0080	green1_gain (R/W)	Y	N
	Digital gain for Green1 (Gr) pixels in Context A, in format of xxxx.yyyyyyy.				
12376 R0x3058	15:0	0x0080	blue_gain (R/W)	Y	N
	Digital gain for Blue pixels, in format of xxxx.yyyyyyy.				
12378 R0x305A	15:0	0x0080	red_gain (R/W)	Y	N
	Digital gain for Red pixels, in format of xxxx.yyyyyyy.				
12380 R0x305C	15:0	0x0080	green2_gain (R/W)	Y	N
	Digital gain for Green2 (Gb) pixels in Context A, in format of xxxx.yyyyyyy.				
12382 R0x305E	15:0	0x0080	global_gain (R/W)	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12384 R0x3060	15:0	0x0606	analog_gain (R/W)	Y	N
	15:14	X	Reserved		
	13:12	0x0000	coarse_gain_cb Coarse Analog gain in context B.	Y	N
	11:8	0x0006	fine_gain_cb Fine analog gain in context B	Y	N
	7:6	X	Reserved		
	5:4	0x0000	coarse_gain Coarse Analog gain in context A.	Y	N
	3:0	0x0006	fine_gain Fine analog gain in context A.	Y	N
	Defines analog gains for both contexts				
12388 R0x3064	15:0	0x1902	smia_test (R/W)		
	15:13	X	Reserved		
	12	0x0001	Reserved		
	11:10	0x0002	Reserved		
	9	0x0000	Reserved		
	8	0x0001	embedded_data 0: Frames out of the sensor exclude the embedded data. 1: Frames of data out of the sensor include 2 rows of embedded data. This register field should only be change while the sensor is in software standby. Disabling the embedded data will not reduce the number of vertical blanking rows.	N	N
	7	0x0000	embedded_stats_en 0: Embedded statistics are not transmitted on the 2 stats rows after the frame pixel data. 1: Embedded statistics are transmitted on the 2 stats data rows after the frame pixel data.	N	N
	6:4	X	Reserved		
	3:0	0x0002	Reserved		

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12398 R0x306E	15:0	0x9010	datapath_select (R/W)	N	N
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[11:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value (111) results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value (111) results in the fastest edge rate. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	9	0x0000	high_vcm 0: Selects HiSPi low vcm (SLVS) mode. VDD_SLVS must be 0.4V 1: Selects HiSPi high vcm mode. VDD_SLVS = VDD_IO = 1.8V	N	N
	8	0x0000	datapath_select_bit8 Not used.	N	N
	7:5	X	Reserved		
	4	0x0001	Reserved		
	3:2	X	Reserved		
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID 11: Reserved.	N	N
12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y
	0: Normal operation. Generates output data from pixel array 1: Solid color test pattern. 2: Full color bar test pattern 3: Fade to gray color bar test pattern 256: Walking 1 test pattern (12-bit) Other: Reserved.				
12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.				
12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.				
12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12418 R0x3082	15:0	0x0008	operation_mode_ctrl (R/W)	Y	N
	15:4	X	Reserved		
	3:2	0x0002	ratio_t1_t2 T1/T2 Exposure Ratio for Context A. 0: 4x 1: 8x 2: 16x 3: 32x	Y	N
	1:0	0x0000	operation_mode Operation Mode for Context A. 0: HDR mode 1: ERS Linear mode	N	N
12420 R0x3084	15:0	0x0009	operation_mode_ctrl_cb (R/W)	Y	N
	15:4	X	Reserved		
	3:2	0x0002	ratio_t1_t2_cb T1/T2 Exposure Ratio for Context B. 0: 4x 1: 8x 2: 16x 3: 32x	N	N
	1:0	0x0001	operation_mode_cb Operation Mode for Context B. 0: HDR mode 1: ERS Linear mode	N	N
12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N
	Register used to write to or read from the sequencer RAM.				
12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N
	14	0x0001	auto_inc_on_read 1: The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only 1 byte).	N	N
	13:9	X	Reserved		
	8:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N
	Register controlling the read and write to sequencer RAM.				
12426 R0x308A	15:0	0x0042	x_addr_start_cb (R/W)	N	N
	X_ADDR_START for context B				
12428 R0x308C	15:0	0x0004	y_addr_start_cb (R/W)	N	N
	Y_ADDR_START for context B				
12430 R0x308E	15:0	0x07C9	x_addr_end_cb (R/W)	N	N
	X_ADDR_END for context B				
12432 R0x3090	15:0	0x0603	y_addr_end_cb (R/W)	N	N
	Y_ADDR_END for context B				
12442 R0x309A	15:0	0x0000	ratio_actual_t1_t2 (RO)	N	N
	Actual t1/t2 ratio calculated by RTL. Register has 5 fractional bits.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N
	Read-only.				
12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM
	1: No skip. 3: Skip 2. 5: Skip 3. Other values are not supported.				
12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N
	Read-only.				
12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM
	1: No skip. 3: Skip 2. 5: Skip 3. Other values are not supported.				
12456 R0x30A8	15:0	0x0001	y_odd_inc_cb (R/W)	N	N
	Y_ODD_INC context B				
12458 R0x30AA	15:0	0x060C	frame_length_lines_cb (R/W)	N	N
	FRAME_LENGTH_LINES context B. See description for R0x300A				
12462 R0x30AE	15:0	0x0005	x_odd_inc_cb (R/W)	N	N
	X_ODD_INC context B				
12464 R0x30B0	15:0	0x0000	digital_test (R/W)	N	Y
	15	0x0000	Reserved		
	14	0x0000	pll_complete_bypass 0: PLL is enabled 1: PLL is bypassed. EXTCLK will be used. Note that the serial interface does not function when PLL is bypassed.	N	N
	13	0x0000	context_b Context Control. 0: Use Context A 1: Use Context B	N	N
	12:8	X	Reserved		
	7	0x0000	mono_chrome_operation Mono Chrome Sensor Operation. 0: Normal operation. 1: Sensor will operate similar to a mono chrome sensor. Useful in the bin2 mode.	N	N
	6:2	X	Reserved		
	1	0x0000	no_sh_jump_limit 0: In HDR mode, the increase in integration time will be limited to 4 times T2/T1 ratio. 1: In HDR mode, the sensor will accept any increase in the integration time.	N	N
	0	X	Reserved		
12466 R0x30B2	15:0	0x0000	tempsens_data (R/W)	Y	N
	Output value from temperature sensor.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)	N	N
	15:6	0x0000	retrigger_threshold When the measured absolute temperature (ADC value) changes more than this setting, the delta dark algorithm is retriggered and the temperature is saved as the comparison level for the next measurement. If the value is set to zero, the retrigger function will be disabled.	N	N
	5	0x0000	temp_clear_value Clear data register (sanity check).	N	N
	4	0x0000	temp_start_conversion When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated.	N	N
	3:1	0x0000	Reserved		
	0	0x0000	tempsens_power_on 0: Temperature sensor power on 1: Temperature sensor power off	N	N
	Control register for temperature sensor				
12470 R0x30B6	15:0	0x0000	spare_0x30b6 (R/W)	N	N
	Spare register for tempsens calibration values.				
12472 R0x30B8	15:0	0x0000	spare_0x30b8 (R/W)		
	Spare register for tempsens calibration data.				
12474 R0x30BA	15:0	0x07EC	digital_ctrl (R/W)	Y	N
	15:11	X	Reserved		
	10	0x0001	Reserved		
	9	0x0001	Reserved		
	8	0x0001	combi_mode 1: Operation mode can switch seamlessly between HDR and Linear mode (no bad frames). The HDR sequencer is used. T1 data is output when linear mode is set by register R0x3082.	Y	N
	7	0x0001	Reserved		
	6	0x0001	Reserved		
	5	0x0001	dither_enable Enables dithering after digital gain. Dither will automatically disabled if one of digital color gains is less than 2.	N	N
	4	X	Reserved		
	3:2	0x0003	Reserved		
	1:0	0x0000	Reserved		
12476 R0x30BC	15:0	0x0080	green1_gain_cb (R/W)	N	N
	Digital gain for Green1 (Gr) pixels in Context B, in format of xxxx.yyyyyyy.				
12478 R0x30BE	15:0	0x0080	blue_gain_cb (R/W)	N	N
	Digital gain for Blue pixels in Context B, in format of xxxx.yyyyyyy.				
12480 R0x30C0	15:0	0x0080	red_gain_cb (R/W)	N	N
	Digital gain for Red pixels in Context B, in format of xxxx.yyyyyyy.				
12482 R0x30C2	15:0	0x0080	green2_gain_cb (R/W)	N	N
	Digital gain for Green2 (Gb) pixels in Context B, in format of xxxx.yyyyyyy.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12484 R0x30C4	15:0	0x0080	global_gain_cb (R/W)	N	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers in Context B. Reading from this register returns the value most recently written to the green1_gain register.				
12486 R0x30C6	15:0	0x0123	tempsens_calib1 (R/W)	N	N
12488 R0x30C8	15:0	0x4567	tempsens_calib2 (R/W)	N	N
12490 R0x30CA	15:0	0x89AB	tempsens_calib3 (R/W)	N	N
12492 R0x30CC	15:0	0xCDEF	tempsens_calib4 (R/W)	N	N
12494 R0x30CE	15:0	0x0000	grr_control1 (R/W)	N	N
	15:8	X	Reserved		
	7	0x0000	shutter_always_open 1: The shutter pin will always be asserted (OPEN) in GRR mode.	N	N
	6	0x0000	shutter_disable 1: The shutter pin will be disabled (CLOSED) in GRR mode.	N	N
	5	0x0000	frame_start_mode 1: The sensor will match the frame time to the frame_length_lines and line_length_pck. It will not increase the frame time even if the integration time specified by coarse integration time is longer than the minimum frame-time.	N	N
	4	0x0000	slave_mode 1: The start of sensor readout will be synchronized with the external trigger (applied to pad TRIGGER).	N	N
	3	X	Reserved		
	2	0x0000	ext_shut_pulsed 0: The external shutter is controlled by level shift. 1: The external shutter is controlled by user defined pulse	N	N
	1	X	Reserved		
	0	0x0000	grr_mode 0: Normal ERS mode. 1: Global reset release mode.	N	N
12496 R0x30D0	15:0	0x0005	grr_control2 (R/W)	N	N
	15:8	X	Reserved		
	7:0	0x0005	gr_delay Delay between external trigger and global reset in number of rows.	N	N
12498 R0x30D2	15:0	0x0004	grr_control3 (R/W)	N	N
	15:0	0x0004	ext_shut_pulse_width Width of the external shutter pulse in clock cycles. 0: The shutter pulse will be controlled by GRR_CONTROL4.	N	N
12506 R0x30DA	15:0	0x000A	grr_control4 (R/W)	N	N
	15:0	0x000A	ext_shut_delay	N	N
	Delay between external trigger and close of external shutter in number of rows.				
12542 R0x30FE	15:0	0x0000	noise_pedestal Should be set to the same value as adacd pedestal.	N	Y

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12608 R0x3140	15:0	0x0000	ae_roi_x_start_offset (R/W)	N	N
	Number of pixels into each row before the ROI starts NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels				
12610 R0x3142	15:0	0x0000	ae_roi_y_start_offset (R/W)	N	N
	Number of rows into each frame before the ROI starts				
12612 R0x3144	15:0	0x0804	ae_roi_x_size (R/W)	N	N
	Number of columns in the ROI				
12614 R0x3146	15:0	0x0614	ae_roi_y_size (R/W)	N	N
	Number of rows in the ROI				
12616 R0x3148	15:0	0x0000	ae_hist_begin_perc (R/W)	N	N
	Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx				
12618 R0x314A	15:0	0xFFFF	ae_hist_end_perc (R/W)	N	N
	Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)				
12620 R0x314C	15:0	0x0100	ae_hist_div (R/W)	N	N
	Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16				
12622 R0x314E	15:0	0x0020	ae_norm_width_min (R/W)	N	N
	Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option i.e. all absolute deviation is normalized by hist_end - hist_begin				
12624 R0x3150	15:0	0x0000	ae_mean_h (RO)	N	N
	The true mean of all Gr pixels in the ROI (higher bits)				
12626 R0x3152	15:0	0x0000	ae_mean_l (RO)	N	N
	The true mean of all Gr pixels in the ROI (16 least significant bits)				
12628 R0x3154	15:0	0x0000	ae_hist_begin_h (RO)	N	N
	Code value corresponding to the histogram bin below which(hist_begin_perc*100)% of pixels exist (higher bits)				
12630 R0x3156	15:0	0x0000	ae_hist_begin_l (RO)	N	N
	Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower 16 bits)				
12632 R0x3158	15:0	0x0000	ae_hist_end_h (RO)		
	Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (higher bits)				
12634 R0x315A	15:0	0x0000	ae_hist_end_l (RO)	N	N
	Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (lower 16 bits)				
12636 R0x315C	15:0	0x0000	ae_hist_end_mean_h (RO)		
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (higher bits)				
12638 R0x315E	15:0	0x0000	ae_hist_end_mean_l (RO)	N	N
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (lower 16 bits)				
12640 R0x3160	15:0	0x0000	ae_perc_low_end (RO)	N	N
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12642 R0x3162	15:0	0x0000	ae_norm_abs_dev (RO)		
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				
12672 R0x3180	15:0	0x8089	delta_dk_control (R/W)	N	N
	15	0x0001	delta_dk_sub_en Enables the delta dark correction.	N	N
	14	0x0000	delta_dk_every_frame Running the delta dark algorithm every frame or when gain, integration time is changing.	N	N
	13	0x0000	delta_dk_recalc Forces recalculation of the delta dark value.	N	N
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	delta_dk_gradient_removal Enables the gradient removal algorithm.	N	N
	9	0x0000	delta_dk_gradient_every_frame 1: The measured delta dark gradient will be applied every frame. 0: The measured delta dark gradient will be applied to the first frame after standby only. The delta dark values will be recalculated for the second frame after standby.	N	N
	8	X	Reserved		
	7:4	0x0008	delta_dk_rows Number of dark rows to use for delta dark measurements.	N	N
	3:0	0x0009	Reserved		
12682 R0x318A	15:0	0x0E10	hdr_mc_ctrl1 (R/W)	Y	N
	15:12	X	Reserved		
	11:0	0x0E10	s2_threshold Threshold level for end point of weighting transfer function. Pixel values above this level are chosen from exposure 2 only.	Y	N

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12684 R0x318C	15:0	0xC001	hdr_mc_ctrl2 (R/W)	Y	N
	15	0x0001	smoothing_filter_enable 0: 3-tab Motion Smoothing Filter Disabled. 1: The 3-tab Motion Smoothing Filter Enabled. Filtering is done on the motion area only.	Y	N
	14	0x0001	motion_correct_enable Motion Correction Control. 0: Motion Correction Disabled. When Motion Correction is disabled, the input data will be fed through the module as is, but with the same delay as when the algorithm is enabled. Set R0x318C[13] to remove this delay. 1: Motion Correction is enabled.	Y	N
	13	0x0000	Reserved		
	12	0x0000	Reserved		
	11:3	X	Reserved		
	2	0x0000	all_motion_functions_force_on 1: All motion-related functions (motion correction and motion smoothing filter) are forced to be on also for HDR bypass modes.	Y	N
	1	0x0000	Reserved		
	0	0x0001	blue_halo_enable Blue Halo Algorithm Control. 0: Blue Halo Algorithm Disabled. When Blue Halo Algorithm is disabled, the input data still goes through the module as is, but with the same delay as when the algorithm is enabled. Set R0x318C[1] to remove this delay. 1: Blue Halo Algorithm Enabled.	Y	N
12686 R0x318E	15:0	0x0000	hdr_mc_ctrl3 (R/W)	Y	N
	15:14	0x0000	bypass_pix_comb_cb Data select for context B. 0: HDR data 1: T1 data. 2: T2 data. 3: Interleave mode(T1, T2, ...)	Y	N
	13:12	0x0000	bypass_pix_comb Data select for context A. 0: HDR data. 1: T1 data. 2: T2 data. 3: Interleave mode (T1, T2, ...)	Y	N
	11:0	X	Reserved		

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12688 R0x3190	15:0	0x0000	hdr_mc_ctrl4 (R/W)	Y	N
	15	0x0000	Reserved		
	14	0x0000	noise_filter_dlo_en Enables noise filtering of small pixel values in the digital lateral overflow pixel combination.	Y	N
	13	0x0000	pixel_build_dlo 0: Digital Lateral Overflow Disabled 1: Use the digital lateral overflow method for combining t1and t2 data. This also overrides R0x318C[14], MOTION_CORRECT_EN which gets disabled.	Y	N
	12:0	X	Reserved		
12690 R0x3192	15:0	0x0400	hdr_mc_ctrl5 (R/W)	Y	N
	15:13	X	Reserved		
	12:0	0x0400	s12_range Range for the HDR smooth combination weighting transfer function defined by S2-S1.	Y	N
12692 R0x3194	15:0	0x0BB8	hdr_mc_ctrl6 (R/W)	Y	N
	15:12	X	Reserved		
	11:0	0x0BB8	t1_barrier Barrier for clipping T1 data in the digital lateral overflow combination method.	Y	N
12694 R0x3196	15:0	0x0DAC	hdr_mc_ctrl7 (R/W)	Y	N
	15:12	X	Reserved		
	11:0	0x0DAC	t2_barrier Barrier for clipping T2 data in the digital lateral overflow combination method.	Y	N
12696 R0x3198	15:0	0x061E	hdr_mc_ctrl8 (R/W)		
	15	X	Reserved		
	14:8	0x0006	motion_detect_q2 Range for the motion detection algorithm.	Y	N
	7:0	0x001E	motion_detect_q1 Lower threshold for the motion detection algorithm.	Y	N

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12702 R0x319E	15:0	0x5040	hdr_mc_ctrl9 (R/W)	Y	N
	15:12	0x0005	s12_dlo_range Range of code values for the noise filter weighting transfer function for digital lateral overflow defined by s2_dlo - s1_dlo 4'b0000 = 1 4'b0001 = 2 4'b0010 = 4 4'b0011 = 8 4'b0100 = 16 4'b0101 = 32 4'b0110 = 64 4'b0111 = 128 4'b1000 = 256 4'b1001 = 512 4'b1010 = 1024 4'b1011 = 2048 4'b1100 = 4096 >= 4'b1101 = 8192 Setting the range to 8192 effectively sets s1_dlo to -4095 and s2_dlo to 4095.	N	N
	11:0	0x0040	s2_dlo_threshold Threshold level for end point of noise filter weighting transfer function for digital lateral overflow.	N	N
12706 R0x31A2	15:0	0x0BB8	hdr_mc_ctrl11 (R/W)		
	15:12	X	Reserved		
	11:0	0x0BB8	noise_dlo_dis_threshold For the digital lateral overflow method, if either T1 data or T2 data is greater than this threshold, noise filtering is turned off. Evaluated on a single pixel.	Y	N
12716 R0x31AC	15:0	0x100C	data_format_bits (R/W)	Y	N
	15:13	X	Reserved		
	12:8	0x0010	data_format_in The bit-width of the pixel data pre compression or truncation	N	N
	7:5	X	Reserved		
	4:0	0x000C	data_format_out The bit-width of the pixel data post compression or truncation. 0x10: 16-bit 0x0C: 12-bit 0x0A: 10-bit	N	N
	Data formats pre and post compression or truncation. Compression or truncation is selected in COMPANDING 0x31D0				
12718 R0x31AE	15:0	0x0304	serial_format (R/W)		
	The upper byte of this register (interface type) is read-only. When the serial interface is enabled (reset_register[12]=0), the lower byte configures the number of HiSPi lanes to be used: 4: Quad-lane HiSPi 2: Dual-lane HiSPi 1: Single-lane HiSPi or for parallel				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12736 R0x31C0	15:0	0x8000	hispi_timing (R/W)		
	15	0x0001	reva_comp 0: 'Disabled' - lowest power state, *_mode_sel = 2'b00. This is the 'power up' state and the state when the sensor goes into standby. - 'Inactive' - *_mode_sel = 2'b11 but internal high speed clocks gated and transmitted clock can be stopped (as selected by 'cont_tx_clk'). This is the state during blanking - 'Active' - *_mode_sel - high speed transmission mode 1: HiSPi protocol operates as in previous designs; *_mode_sel will always = 2'b11. When the sensor goes into standby the HiSPi data and clock lanes will go high-Z (by asserting *_zstate)	N	N
	14:12	0x0000	clock_del Delay applied to the clock lane in 1/8 unit interval (UI) steps.	N	N
	11:9	0x0000	data3_del Delay applied to Data Lane 3 in 1/8 unit interval (UI) steps.	N	N
	8:6	0x0000	data2_del Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps.	N	N
	5:3	0x0000	data1_del Delay applied to Data Lane 1 in 1/8 unit interval (UI) steps.	N	N
	2:0	0x0000	data0_del Delay applied to Data Lane 0 in 1/8 unit interval (UI) steps.	N	N
	Within the HiSPi PHY there is a DLL connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.				
12738 R0x31C2	15:0	0xFFFF	hispi_blanking (R/W)	N	N
	HiSPi Blanking Data				
12740 R0x31C4	15:0	0xF555	hispi_sync_patt (R/W)		
	15:8	0x00F5	Reserved		
	7:0	0x0055	Reserved		
	HiSPi Sync Pattern				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)		
	15	RO	Reserved		
	14	RO	Reserved		
	13	0x0000	Reserved		
	12	X	Reserved		
	11:10	0x0000	hispi_mode_sel Will select the HiSPi output protocol: 00: Data will be transmitted according to hispiS (Streaming) protocol 01: Data will be transmitted according to hispiSP protocol. SP-Packetized or SP-Streaming is selected using register R0x31C6[2]	N	N
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7	0x0000	test_enable 1: The test pattern (as defined by the test_mode) is output through the HiSPi PHY interface.	N	N
	6:4	0x0000	test_mode Determines test mode if the test mode is enabled. 0: Reserved 1: Reserved 2: Transmit differential 0 on all enabled data lanes 3: Transmit differential 1 on all enabled data lanes 4: Transmit a square wave at half the potential serial data rate on all enabled data lanes 5: Transmit a square wave at the pixel data rate on all enabled data lanes 6: Reserved 7: Transmit a continuous, repeated, sequence of pseudorandom data, with no SAV code, copied on all enabled data lanes.	N	N
	3	0x0000	blanking_data_enable Value 0, the default pattern (constant 1) is output during horizontal and vertical blanking periods Value 1, the pattern defined by the blanking_data input is output during horizontal and vertical blanking periods NOTE: for hispiSP only	N	N
	2	0x0000	streaming_mode 0: Data will be transmitted in 'packetized' format when hispiSP protocol is selected 1: Data will be transmitted in 'streaming' format when hispiSP protocol is selected Not relevant when hispi_mode_sel[1:0] is not set to 01 (HiSPiSP)	N	N
	1	0x0000	output_msb_first Output MSB of hispi_data first	N	N
	0	0x0000	vert_left_bar_en An optional filler code of 1s may be padded after the sync code. When filler codes are enabled, the receiver must window the received image to eliminate the first data word per data lane columns per PHYs).	N	N
	See descriptions in the bit fields.				
12744 R0x31C8	15:0	0x0000	hispi_crc_0 (RO)		

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12746 R0x31CA	15:0	0x0000	hispi_crc_1 (RO)		
12748 R0x31CC	15:0	0x0000	hispi_crc_2 (RO)		
12750 R0x31CE	15:0	0x0000	hispi_crc_3 (RO)		
12752 R0x31D0	15:0	0x0001	companding (R/W)	N	N
	15:1	X	Reserved		
	0	0x0001	compand_en Enables companding. The actual input and output data width is set in DATA_FORMAT_BITS 0x31AC	N	N
12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)	N	N
12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)	N	N
	Checksum of I2C write operations.				
12768 R0x31E0	15:0	0x0200	pix_def_id	N	N
	15:10	X	Reserved		
	9	0x0001	pix_def_2D_single_en	N	N
	8:0	x	Reserved		
	Checksum of I2C write operations.				
12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)	N	N
	Specifies the start row for the test cursor.				
12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)	N	N
	Specifies the start column for the test cursor.				
12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)		
	Specifies the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.				
12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)		
	Specifies the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.				
12788 R0x31F4	15:0	0x0000	fuse_id1 (R/W)		
	Read protected. Set reset_register[5] to get access to this register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be overwritten and will be restored on reset)				
12790 R0x31F6	15:0	0x0000	fuse_id2 (R/W)		
	Read protected. Set reset_register[5] to get access to this register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be overwritten and will be restored on reset)				
12792 R0x31F8	15:0	0x0000	fuse_id3 (R/W)	N	N
	Read protected. Set reset_register[5] to get access to this register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be overwritten and will be restored on reset)				
12794 R0x31FA	15:0	0x0000	fuse_id4 (R/W)		
	Read protected. Set reset_register[5] to get access to this register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be overwritten and will be restored on reset)				
12796 R0x31FC	15:0	0x3020	cci_ids (R/W)	N	N
	CCI addresses.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12800 R0x3200	15:0	0x0002	adacd_control (R/W)	N	N
	15:2	X	Reserved		
	1	0x0001	adacd_filter_en 0: AdaCD Noise Filter is disabled. 1: AdaCD Noise Filter is enable.d	N	N
	0	0x0000	low_light Adjust AdaCD algorithm for low light	N	N
12802 R0x3202	15:0	0x00A0	adacd_noise_model1 (R/W)	N	N
	Filter strength. Larger values have greater noise reduction, but more blurring. Smaller values result in more detail, but less noise filtering.				
12810 R0x320A	15:0	0x0000	adacd_pedestal (R/W)	N	N
	AdaCD pedestal value. Should be set to the same value as the noise pedestal.				
13824 R0x3600	15:0	0x0000	p_gr_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13826 R0x3602	15:0	0x0000	p_gr_p0q1 (R/W)		
	P0 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13828 R0x3604	15:0	0x0000	p_gr_p0q2 (R/W)	N	N
	P0 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13830 R0x3606	15:0	0x0000	p_gr_p0q3 (R/W)		
	P0 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13832 R0x3608	15:0	0x0000	p_gr_p0q4 (R/W)		
	P0 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13834 R0x360A	15:0	0x0000	p_rd_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13836 R0x360C	15:0	0x0000	p_rd_p0q1 (R/W)		
	P0 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13838 R0x360E	15:0	0x0000	p_rd_p0q2 (R/W)	N	N
	P0 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13840 R0x3610	15:0	0x0000	p_rd_p0q3 (R/W)	N	N
	P0 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13842 R0x3612	15:0	0x0000	p_rd_p0q4 (R/W)	N	N
	P0 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13844 R0x3614	15:0	0x0000	p_bl_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
13846 R0x3616	15:0	0x0000	p_bl_p0q1 (R/W)		
	P0 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13848 R0x3618	15:0	0x0000	p_bl_p0q2 (R/W)	N	N
	P0 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13850 R0x361A	15:0	0x0000	p_bl_p0q3 (R/W)		
	P0 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13852 R0x361C	15:0	0x0000	p_bl_p0q4 (R/W)		
	P0 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13854 R0x361E	15:0	0x0000	p_gb_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13856 R0x3620	15:0	0x0000	p_gb_p0q1 (R/W)	N	N
	P0 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13858 R0x3622	15:0	0x0000	p_gb_p0q2 (R/W)	N	N
	P0 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13860 R0x3624	15:0	0x0000	p_gb_p0q3 (R/W)	N	N
	P0 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13862 R0x3626	15:0	0x0000	p_gb_p0q4 (R/W)	N	N
	P0 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13888 R0x3640	15:0	0x0000	p_gr_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13890 R0x3642	15:0	0x0000	p_gr_p1q1 (R/W)	N	N
	P1 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13892 R0x3644	15:0	0x0000	p_gr_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13894 R0x3646	15:0	0x0000	p_gr_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13896 R0x3648	15:0	0x0000	p_gr_p1q4 (R/W)		
	P1 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13898 R0x364A	15:0	0x0000	p_rd_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
13900 R0x364C	15:0	0x0000	p_rd_p1q1 (R/W)		
	P1 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13902 R0x364E	15:0	0x0000	p_rd_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13904 R0x3650	15:0	0x0000	p_rd_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13906 R0x3652	15:0	0x0000	p_rd_p1q4 (R/W)		
	P1 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13908 R0x3654	15:0	0x0000	p_bl_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13910 R0x3656	15:0	0x0000	p_bl_p1q1 (R/W)	N	N
	P1 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13912 R0x3658	15:0	0x0000	p_bl_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13914 R0x365A	15:0	0x0000	p_bl_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13916 R0x365C	15:0	0x0000	p_bl_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13918 R0x365E	15:0	0x0000	p_gb_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13920 R0x3660	15:0	0x0000	p_gb_p1q1 (R/W)	N	N
	P1 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13922 R0x3662	15:0	0x0000	p_gb_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13924 R0x3664	15:0	0x0000	p_gb_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13926 R0x3666	15:0	0x0000	p_gb_p1q4 (R/W)		
	P1 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13952 R0x3680	15:0	0x0000	p_gr_p2q0 (R/W)		
	P2 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
13954 R0x3682	15:0	0x0000	p_gr_p2q1 (R/W)		
	P2 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13956 R0x3684	15:0	0x0000	p_gr_p2q2 (R/W)		
	P2 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13958 R0x3686	15:0	0x0000	p_gr_p2q3 (R/W)		
	P2 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13960 R0x3688	15:0	0x0000	p_gr_p2q4 (R/W)		
	P2 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
13962 R0x368A	15:0	0x0000	p_rd_p2q0 (R/W)		
	P2 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13964 R0x368C	15:0	0x0000	p_rd_p2q1 (R/W)		
	P2 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13966 R0x368E	15:0	0x0000	p_rd_p2q2 (R/W)		
	P2 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13968 R0x3690	15:0	0x0000	p_rd_p2q3 (R/W)		
	P2 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13970 R0x3692	15:0	0x0000	p_rd_p2q4 (R/W)		
	P2 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
13972 R0x3694	15:0	0x0000	p_bl_p2q0 (R/W)		
	P2 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13974 R0x3696	15:0	0x0000	p_bl_p2q1 (R/W)		
	P2 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13976 R0x3698	15:0	0x0000	p_bl_p2q2 (R/W)		
	P2 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13978 R0x369A	15:0	0x0000	p_bl_p2q3 (R/W)		
	P2 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13980 R0x369C	15:0	0x0000	p_bl_p2q4 (R/W)		
	P2 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
13982 R0x369E	15:0	0x0000	p_gb_p2q0 (R/W)		
	P2 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
13984 R0x36A0	15:0	0x0000	p_gb_p2q1 (R/W)		
	P2 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13986 R0x36A2	15:0	0x0000	p_gb_p2q2 (R/W)		
	P2 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13988 R0x36A4	15:0	0x0000	p_gb_p2q3 (R/W)		
	P2 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
13990 R0x36A6	15:0	0x0000	p_gb_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14016 R0x36C0	15:0	0x0000	p_gr_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14018 R0x36C2	15:0	0x0000	p_gr_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14020 R0x36C4	15:0	0x0000	p_gr_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14022 R0x36C6	15:0	0x0000	p_gr_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14024 R0x36C8	15:0	0x0000	p_gr_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14026 R0x36CA	15:0	0x0000	p_rd_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14028 R0x36CC	15:0	0x0000	p_rd_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14030 R0x36CE	15:0	0x0000	p_rd_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14032 R0x36D0	15:0	0x0000	p_rd_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14034 R0x36D2	15:0	0x0000	p_rd_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14036 R0x36D4	15:0	0x0000	p_bl_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14038 R0x36D6	15:0	0x0000	p_bl_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14040 R0x36D8	15:0	0x0000	p_bl_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14042 R0x36DA	15:0	0x0000	p_bl_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14044 R0x36DC	15:0	0x0000	p_bl_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14046 R0x36DE	15:0	0x0000	p_gb_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14048 R0x36E0	15:0	0x0000	p_gb_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14050 R0x36E2	15:0	0x0000	p_gb_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14052 R0x36E4	15:0	0x0000	p_gb_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14054 R0x36E6	15:0	0x0000	p_gb_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14080 R0x3700	15:0	0x0000	p_gr_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14082 R0x3702	15:0	0x0000	p_gr_p4q1 (R/W)	N	N
	P4 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14084 R0x3704	15:0	0x0000	p_gr_p4q2 (R/W)	N	N
	P4 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14086 R0x3706	15:0	0x0000	p_gr_p4q3 (R/W)	N	N
	P4 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14088 R0x3708	15:0	0x0000	p_gr_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
14090 R0x370A	15:0	0x0000	p_rd_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14092 R0x370C	15:0	0x0000	p_rd_p4q1 (R/W)		
	P4 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14094 R0x370E	15:0	0x0000	p_rd_p4q2 (R/W)		
	P4 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14096 R0x3710	15:0	0x0000	p_rd_p4q3 (R/W)		
	P4 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14098 R0x3712	15:0	0x0000	p_rd_p4q4 (R/W)		
	P4 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
14100 R0x3714	15:0	0x0000	p_bl_p4q0 (R/W)		
	P4 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14102 R0x3716	15:0	0x0000	p_bl_p4q1 (R/W)		
	P4 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14104 R0x3718	15:0	0x0000	p_bl_p4q2 (R/W)	N	N
	P4 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14106 R0x371A	15:0	0x0000	p_bl_p4q3 (R/W)	N	N
	P4 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14108 R0x371C	15:0	0x0000	p_bl_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
14110 R0x371E	15:0	0x0000	p_gb_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14112 R0x3720	15:0	0x0000	p_gb_p4q1 (R/W)		
	P4 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14114 R0x3722	15:0	0x0000	p_gb_p4q2 (R/W)		
	P4 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14116 R0x3724	15:0	0x0000	p_gb_p4q3 (R/W)		
	P4 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
14118 R0x3726	15:0	0x0000	p_gb_p4q4 (R/W)		
	P4 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				

Table 2: Manufacturer-Specific Register Description (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14208 R0x3780	15:0	0x0000	poly_sc_enable (R/W)		
	15	0x0000	enable 0: Lens Shading Disabled. 1: Lens Shading Enabled.	N	N
	14:0	X	Reserved		
14210 R0x3782	15:0	0x0A5C	poly_origin_c (R/W)		
	Origin of polynomial function: applied as offset to X (col) coordinate of pixel.				
14212 R0x3784	15:0	0x0361	poly_origin_r (R/W)		
	Origin of polynomial function: applied as offset to Y (row) coordinate of pixel.				
14272 R0x37C0	15:0	0x0000	p_gr_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for greenR pixels.				
14274 R0x37C2	15:0	0x0000	p_rd_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for red pixels.				
14276 R0x37C4	15:0	0x0000	p_bl_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for blue pixels.				
14278 R0x37C6	15:0	0x0000	p_gb_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for greenB pixels.				
16082 R0x3ED2	15:0	0xBF46	dac_ld_6_7 (R/W)	N	N
	15	0x0001	ana_sreg_shading_en Analog shading correction enable	N	N
	14	0x0000	ana_sreg_shading_on_shs Analog shading correction applied on shs when set (on shr when cleared)	N	N
	13:9	0x001F	ana_sreg_shading_curr Analog shading correction current	N	N
	8	0x0001	Reserved		
	7:6	0x0001	Reserved		
	5:3	0x0000	Reserved		
	2:1	0x0003	Reserved		
	0	0x0000	Reserved		

Revision History

Rev. E 2/27/13

- I n Table 2, “Manufacturer-Specific Register Description,” on page 17, updated R0x30CE bit 2 and R0x31AE

Rev. D, Production 11/11/11

- Updated analog_gain in Table 1 and Table 2
- Deleted Register 12352: bits 8 and 9 from Table 2
- Added R0x2420, R0x31E0, R0x2410, and R0x2412 to Table 1 and Table 2
- Changed R0x301A:bit 4 to Reserved in Table 2

Rev. C, Preliminary. 10/26/11

- Added R0x2420 to Table 1 and Table 2.
- Added R0x31E0 to Table 1 and Table 2
- Added R0x2410 to Table 1 and Table 2
- Added R0x2412 to Table 1 and Table 2

Rev. B, Preliminary 9/8/11

- Updated to Preliminary
- Updated register tables to Rev. 2 database

Rev. A, Advance 2/15/11

- Initial release

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