1/4-Inch, 5Mp CMOS Digital Image Sensor Die

AR0542 Die Data Sheet

For product data sheets, refer to Aptina's Web site: www.aptina.com

Features

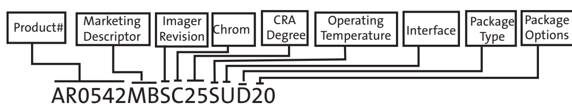
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Support for external LED or xenon flash
- High frame rate preview mode with arbitrary downsize scaling from maximum resolution
- Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning
- Data interfaces: parallel or CCP2-compliant sub-low-voltage differential signaling (sub-LVDS) or single/dual lanes serial mobile industry processor interface (MIPI)
- On-die phase-locked loop (PLL) oscillator
- Bayer pattern down-size scaler
- Integrated color/lens shading correction
- 7.7Kb one-time programmable memory (OTPM) for storing shading correction coefficients of three light sources and module information
- Extended flash duration that is up to start of frame readout
- Superior low-light performance
- On-chip VCM driver

General Physical Specifications

- Die thickness: 200µm ±12µm (Consult factory for other thickness)
- Back side wafer surface of bare silicon
- Typical metal 2 thickness: 1.8kÅ
- Typical metal 3 thickness: 1.8kÅ
- Typical metal 4 thickness: 3.6kÅ
- Metallization composition: 100 percent Cu with Ta barrier
- Typical topside passivation: 2.1kÅ nitride over 5.5kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

Die: AR0542MBSC25SUD20



Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database

- Die outline, see Figure 5 on page 13
- Singulated die size: 5263±25µm x 5072±25µm
- Bond Pad Identification Tables, see pages 8–11

Options	Designator
• Form	
– Die	D
• Testing	
– Standard (level 1) probe	C1

Key Performance Parameters

- Optical format: 1/4-inch (4:3)
- Active imager size: 3.63mm(H)x2.72mm(V): 4.54mm diagonal
- Full resolution: 2592H x 1944V
- Pixel size: 1.4µm x 1.4µm
- Chief ray angle: 25.0°
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Input clock frequency: 6–27 MHz
- Maximum data rate
  - Parallel: 84 Megapixels/second at 84 MHz PIXCLK
  - CCP2: 650 Mbps
  - MIPI: 840 Mbps per lane
- Frame rate
  - Full resolution: 15 fps
  - 1080P: 30 fps (smaller FOV)
  - 720P: 30 fps/60 fps (binning/skipping)
  - VGA: 30 fps/60 fps/115 fps
  - QVGA: 115 fps
- ADC resolution: 10-bit, on-die
- Responsivity: 820V/lux-sec (550nm)
- Dynamic range: 66 dB
- SNR MAX: 36.5 dB
- Supply voltage
  - I/O digital 1.7–1.9V (1.8V nominal), or 2.4–3.1V (2.8V nominal)
  - Digital 1.8V power: 1.7–1.9V (1.8V nominal)
  - Digital core: 1.15–1.25V (1.2V nominal)
  - Analog: 2.6–3.1V (2.8V nominal)
- Power consumption: Full resolution
  - Parallel: 245 mW at 70°C (TYP)
  - MIPI: 215 mW at 70°C (TYP)
  - Standby: 10 µA at 70°C (TYP)
- Operating temperature: –30°C to +70°C (at junction)

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‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Aptina without notice. Products are only warranted by Aptina to meet Aptina's production data sheet specifications.

General Description

The Aptina AR0542 is a 1/4-inch format CMOS active-pixel digital image sensor die with an active pixel array of 2592H x 1944V (2608H x 1960V including border pixels). It incorporates sophisticated on-die camera functions such as windowing, mirroring, column/row binning and skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The AR0542 digital image sensor die features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's standard package. Since the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

These specifications are provided for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The AR0542 imager die has 67 bond pads. Refer to Table 1 and Table 2 on pages 8–11 for a complete list of bond pads and coordinates.

The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 through Figure on page 8 show the AR0542 typical die connections. For low-noise operation, the AR0542 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. Do not use of inductance filters on the power supplies or output signals without consulting Aptina Applications Engineering.

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The AR0542 includes an internal regulator to supply 1.2V to digital core block and an internal PLL. Also, the power for the internal PLL can be supplied by either internal PLL regulator (in this case, no external connection to the VDD_PLL) or connection to REG_OUT (VDD and VDD_PLL are tied together).

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

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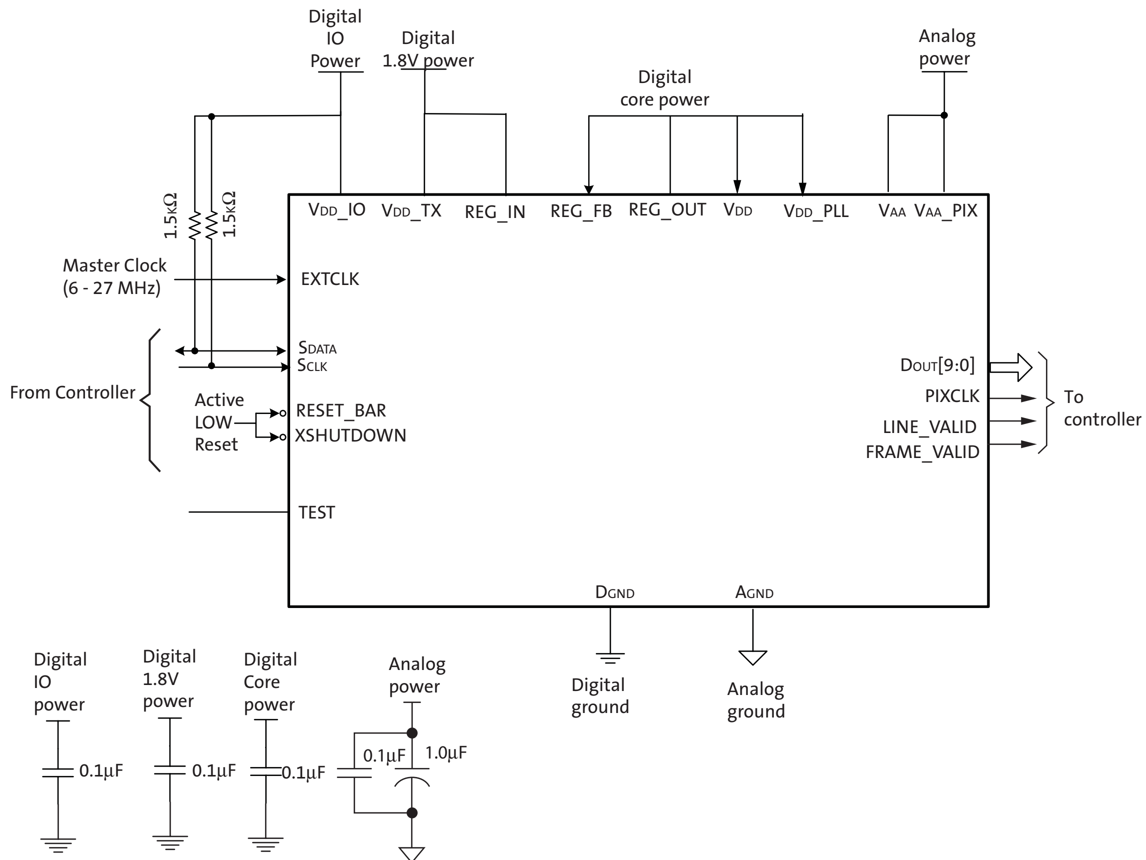
Typical Connections

Figure 1 below to Figure 3 on page 6 show typical connection schematics for the AR0542 die.

Figure 1: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
3. VDD_IO can be either 1.8V(nominal) or 2.8V(nominal). If VDD_IO is 1.8V, VDD_IO can be tied to Digital 1.8V Power.
4. VAA and VAA_PIX must be tied together.
5. VDD and VDD_PLL must be tied together.
6. The serial interface output pads can be left unconnected if the parallel output interface is used.
7. Aptina recommends that 0.1µF decoupling capacitor for analog power supply and 0.1µF decoupling capacitor for other power supplies. Actual values and results may vary depending on layout and design considerations.
8. TEST can be tied to DGND (Device ID address=0x20) or VDD_IO (Device ID address=0x6C).
9. VDD _TX and REG_IN must be tied together.
10. Aptina recommends that RESET_BAR and XSHUTDOWN be tied together.
11. The frequency range for EXTCLK must be 6-27 MHz.
12. VPP, which can be used during the module manufacturing process, is not shown in Figure 1. This pad is left unconnected during normal operation.
13. VCM_ISINK and VCM_GND, which can be used for internal VCM AF driver, are not shown in Figure 1. VCM_ISINK must be tied to the VCM actuator and VCM_GND must be tied to the DGND when the internal VCM is used. These pads are left unconnected if the internal VCM driver is not used.

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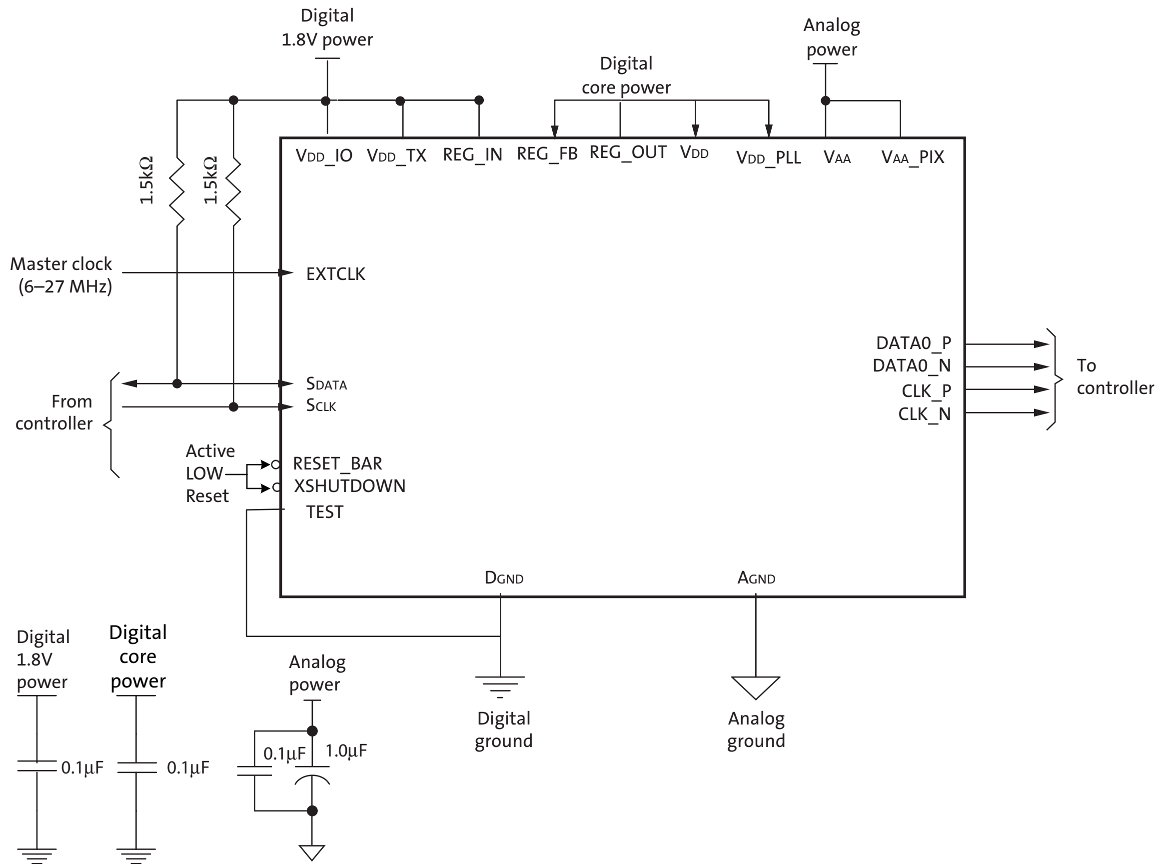
14. The GPI[3:0] pins, which can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_BAR, SADDR, STANDBY) to be dynamically controlled, are not shown in Figure 1.
15. The FLASH, which can be used for flash control, is not shown in Figure 1.

Figure 2: Typical Configuration: Serial CCP2 Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. Aptina recommends a resistor value of 1.5KΩ, but a greater value may be used for slower two-wire speed. This pull-up resistor is not required if the controller drivers a valid logic level on SCLK at all times.
3. VAA and VAA _PIX must be tied together.
4. VDD AND VDD_PLL must be tied together.
5. The parallel interface output pads can be left unconnected if the serial output interface is used.
6. Aptina recommends that 0.1µF decoupling capacitor for analog power supply and 0.1µF decoupling capacitor for other power supplies. Actual values and results may vary depending on layout and design considerations.
7. TEST must be tied to DGND.
8. VDD _TX and REG_IN must be tied together.
9. Aptina recommends that RESET_BAR and XSHUTDOWN be tied together.
10. The frequency range for EXTCLK must be 6-27 MHz.
11. VPP, which can be used during the module manufacturing process, is not shown in Figure 2. This pad is left unconnected during normal operation
12. VCM_ISINK and VCM_GND, which can be used for internal VCM AF driver, are not shown in Figure 2. VCM_ISINK must be tied to the VCM actuator and VCM_GND must be tied to the DGND when the internal VCM is used. These pads are left unconnected if the internal VCM driver is not used.

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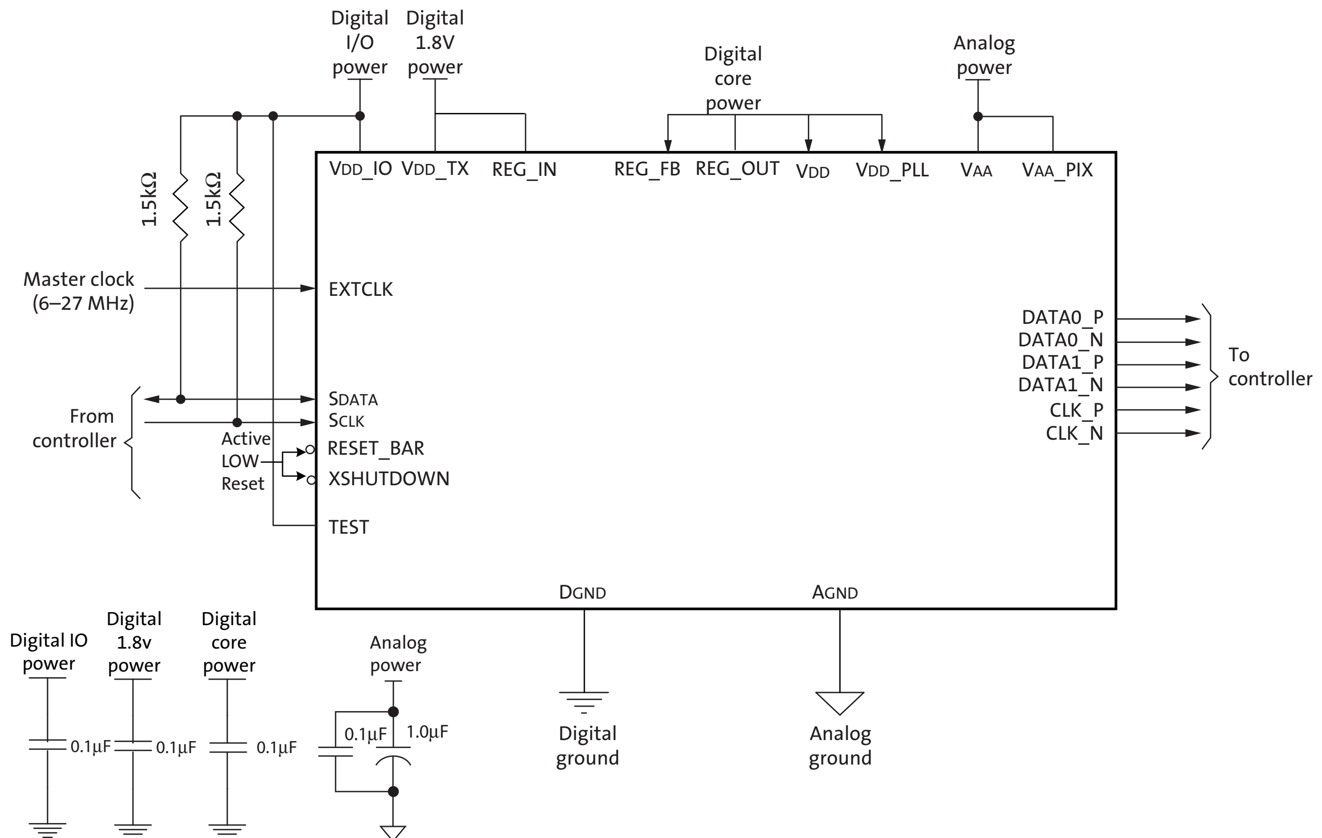
13. The GPI[3:0] pins, which can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_BAR, SADDR, STANDBY) to be dynamically controlled, are not shown in Figure 2.
14. The FLASH, which can be used for flash control, is not shown in Figure 2.

Figure 3: Typical Configuration: Serial Dual-Lane MIPI Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5KΩ, but a greater value may be used for slower two-wire speed. This pull-up resistor is not required if the controller drivers a valid logic level on SCLK at all times.
3. VAA and VAA _PIX must be tied together.
4. VDD and VDD _PLL must be tied together.
5. VDD_IO can be either 1.8V(nominal) or 2.8V(nominal). If VDD_IO is 1.8V, VDD_IO can be tied to the Digital 1.8V Power.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. If single lane MIPI is used, DATA1_P and DATA1_N can be left unconnected.
8. Aptina recommends that 0.1µF decoupling capacitor ffor analog power supply and 0.1µF decoupling capacitor for other power supplies. Actual values and results may vary depending on layout and design considerations.
9. TEST must be tied to VDD _IO.
10. VDD _TX and REG_IN must be tied together.
11. Aptina recommends that RESET_BAR and XSHUTDOWN be tied together.
12. The frequency range for EXTCLK must be 6-27MHz.
13. VPP, which can be used during the module manufacturing process, is not shown in Figure 3. This pad is left unconnected during normal operation
14. VCM_ISINK and VCM_GND, which can be used for internal VCM AF driver, are not shown in Figure 3. VCM_ISINK must be tied to the VCM actuator and VCM_GND must be tied to the DGND when the internal VCM is used. These pads are left unconnected if the internal VCM driver is not used.

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15. The GPI[3:0] pins, which can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_BAR, SADDR, STANDBY) to be dynamically controlled, are not shown in Figure 3.
16. The FLASH, which can be used for flash control, is not shown in Figure 3.

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Bond Pad Identification Tables

Table 1: Bond Pad Location and Identification from Center of Pad 1
To ensure proper device operation, all power supply bond pads must be bonded

Pad Number	Pad Name	"X" Microns	"Y" Microns
1	DGND4	0.0000	0.0000
2	VDD _TX	150.1200	0.0000
3	DATA_1N	329.7600	0.0000
4	DATA_1P	649.0800	0.0000
5	DATA_0N	1011.9600	0.0000
6	DATA_0P	1331.2800	0.0000
7	CLK_N	1580.4000	0.0000
8	CLK_P	1899.7200	0.0000
9	EXTCLK	2083.6800	0.0000
10	VDD1	2233.8000	0.0000
11	DGND1	2383.9200	0.0000
12	GPI0	2534.0400	0.0000
13	GPI1	2684.1600	0.0000
14	RESET_BAR	2834.2800	0.0000
15	LINE_VALID	2998.6800	0.0000
16	FRAME_VALID	3199.4400	0.0000
17	VDD _IO1	3349.5600	0.0000
18	PIXCLK	3499.6800	0.0000
19	DGND5	3649.8000	0.0000
20	DOUT9	3799.9200	0.0000
21	DOUT8	3982.5600	0.0000
22	GPI2	4140.3600	0.0000
23	DOUT7	4290.4800	0.0000
24	DOUT6	4473.1200	0.0000
25	VDD _IO2	4623.2400	0.0000
26	DOUT5	4773.3600	0.0000
27	DGND6	4923.4800	0.0000
28	DOUT 4	5014.0400	-471.8400
29	DGND2	5014.0400	-621.9600
30	VDD 2	5014.0400	-772.0800
31	DOUT 3	5014.0400	-922.2000
32	VDD_IO3	5014.0400	-1072.3200
33	DOUT2	5014.0400	-1222.4400
34	DGND7	5014.0400	-1372.5600
35	DOUT1	5014.0400	-1527.1200
36	DOUT0	5014.0400	-1700.8800
37	VCM_GND	5014.0400	-1898.2850
38	VCM_ISINK	5014.0400	-2265.9800
39	AGND0	5014.0400	-2421.8400
40	DNU	5014.0400	-2532.0000
41	VAA 0	5014.0400	-2642.1600
42	DNU	5014.0400	-2752.3200
43	VAA1	5014.0400	-2862.4800

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Table 1: Bond Pad Location and Identification from Center of Pad 1 (continued)
To ensure proper device operation, all power supply bond pads must be bonded

Pad Number	Pad Name	"X" Microns	"Y" Microns
44	VAA 2	5014.0400	-2992.8000
45	VAA 3	5014.0400	-4606.3200
46	AGND1	5014.0400	-4736.6400
47	AGND2	5014.0400	-4866.9600
48	AGND3	-88.1600	-4869.8400
49	VAA_PIX0	-88.1600	-4739.5200
50	VAA_PIX1	-88.1600	-4609.2000
51	VPP	-88.1600	-4448.2800
52	REG_IN1	-88.1600	-4283.7600
53	XSHUTDOWN	-88.1600	-4133.6400
54	VDD_IO0	-88.1600	-3983.5200
55	SDATA	-88.1600	-3833.4000
56	SCLK	-88.1600	-3683.2800
57	DGND8	-88.1600	-3533.1600
58	FLASH	-88.1600	-3383.0400
59	TEST	-88.1600	-3220.8000
60	GPI3	-88.1600	-3070.6800
61	DGND3	-88.1600	-2920.5600
62	REG_FB	-88.1600	-2667.6650
63	REG_OUT	-88.1600	-2517.6650
64	REG_IN0	-88.1600	-2230.3850
65	VDD_PLL	-88.1600	-2080.3850
66	VDD0	-88.1600	-739.5650
67	DGND0	-88.1600	-530.7650

Notes:
1. Reference to center of each bond pad from center.
2. For normal device operation, TEST must be connected to:
   - DGND for serial CCP2 interface
   - VDD_IO for serial MIPI interface
3. DNU = do not use. See “Bonding Instructions” on page 2.

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Table 2: Bond Pad Location and Identification from Center of Die (0,0)
To ensure proper device operation, all power supply bond pads must be bonded

Pad Number	Pad Name	"X" Microns	"Y" Microns
1	DGND4	-2462.9400	2455.6000
2	VDD _TX	-2312.8200	2455.6000
3	DATA_1N	-2133.1800	2455.6000
4	DATA_1P	-1813.8600	2455.6000
5	DATA_0N	-1450.9800	2455.6000
6	DATA_0P	-1131.6600	2455.6000
7	CLK_N	-882.5400	2455.6000
8	CLK_P	-563.2200	2455.6000
9	EXTCLK	-379.2600	2455.6000
10	VDD1	-229.1400	2455.6000
11	DGND1	-79.0200	2455.6000
12	GPI0	71.1000	2455.6000
13	GPI1	221.2200	2455.6000
14	RESET_BAR	371.3400	2455.6000
15	LINE_VALID	535.7400	2455.6000
16	FRAME_VALID	736.5000	2455.6000
17	VDD _IO1	886.6200	2455.6000
18	PIXCLK	1036.7400	2455.6000
19	DGND5	1186.8600	2455.6000
20	DOUT9	1336.9800	2455.6000
21	DOUT8	1519.6200	2455.6000
22	GPI2	1677.4200	2455.6000
23	DOUT7	1827.5400	2455.6000
24	DOUT6	2010.1800	2455.6000
25	VDD _IO2	2160.3000	2455.6000
26	DOUT5	2310.4200	2455.6000
27	DGND6	2460.5400	2455.6000
28	DOUT 4	2551.1000	1983.7600
29	DGND2	2551.1000	1833.6400
30	VDD 2	2551.1000	1683.5200
31	DOUT 3	2551.1000	1533.4000
32	VDD_IO3	2551.1000	1383.2800
33	DOUT2	2551.1000	1233.1600
34	DGND7	2551.1000	1083.0400
35	DOUT1	2551.1000	928.4800
36	DOUT0	2551.1000	754.7200
37	VCM_GND	2551.1000	557.3150
38	VCM_ISINK	2551.1000	189.6200
39	AGND0	2551.1000	33.7600
40	DNU	2551.1000	-76.4000
41	VAA 0	2551.1000	-186.5600
42	DNU	2551.1000	-296.7200
43	VAA1	2551.1000	-406.8800
44	VAA 2	2551.1000	-537.2000

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Table 2: Bond Pad Location and Identification from Center of Die (0,0) (continued)
To ensure proper device operation, all power supply bond pads must be bonded

Pad Number	Pad Name	"X" Microns	"Y" Microns
45	VAA 3	2551.1000	-2150.7200
46	AGND1	2551.1000	-2281.0400
47	AGND2	2551.1000	-2411.3600
48	AGND3	-2551.1000	-2414.2400
49	VAA _PIX0	-2551.1000	-2283.9200
50	VAA _PIX1	-2551.1000	-2153.6000
51	VPP	-2551.1000	-1992.6800
52	REG_IN1	-2551.1000	-1828.1600
53	XSHUTDOWN	-2551.1000	-1678.0400
54	VDD _IO0	-2551.1000	-1527.9200
55	SDATA	-2551.1000	-1377.8000
56	SCLK	-2551.1000	-1227.6800
57	DGND8	-2551.1000	-1077.5600
58	FLASH	-2551.1000	-927.4400
59	TEST	-2551.1000	-765.2000
60	GPI3	-2551.1000	-615.0800
61	DGND3	-2551.1000	-464.9600
62	REG_FB	-2551.1000	-212.0650
63	REG_OUT	-2551.1000	-62.0650
64	REG_IN0	-2551.1000	225.2150
65	VDD _PLL	-2551.1000	375.2150
66	VDD0	-2551.1000	1716.0350
67	DGND0	-2551.1000	1924.8350

Notes:
1. Reference to center of each bond pad frame center.
2. For normal device operation, TEST must be connected to:
   - DGND for serial CCP2 interface
   - VDD_IO for serial MIPI interface
3. DNU = do not use. See "Bonding Instructions" on page 2.

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Spectral Characteristics

Figure 4: Chief Ray Angle (CRA) vs. Image Height

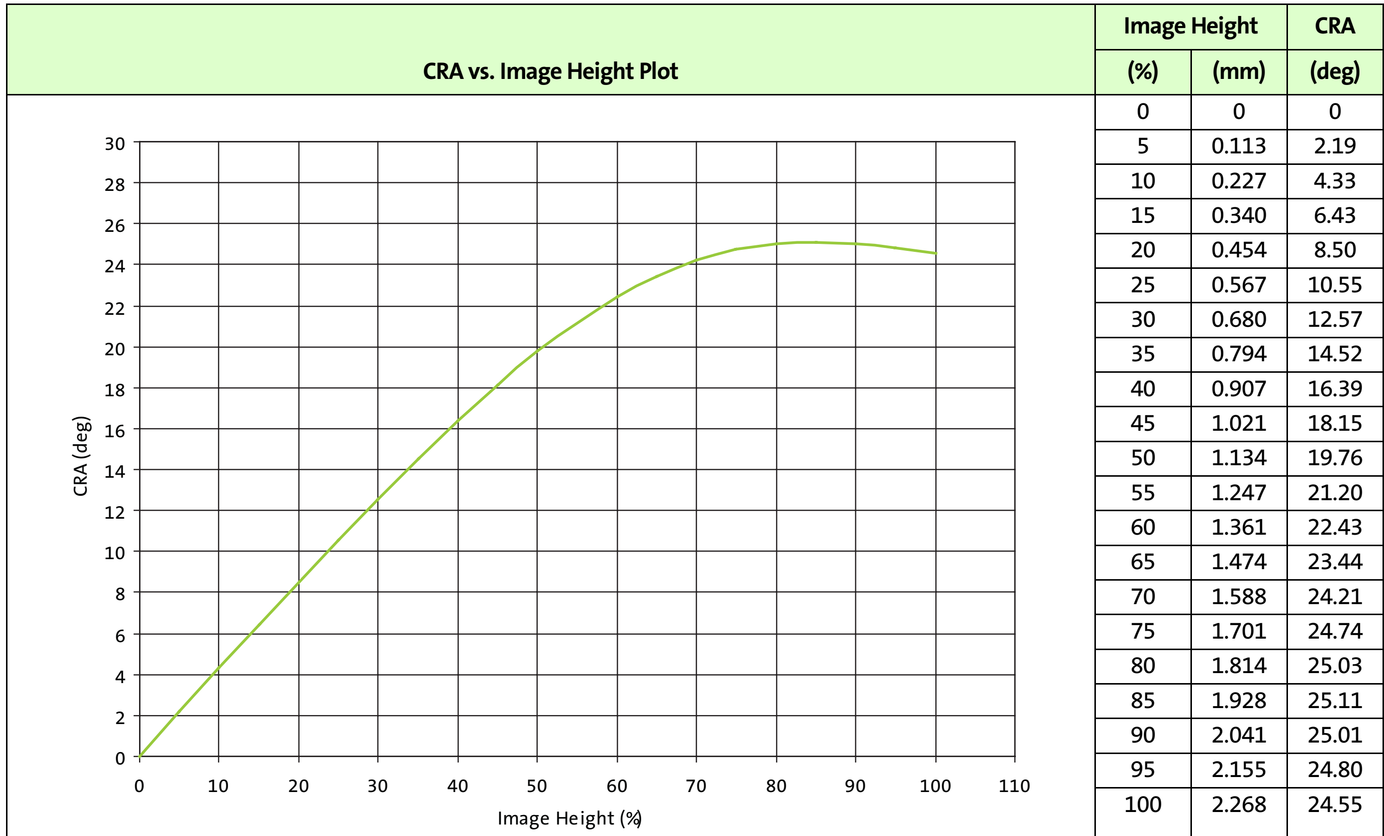

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.113	2.19
10	0.227	4.33
15	0.340	6.43
20	0.454	8.50
25	0.567	10.55
30	0.680	12.57
35	0.794	14.52
40	0.907	16.39
45	1.021	18.15
50	1.134	19.76
55	1.247	21.20
60	1.361	22.43
65	1.474	23.44
70	1.588	24.21
75	1.701	24.74
80	1.814	25.03
85	1.928	25.11
90	2.041	25.01
95	2.155	24.80
100	2.268	24.55

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Die Features

Figure 5: Die Outline (Top View)

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

+Y
-X +X
-Y

67
66

28 29 30 31 32 33 34 35 36 37

First clear active pixel
(col. 44; row 43)

Pixel Array

65
64

38

Die center
(0µm, 0µm)

63
62

39 40 41 42 43 44

Optical center
from the die center
(-46.50µm, -80.08µm)

61 60 59 58 57 56 55 54 53 52 51 50 49 48

Last clear active pixel
(col 2,651; row 2,002)

45 46 47

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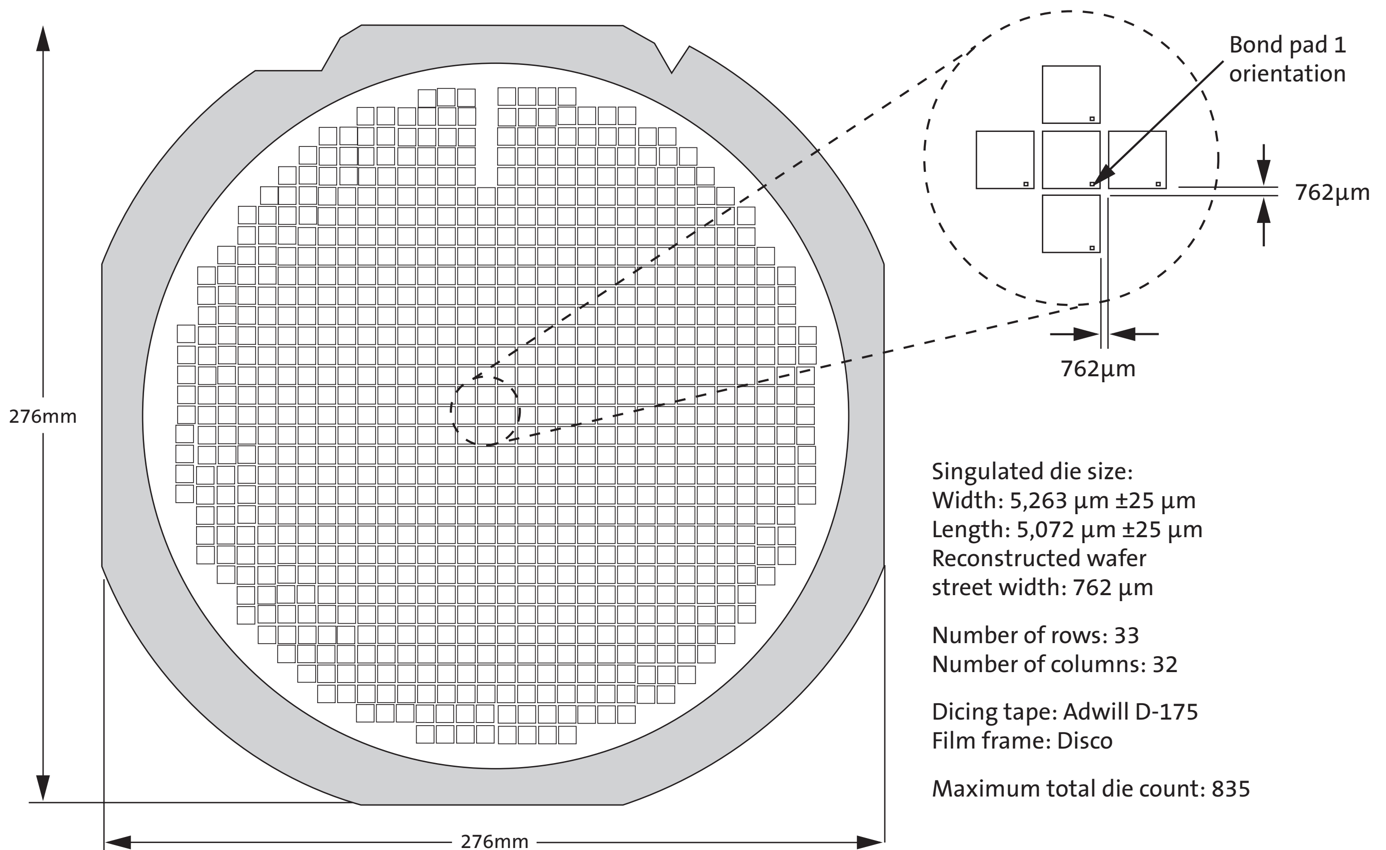
Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) *Width (X dimension):* *Length (Y dimension):*	 5,263 ±25µm 5,072 ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	130.32µm (5.131 mil)
Optical array offset *Optical center from die center:* *Optical center from center of pad 1:*	 X = –46.50µm, Y = –80.08µm X = 2,416.44µm, Y = –2,535.68µm
First clear active pixel (col. 44, row 43) *From die center:* *From center of pad 1:*	 X = 1,778.46µm, Y = 1,291.08µm X = 4,241.40µm, Y = –1,164.51µm
Last clear active pixel (col. 2,651; row 2,002) *From die center:* *From center of pad 1:*	 X = –1871.46µm, Y = –1,451.24µm X = 591.47µm, Y = –3,906.84µm

Figure 6: Die Orientation in Reconstructed Wafer



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Revision History

Rev. B **10/6/11**

- Updated OTPM size to 7.7Kb in “Features” on page 1

Rev. A **6/21/11**

- Initial release

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