# 1-Inch 14Mp CMOS Digital Image Sensor

## AR1411HS Data Sheet

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

## Features

- 2.86µm pixel size with Aptina DR-Pix™ technology
- 1/80 sec frame readout time, 1-inch optical size, 14M pixel imager
- 60 fps continuous readout in full resolution mode
- Multiple operation modes including: HD60_3:2 at 60fps, HD120_16:9 at 120fps, Hi-Speed at 400fps, and Super Hi-Speed at 1200fps
- Low noise, low power consumption high speed differential serial video output (HiSPI™)
- External master clock frequency 29.16 MHz

## Applications and Scope

- AR1411HS is an imager with 1-inch optical format, 14M pixel resolution, and 1/80 sec frame readout speed in still mode for digital camera applications.
- The operation modes of the AR1411HS are highly specified for customer's requirements. Although many combinations of operation settings are possible by various register settings, only the imager operational modes specified in this document are guaranteed.

## General Description

The AR1411HS is a CMOS image sensor with a full resolution high speed capable sensor in various readout operation modes for digital camera applications.

## Ordering Information

**Table 1: Available Part Number**

| Part Number | Description |
|---|---|
| AR1411HSSC10SHAA0E | 124CLCC, 10.3deg CRA |

**Table 2: Key Performance Parameters**

| Parameter | | Value |
|---|---|---|
| Optical format | | 15.8mm diagonal (3:2) |
| | | 13.5mm x 8.8mm |
| Pixel size | | 2.86mm x 2.86mm with DR-Pix™ |
| Entire array format | | 3984 (H) x 2712 (V) |
| Primary modes | | Full resolution: 4620 x 3048 at 1/80 |
| | | HD60_3:2: 4620 x 2048 at 60fps |
| | | HD120_16:9: 4620 x 2048 at 120fps |
| | | Hi-Speed: 4620 x 586 at 400fps |
| | | Super Hi-Speed: 4620 x 170 at 1200fps |
| Chief ray angle | | 10.3 degree |
| Color filter array | | RGB Bayer pattern |
| Shutter type | | Electronic rolling shutter (ERS) |
| Master clock | | 29.16MHz |
| Control interface | | 2-wire serial (Max 400kHz) |
| Outputs | | Data: 24 lanes (700Mbps/lane) |
| | | Clock: 6 lanes (350MHz DDR) |
| ADC resolution | | 13-bit, on-chip ADC (12bit output) |
| Analog gain | | 1x, 2x, 4x, and 8x |
| Responsivity | | 20.5ke-/lux*sec |
| Dynamic range | | 79dB |
| SNRMAX | | 40dB |
| Supply voltage | $V_{DD}$ | 1.7-1.9V, typ. 1.8V |
| | $V_{AA}$ | 2.9-3.1V, typ. 3.0V |
| | $V_{AA}1.8$ | 1.7-1.9V, typ. 1.8V |
| | $V_{AA\_PIX}$ | 2.9-3.1V, typ. 3.0V |
| | $V_{DD\_HiSPi}$ | 0.35-0.45V, typ. 0.4V |
| | $V_{DD\_PLL}$ | 2.7-2.9V, typ. 2.8V |
| Package | | 124pin CLCC |
| | | 23.6mm x 22mm x 2.6mm |



Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Aptina without notice. Products are only warranted by Aptina to meet Aptina's production data sheet specifications.

## Table of Contents




Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## List of Figures





Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## List of Tables




Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Functional Overview and Operation Modes

The AR1411HS is a 14-megapixel image sensor designed using Aptina's latest 2.86 m pixel technology. Aptina's Dual Conversion Gain DR-Pix™ pixel technology, which enables the pixel level selection of the high/low sensitivity control, is implemented in the sensor.

This document describes the sub-resolution schemes, which enable the special video modes, that is, HD120_16:9_SLV mode, HD60_3:2_SLV mode, HD60_16:9_LP mode, HD60_3:2 mode, Pre-Flash A mode, Pre-Flash B mode, EVF mode, Hi-Speed mode, and Super Hi-Speed mode, as shown in Table 3. The operation timings are designed based on an external clock at 29.16 MHz.

Another feature of the AR1411HS is context mode change by a macro control register, which enables the very quick mode change from video mode to still image capture mode, minimizing shutter lag.

**Table 1: Operation Mode Definitions (EXTCLK = 29.16 MHz)**

| Operating Mode | Sub Res | | Image Area Size | | Frame Cycle (mclks) | Row Cycle (mclks) | | Frame Cycle (rows) | | Frame Rate | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | H | V | H | V | | Total | Effect. | Total | Effect. | w/ VB | w/o VB |
| Full Resolution | Full | Full | 4620 | 3084 | 972972 | 234 | 198 | 4158 | 3084 | 59.94 | 80.81 |
| HD_120_16:9_SLV | Full | Full | 4620 | 2052 | 486486 | 234 | 198 | 2079 | 2052 | 119.88 | - |
| HD_60_3:2_SLV | Full | Full | 4620 | 3084 | 972972 | 234 | 198 | 4158 | 3084 | 59.94 | - |
| HD_60_16:9_LP | Full | Full | 4620 | 2604 | 972972 | 364 | 198 | 2673 | 2604 | 59.94 | - |
| HD_60_3:2 | Full | Full | 4620 | 3084 | 972972 | 308 | 198 | 3159 | 3084 | 59.94 | - |
| Hi-Speed | Full | Skip 2/5 | 4620 | 1645 | 145080 | 234 | 198 | 620 | 586 | 401.99 | - |
| Super Hi-Speed | Full | Skip 1/5 | 4620 | 850 | 47736 | 234 | 198 | 204 | 170 | 1221.72 | - |
| Pre-flash A | Skip 1/3 | Skip 1/15 | 4620 | 3084 | 486486 | 462 | 66 | 1053 | 204 | 119.88 | 618.79 |
| Pre-flash B | Skip 1/3 | Skip 1/45 | 4620 | 3084 | 486486 | 462 | 66 | 1053 | 68 | 119.88 | 1856.38 |
| EVF | Full | Skip 2/3 | 4620 | 3084 | 972972 | 364 | 198 | 2673 | 2056 | 59.94 | - |



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Signal Descriptions

## Pin Assignment

Table 4 below shows the pin names and the pin assignment in a package. Figure 2 on page 4 shows the pin connections.

**Table 2: Package Pin List**

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|---|---|---|---|---|---|
| 1 | VDD_HiSPi | 43 | ATEST_BOT | 85 | DATA6_N |
| 2 | DATA1_N | 44 | VRS_HI | 86 | DATA4_P |
| 3 | DATA1_P | 45 | VRST_LO | 87 | DATA4_N |
| 4 | DATA3_N | 46 | VTX_LO2 | 88 | D_CLK0_P |
| 5 | DATA3_P | 47 | VTX_LO1 | 89 | D_CLK0_N |
| 6 | D_CLK1_N | 48 | VDCG_LO | 90 | DATA2_P |
| 7 | D_CLK1_P | 49 | VDCG_HI2 | 91 | DATA2_N |
| 8 | DATA5_N | 50 | VDCG_HI1 | 92 | DATA0_P |
| 9 | DATA5_P | 51 | VAA_PIX_BOOSTER | 93 | DATA0_N |
| 10 | DATA7_N | 52 | ATEST_TOP | 94 | VDD_HiSPi |
| 11 | DATA7_P | 53 | VREF1_TOP | 95 | DGND |
| 12 | DATA9_N | 54 | VREF2_TOP | 96 | VDD |
| 13 | DATA9_P | 55 | VAA1.8 | 97 | VDD |
| 14 | DATA11_N | 56 | VAA_PIX | 98 | DGND |
| 15 | DATA11_P | 57 | AGND | 99 | VDD |
| 16 | D_CLK3_N | 58 | VAA | 100 | VAA |
| 17 | D_CLK3_P | 59 | AGND | 101 | AGND |
| 18 | DATA13_N | 60 | DGND | 102 | VAA_PIX |
| 19 | DATA13_P | 61 | VDD | 103 | SCLK |
| 20 | DATA15_N | 62 | DGND | 104 | SDATA |
| 21 | DATA15_P | 63 | VDD_HiSPi | 105 | DGND |
| 22 | DATA17_N | 64 | DATA22_P | 106 | PHY_STABLE |
| 23 | DATA17_P | 65 | DATA22_N | 107 | TEST |
| 24 | DATA19_N | 66 | DATA20_P | 108 | TRIGGER |
| 25 | DATA19_P | 67 | DATA20_N | 109 | VDD_PLL |
| 26 | D_CLK5_N | 68 | D_CLK4_P | 110 | VDD |
| 27 | D_CLK5_P | 69 | D_CLK4_N | 111 | EXTCLK2 |
| 28 | DATA21_N | 70 | DATA18_P | 112 | EXTCLK |
| 29 | DATA21_P | 71 | DATA18_N | 113 | DGND |
| 30 | DATA23_N | 72 | DATA16_P | 114 | RESET_B |
| 31 | DATA23_P | 73 | DATA16_N | 115 | RESYNC_CODE_VALID |
| 32 | VDD_HiSPi | 74 | DATA14_P | 116 | DSPARE1 |
| 33 | DGND | 75 | DATA14_N | 117 | VAA_PIX |
| 34 | VDD | 76 | DATA12_P | 118 | AGND |
| 35 | DGND | 77 | DATA12_N | 119 | VAA |
| 36 | AGND | 78 | D_CLK2_P | 120 | VDD |
| 37 | VAA | 79 | D_CLK2_N | 121 | DGND |
| 38 | AGND | 80 | DATA10_P | 122 | VDD |
| 39 | VAA_PIX | 81 | DATA10_N | 123 | VDD |

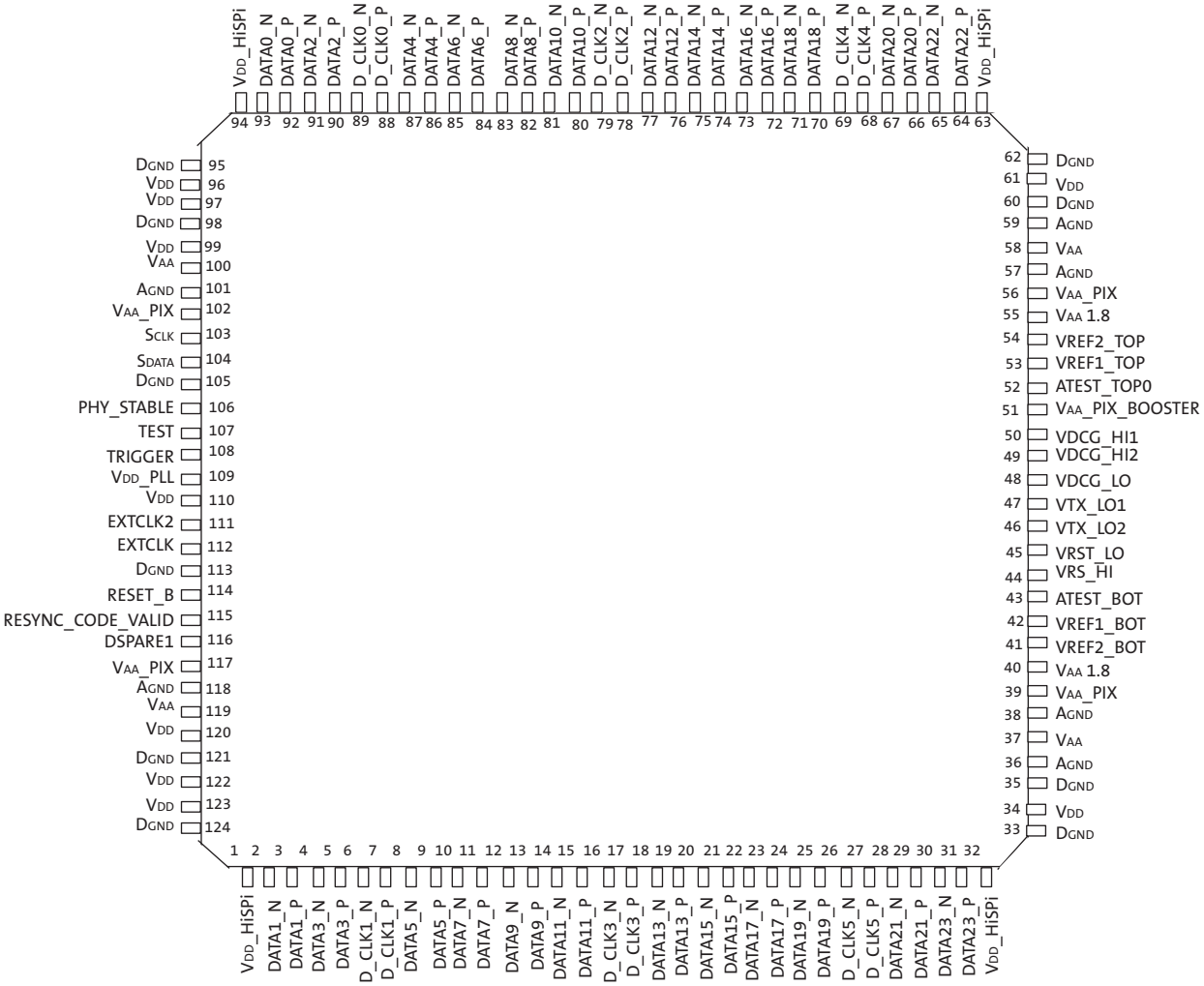


Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Table 2: Package Pin List (continued)**

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|---|---|---|---|---|---|
| 40 | VAA1.8 | 82 | DATA8_P | 124 | DGND |
| 41 | VREF2_BOT | 83 | DATA8_N | | |
| 42 | VREF1_BOT | 84 | DATA6_P | | |

**Figure 1: Pin Assignment (Top View)**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 2: Typical Pin Connection**

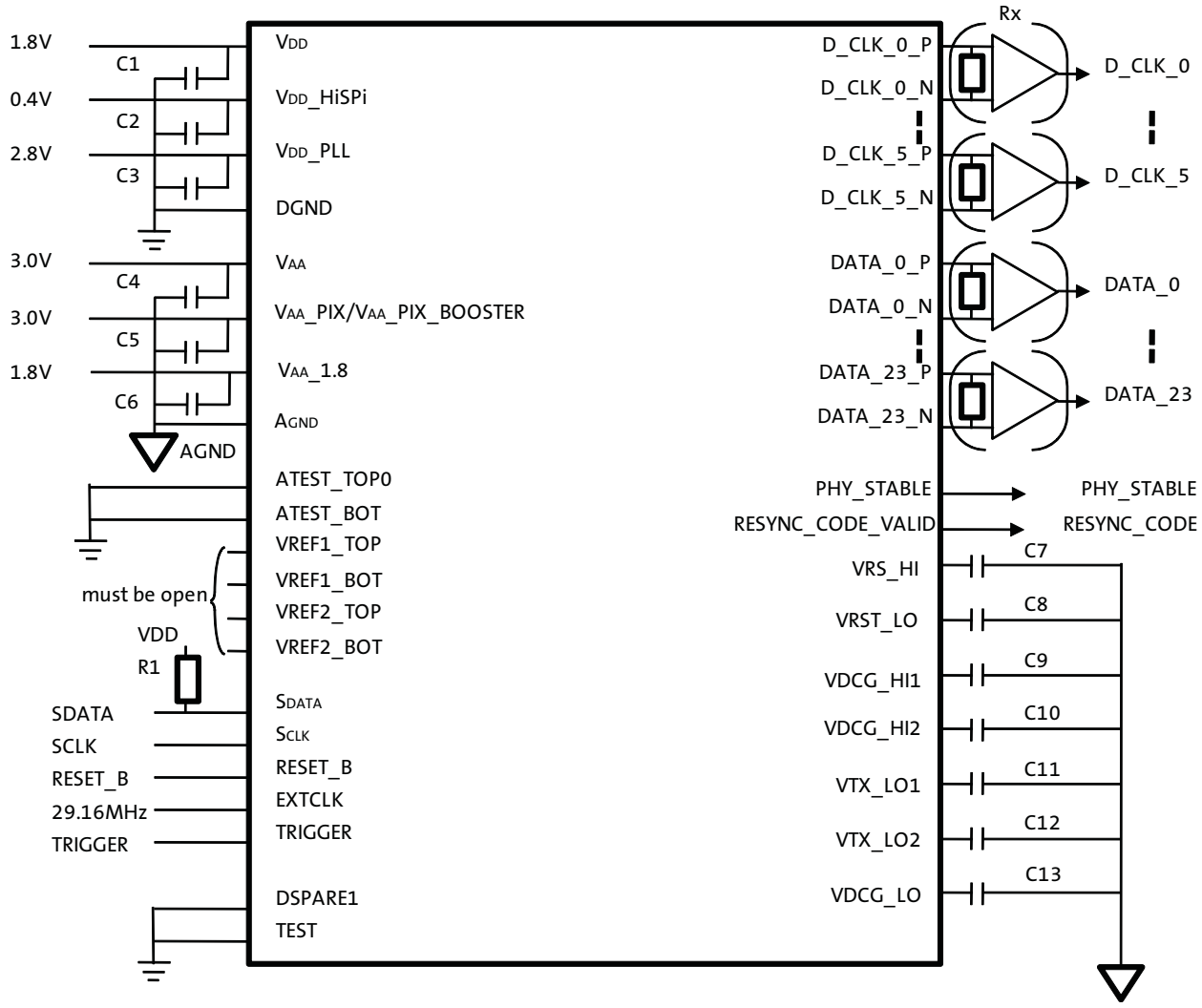



**Table 3: Capacitance and Resistor Values**

| | Values | | Values | | Values |
|---|---|---|---|---|---|
| C1 | 0.1µF(ceramic) +10µF | C2 | 0.1µF(ceramic) +10µF | C3 | 0.1µF(ceramic) +10µF |
| C4 | 0.1µF(ceramic) +10µF | C5 | 0.1µF(ceramic) +10µF | C6 | 0.1µF(ceramic) |
| C7 | 0.1µF(ceramic) | C8 | 0.1µF(ceramic) | C9 | 0.1µF(ceramic) |
| C10 | 0.1µF(ceramic) | C11 | 0.1µF(ceramic) | C12 | 0.1µF(ceramic) |
| C13 | 0.1µF(ceramic) | R1 | 1.5kΩ | | |



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Signal Descriptions

## Power Supplies and Ground

**Table 4: Power Supplies and Ground**

| Name | Description | DC Value (V) | | | Ripple (mV) | Comments |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| VDD | Digital power supply | 1.7 | 1.8 | 1.9 | - | |
| VAA | Analog power supply | 2.9 | 3.0 | 3.1 | 10 | Must be separated from VAA_PIX |
| VAA1.8 | Analog power supply (1.8V) | 1.7 | 1.8 | 1.9 | 10 | |
| VAA_PIX | Pixel power supply | 2.9 | 3.0 | 3.1 | 10 | |
| VDD_HiSPi | HiSPi power supply | 0.35 | 0.4 | 0.45 | - | |
| VDD_PLL | PLL power supply | 2.7 | 2.8 | 2.9 | - | |
| DGND | Digital ground | - | | | - | |
| AGND | Analog ground | - | | | - | |

## Absolute Ratings

**Table 5: Absolute Maximum Ratings**

| Name | Definition | Absolute Max Value |
|---|---|---|
| Supply | | (V) |
| VDD | Digital power supply | 2.85 |
| VAA | Analog power supply | 4.8 |
| VAA_PIX, VAA_PIX_BOOSTER | Pixel power supply | 4.8 |
| VDD_HiSPi | HiSPi power supply | 0.675 |
| VDD_PLL | PLL power supply | 4.35 |
| Current | | (mA) |
| $I_{Supply}$ | Maximum supply to power input | 300 |
| $I_{GND}$ | Maximum negative supply to GND | -100 |

Note: ISUPPLY and IGND are defined by input to each pin.

**Table 6: Absolute Minimum and Maximum Temperature Ratings (°C)**

| Symbol | Definition | Min | Max |
|---|---|---|---|
| $t_{OP}$ | Operating temperature | -10 | 70 |
| $t_{PE}$ | Performing temperature | -10 | 60 |
| $t_{ST}$ | Storage temperature | -30 | 80 |

Note: All temperature is defined by chip surface.



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Bias/Analog Test Signals

**Table 7: Bias/Analog Test Signals**

| Name | Type | Description |
|---|---|---|
| VRS_HI | Decoupling | External noise decoupling. Internal analog voltage. |
| VRST_LO1 | Decoupling | External noise decoupling. Internal analog voltage. |
| VTX_LO1 | Decoupling | External noise decoupling. Internal analog voltage. |
| VTX_LO2 | Decoupling | External noise decoupling. Internal analog voltage. |
| VDCG_HI1 | Decoupling | External noise decoupling. Internal analog voltage. |
| VDCG_HI2 | Decoupling | External noise decoupling. Internal analog voltage. |
| VDCG_LO | Decoupling | External noise decoupling. Internal analog voltage. |
| ATEST_TOP | Test | Reserved for test. Tied to DGND. |
| ATEST_BOT | Test | Reserved for test. Tied to DGND. |
| VREF1_TOP | Test | Reserved for test. Must be opened. |
| VREF1_BOT | Test | Reserved for test. Must be opened. |
| VREF2_TOP | Test | Reserved for test. Must be opened. |
| VREF2_BOT | Test | Reserved for test. Must be opened. |

## Digital Signals

Voltage levels for digital input are:

LOW: –0.3V to 0.3V

HIGH: (VDD – 0.3V)to (VDD + 0.3V)

**Table 8: Digital Signals**

| Name | I/O Type | Description | Input Capacitance (Typical) |
|---|---|---|---|
| DATA[23:0]_P | O | Differential data of channel [23:0], HiSPi, positive | - |
| DATA[23:0]_N | O | Differential data of channel [23:0], HiSPi, negative | - |
| D_CLK[5:0]_P | O | Differential clock[5:0], DDR, HiSPi, positive | - |
| D_CLK[5:0]_N | O | Differential clock[5:0], DDR, HiSPi, negative | - |
| EXTCLK | I | External clock input. Typical 29.16 MHz. | 2.6 pF |
| RESET_B | I | Hard reset. Low active. | 6 pF |
| SCLK | I | Serial I/F clock. | 6 pF |
| SDATA | I/O | Serial I/F data input/output | 6 pF |
| TRIGGER | I | Trigger input for starting exposure or starting readout in Full Resolution mode. Also controls operation start timing in video modes. | 7.9 pF |
| PHY_STABLE | O | Output signal that indicates the status of HiSPi PHY. | |
| TEST | I | Reserved for test. Must be tied to DGND. | |
| DSPARE1 | I | Reserved for test. Must be tied to DGND | |

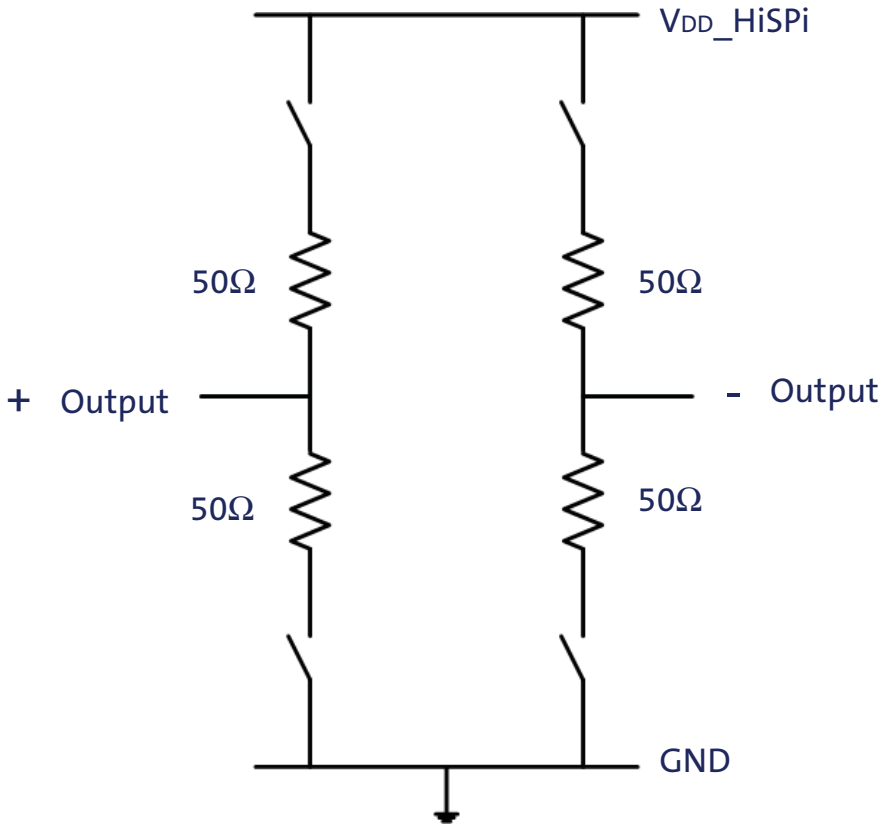


Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## HiSPi Output Equivalent Circuit

HiSPi Output signal DATA_P, DATA_N, D_CLK, D_CLK_N are composed as the equivalent circuit below.

**Figure 3: HiSPi Output Equivalent Circuit**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Power Consumption Estimate

**Table 9: Power Consumption Average 1 frame (Reference)**

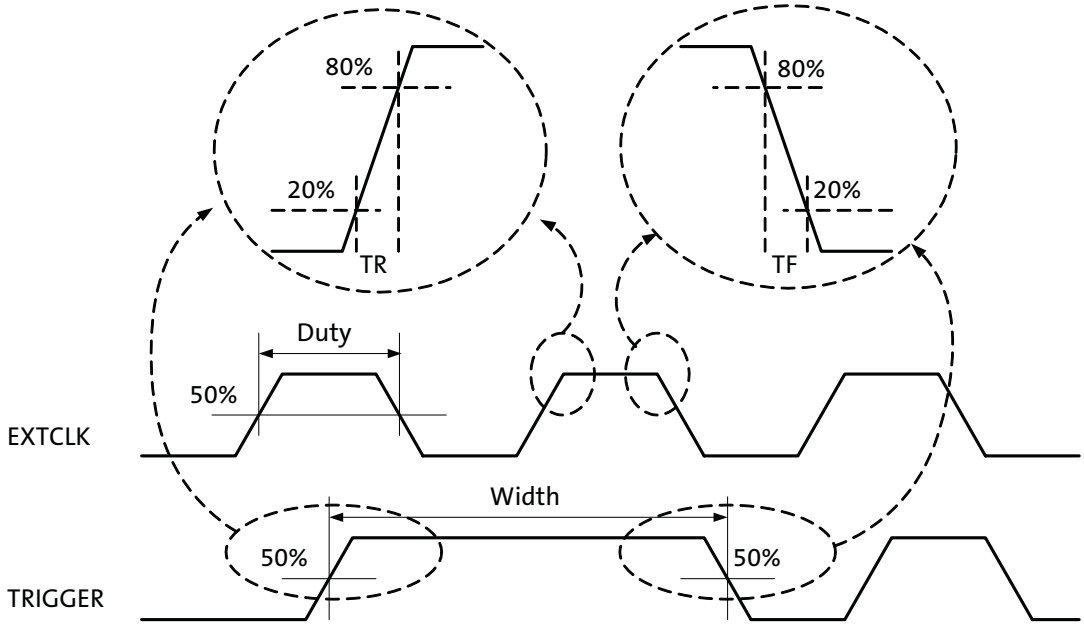
| Name (mW) | Power Consumption (mW) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Wait TRIGGER | Full Res | HD60_16:9_SLV | HD60_3:2_SLV | EVF | Pre Flash A | Pre Flash B | Hi-Speed | Super Hi-Speed |
| Total power | 413 | 1354 | 855 | 1195 | 858 | 873 | 873 | 1249 | 1249 |

**Table 10: Power Consumption Max 1 Frame (Reference)**

| Name (mW) | Power Consumption (mW) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Wait TRIGGER | Full Res | HD60_16:9_SLV | HD60_3:2_SLV | EVF | Pre Flash A | Pre Flash B | Hi-Speed | Super Hi-Speed |
| VDD | 368.6 | 448.7 | 399.6 | 382.7 | 379.9 | 313.5 | 312.8 | 430.4 | 429.2 |
| VAA | 206.8 | 861.9 | 861.9 | 599.4 | 599.1 | 692.2 | 692.0 | 876.2 | 876.7 |
| VAA1.8 | 0.3 | 1.0 | 0.5 | 0.4 | 0.4 | 0.3 | 0.3 | 0.6 | 0.6 |
| VAA_PIX | 46.0 | 247.0 | 199.4 | 115.9 | 115.5 | 116.3 | 116.3 | 181.2 | 181.3 |
| VDD_HiSPi | 24.1 | 24.6 | 19.5 | 16.5 | 16.4 | 6.2 | 6.2 | 24.3 | 24.3 |
| VDD_PLL | 25.0 | 25.1 | 25.0 | 25.1 | 25.1 | 25.1 | 25.0 | 25.2 | 25.2 |
| Total power | 670.8 | 1608.3 | 1505.9 | 1140.0 | 1136.5 | 1153.6 | 1152.5 | 1537.9 | 1537.2 |

## External Pulse Timing

**Figure 4: External Pulse Timing**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Table 11: External Pulse Definition**

| Name | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| EXTCLK | External clock | | 29.16 | 29.19 | MHz |
| Duty | EXTCLK clock duty | 45 | 50 | 55 | % |
| Jitter | EXTCLK clock jitter | – | – | 1 | % |
| Width | TRIGGER width | See Integration Time Control | | | |
| TR | Rise time | – | – | 5 | ns |
| TF | Fall time | – | – | 5 | ns |

## RESET_B

RESET_B is a control pulse for asynchronous hard reset. At the power-up period, RESET_B must be set at LOW, then must be set HIGH after the VDD power supply voltages are settled. The minimum RESET_B assert time is 30 EXTCLK cycles.

**Table 12: Signal I/O Status During RESET_B**

| Name | Status |
|---|---|
| DATA[23:0]_P | High-Z |
| DATA[23:0]_N | High-Z |
| D_CLK[5:0]_P | High-Z |
| D_CLK[5:0]_N | High-Z |
| SDATA | Input state |
| PHY_STABLE | High-Z |

## TRIGGER

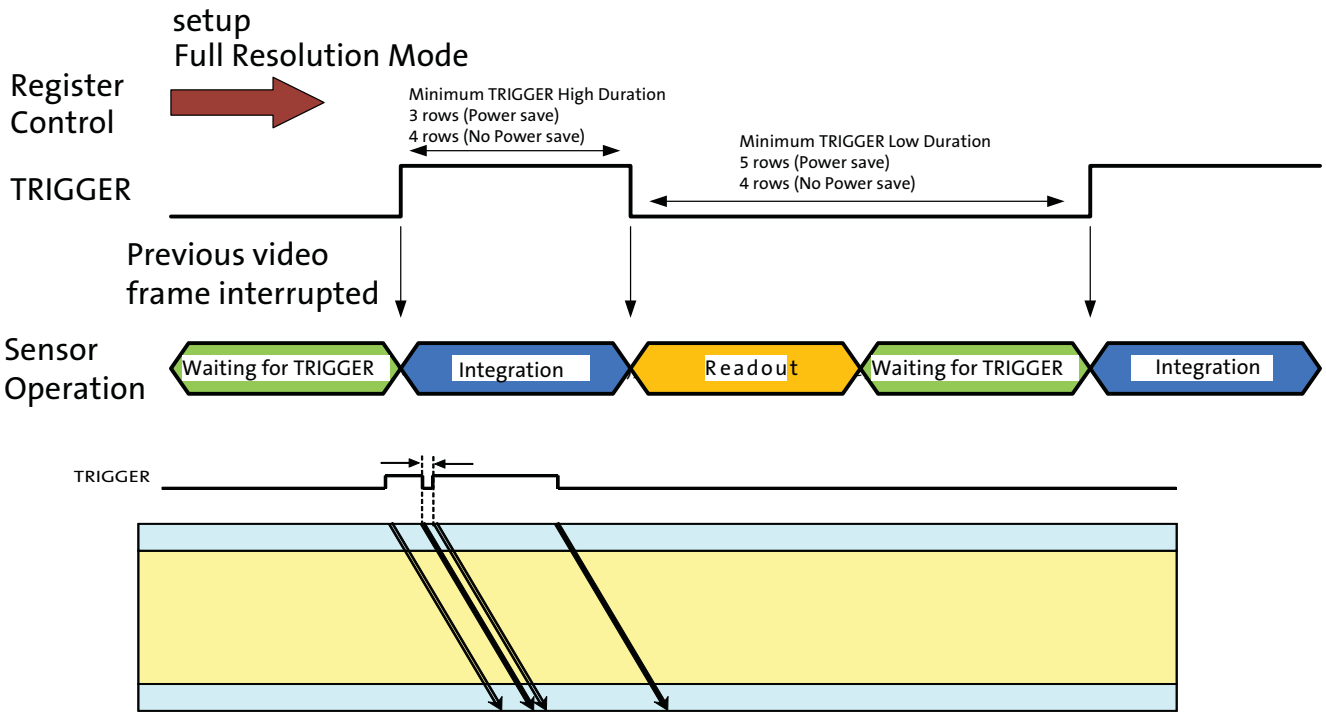
**Table 13: Minimum External TRIGGER High Duration**

| Mode | Full Resolution (Power Save) | Full Resolution (No Power Save) | Video Mode |
|---|---|---|---|
| Minimum TRIGGER High Duration | 3 rows | 4 rows | 10 clk |
| Minimum TRIGGER Low Duration | 5 rows | 4 rows | – |



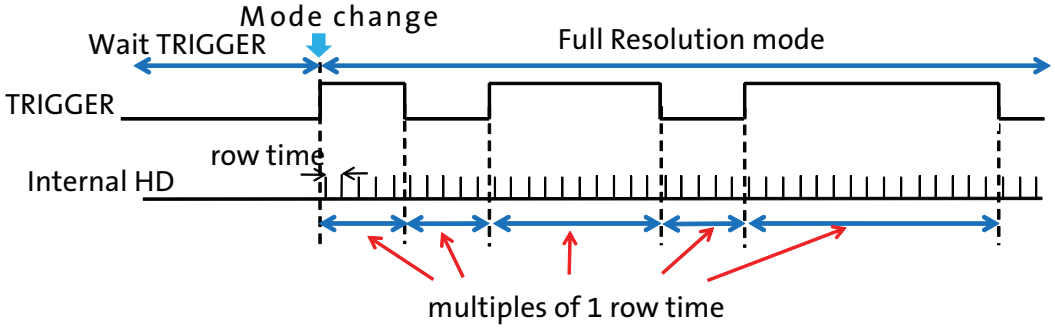
Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 5: TRIGGER Control in Full Resolution HD60_3:2_SLV, HD120_16:9_SLV Mode**




TRIGGER high and low durations are strongly recommended to be set to the multiples of a row time. When a TRIGGER edge overlaps with an internal HD timing, it can cause fluctuation of integration or frame readout timing. Toggling TRIGGER at timings of multiples of the row duration provides an identical margin between TRIGGER toggling to the internal HD, which avoids generating the fluctuation.

**Figure 6: TRIGGER Timing Recommendation in Full Resolution HD60_3:2_SLV, HD120_16:9_SLV Mode**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 7: TRIGGER Timing and Internal HD in Full Resolution HD60_3:2_SLV, HD120_16:9_SLV Mode**

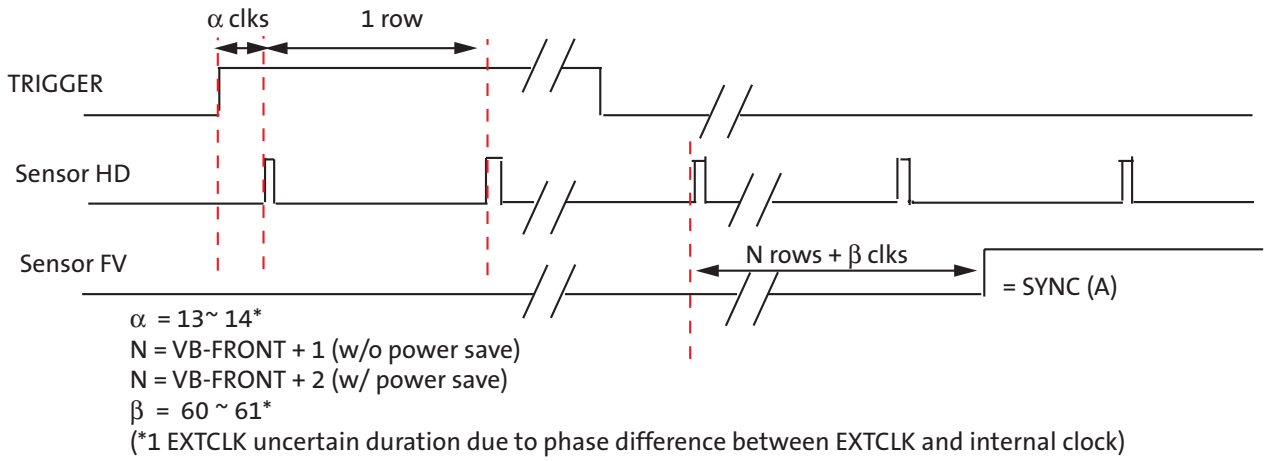



**Figure 8: TRIGGER Control in Video Mode**

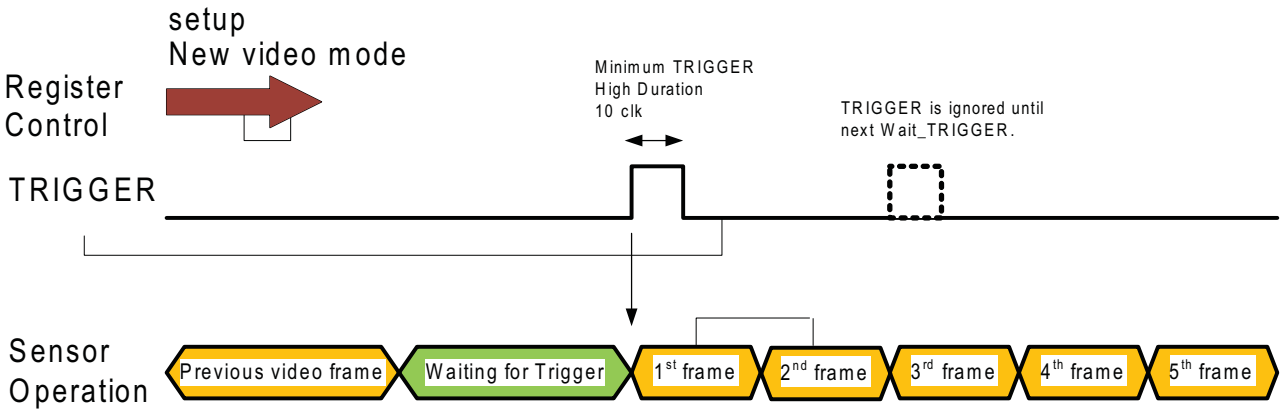
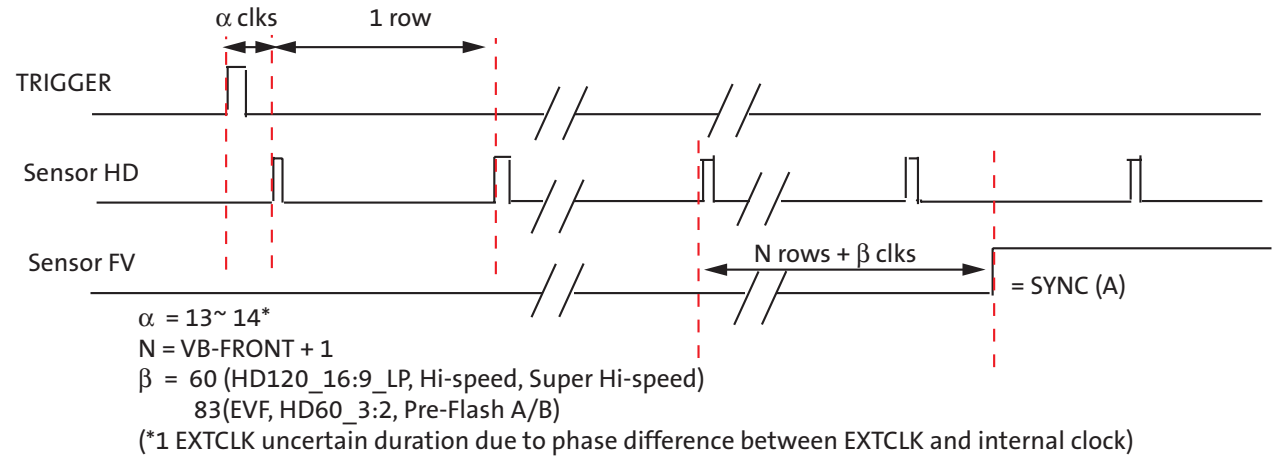



**Figure 9: TRIGGER Timing and Internal HD in Video Mode**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## PHY_STABLE

When PHY_STABLE is HIGH, the HiSPi PHY transmitter output is stable. When the PHY_STABLE output is LOW, the sensor is in power save mode and the differential data output is invalid.

## Power Up and Down Sequences

### Power Up Sequence

**Figure 10: Power Up Sequence**

The power must be settled up
more than 90% before the next power up.

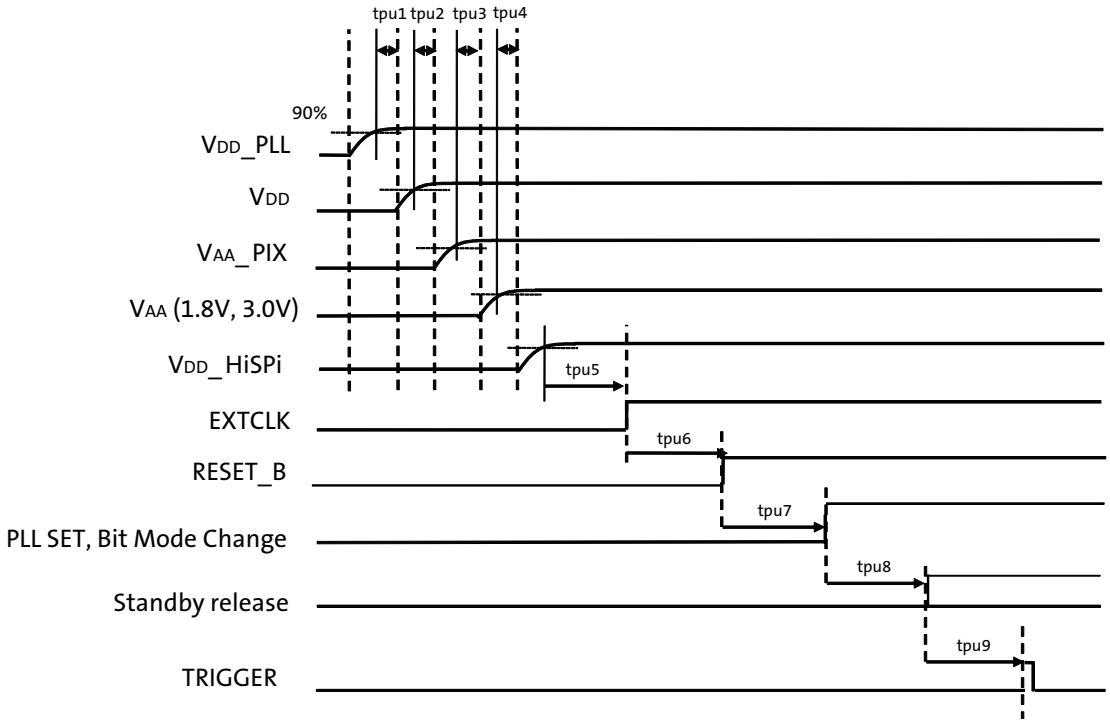



**Table 14: Power-up Sequence Timing Parameters**

| Parameter | Min | Max |
|---|---|---|
| tpu1 | 0 ms[1] | – |
| tpu2 | 0 ms[1] | – |
| tpu3 | 0 ms[1] | |
| tpu4 | 0 ms[1] | – |
| tpu5 | 0.5 ms | – |
| tpu6 | 0.5 ms | – |
| tpu7 | 1 ms | – |
| tpu8 | 0.5 ms | – |
| tpu9 | 1.1 ms | – |

Note: 1. Simultaneous power up is available; however, to avoid extra current, waiting for voltage of the previous power supply in the sequence to settle up is preferred.



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

### Power Down Sequence

**Figure 11: Power Down Sequence**

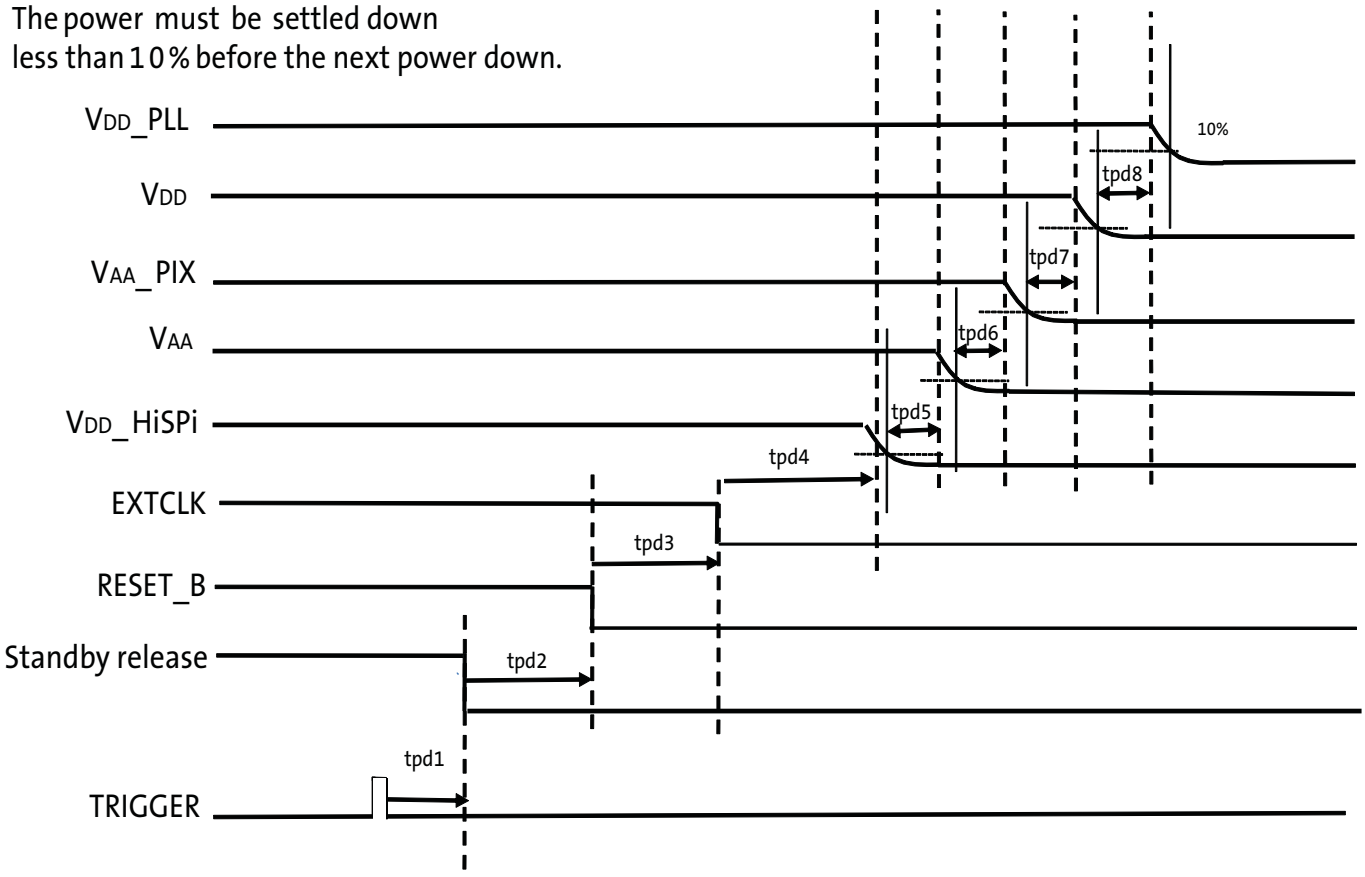



**Table 15: Power Down Sequence Timing Parameters**

| Parameter | Min | Max |
|---|---|---|
| tpd1 | 0.5ms | – |
| tpd2 | 0.5ms | – |
| tpd3 | 0.5ms | – |
| tpd4 | 0ms[1] | – |
| tpd5 | 0ms[1] | – |
| tpd6 | 0ms[1] | – |
| tpd7 | 0ms[1] | – |
| tpd8 | 0ms[1] | – |

Note: 1. Simultaneous power shut down is available; however, to avoid extra current, wait for the voltage of the previous power supply in the sequence to settle down.

## Standby

Standby status needs to be released following RESET_B release. Change of output digital resolution (10-bit or 12-bit) must be done before Standby release.



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Synchronization Codes and Blanking Codes

**Figure 12: Blanking Code and Synchronization Code in a PHY (Case Data_0/2/4/6)**

| | | | | | |
|---|---|---|---|---|---|
| data_0 ..... | Blanking code | Blanking code | Blanking code | Sync_word_1 | Pixel data - - |
| data_2 ..... | Blanking code | Blanking code | Blanking code | Sync_word_2 | Pixel data - - |
| data_4 ..... | Blanking code | Blanking code | Blanking code | Sync_word_3 | Pixel data - - |
| data_6 ..... | Blanking code | Blanking code | Blanking code | Sync_word_4 | Pixel data - - |

| Sync_word_1 | Sync_word_2 | Sync_word_3 | Sync_word_4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| All 1s | All 0s | All 0s | 1 | 0 | V | 0 | V | 0 | V | V | 000... |

V = 1 SYNC-B during frame blanking

V = 0 SYNC-A during active (pixel data) period

| Blanking code | Blanking Code | Blanking Code | Blanking Code |
|---|---|---|---|
| 100---00 | 011---11 | 100---00 | 011---11 |

Table 18 illustrates the basic format of sync code. The code is transmitted from left to right on the line. This order is not affected by MSB first or LSB first selection.

Each “Word” has the same depth as the active image pixels. All 1 and all 0 values are unique to the sync code. The data from an active pixel will not be transmitted with these values. Table 19 on page 15 describes the sync code Word 4 for each word size preceding Active Data - SYNC (A) or Blanking Data- SYNC (B).

**Table 16: Actual Binary Sync Code (Word 4)**
SYNC(A) for Active Data and SYNC(B) for Blanking Data

| Word Size | SYNC (A) Sync Code: Active Data | SYNC (B) Sync Code: Blanking Data |
|---|---|---|
| 12-bit | `b1000 0000 0000 | `b1010 1011 0000 |

Notes:
1. Sync code Word 1 (All 1s) is always transmitted on lane 0.
2. Sync code Word 2 (All 0s) is always transmitted on lane 2.
3. Sync code Word 3 (All 0s) is always transmitted on lane4.
4. Sync code Word 4 (10V0V0VV00...) is always transmitted on lane 6.

The format of the code allows the receiver to correct a single bit error in Word4 or a detection of 2 bit errors.

The protocol layer does not indicate the end of the active image data and the beginning of the horizontal blanking words in a transmitted line. The receiver must be configured to the length of the active pixel data.



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Filler Codes

The synchronization code is four words. An optional filler code of "1" may be added after the sync code. When filler codes are enabled, the receiver must window the received image to eliminate the first 4 data words (columns per PHYs). In other words, if the interface is configured with 6 PHYs, the first 24 words (total columns) of a line will be filler data.

Change of filler code setting from a default value must be completed during the wait_trigger state after RESET_B release.

**Table 17: Binary Representation of Filler Codes**

| Data Word Size | Filler Code |
|---|---|
| 12- bit | 'b0000 0000 0001 |

**Figure 13: Sync Code Format with Extra Filler Codes**

| | | | | | | |
|---|---|---|---|---|---|---|
| data_0----- | Blanking code | Blanking code | Blanking code | Sync word_1 | ... 0001 | Pixeldata- - |
| data_2 ----- | Blanking code | Blanking code | Blanking code | Sync word_2 | ... 0001 | Pixeldata- - |
| data_4 ----- | Blanking code | Blanking code | Blanking code | Sync word_3 | ... 0001 | Pixeldata- - |
| data_6 ----- | Blanking code | Blanking code | Blanking code | Sync word_4 | ... 0001 | Pixeldata- - |

**Table 18: Filler Code Control Register Setting**

| Name | Bit | Default | |
|---|---|---|---|
| vert_left_bar_en | 0 | 0 | 0: Filler is not embedded<br>1: Filler is embedded |



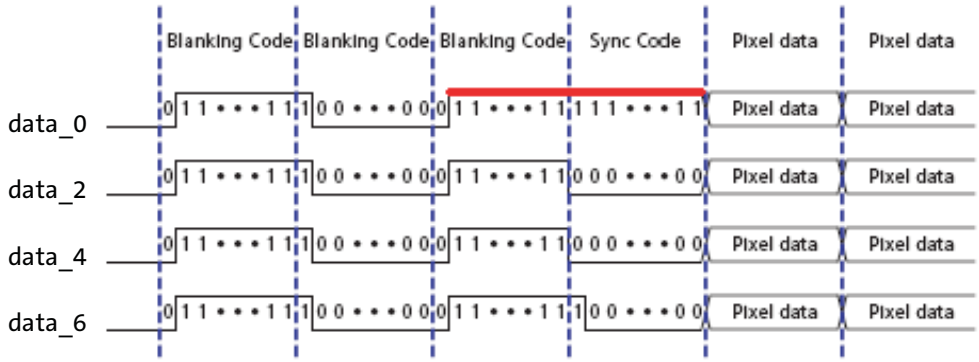
Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Bit Order

Pixel data may be transmitted MSB first or LSB first; it is a programmable option in the sensor. The Sync Codes, Filler Codes, and Blanking Codes are always transmitted MSB first.

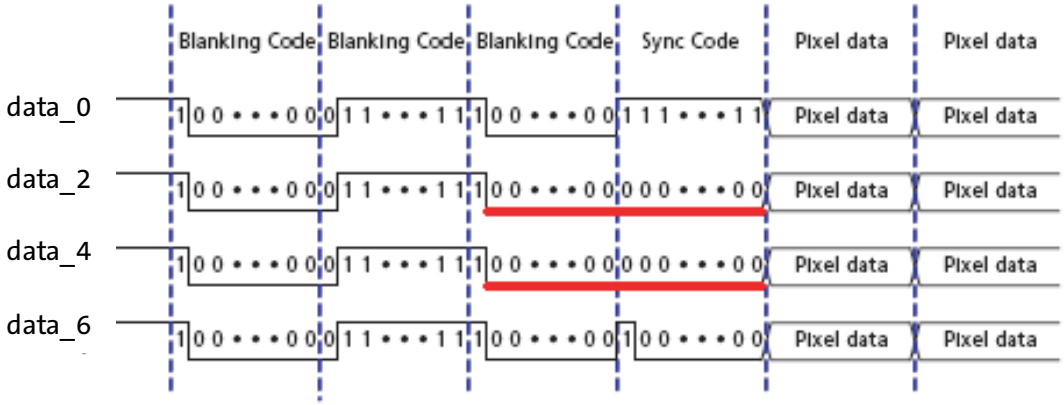
Change of bit order setting must be completed during the wait_trigger state after RESET_B release.

**Figure 14: Sync Code Detection on PHY with 'b011...111 Word**




**23 consecutive 1s detected on lane 0**

**Figure 15: Sync Code Detection on PHY with 'b100...000 Word**




**23 consecutive 1s detected on lane1, 2**

**Table 19: Bit Order Control Register Setting**

| Name | Bit | Default | |
|---|---|---|---|
| output_msb_first | 0 | 1 | 0: LSB first<br>1: MSB first |



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# HiSPi™ Video Interface (I/F)

HiSPi™ (High Speed Serial Pixel) is Aptina's original simple logical layer protocol with low power consumption and high speed interface, which is scalable to accommodate increasing sensor resolutions and high frame rates for advanced digital still cameras (DSC), digital video cameras (DVC), and digital single-lens reflex (DSLR) camera applications.

The interface calls for serial pixel data transmitter on multiple serial lanes. The number of data lanes will be determined by the desired frame rate, bit depth, maximum data rate, and sensor resolution for a particular design.

The HiSPi™ interface enables high bandwidth data transfer for both video and still images. It consists of both data and clock signaling that can be scaled to the required data transfer for an application.

The HiSPi™ interface specification defines the physical layer covering the transmission medium, electrical parameters, signaling and timing relationship between the clock lane and data lanes, the logical protocol layer covering data formats, and synchronization.

The HiSPi™ interface building block is a unidirectional differential serial interface with four data lanes and one double data rate (DDR) clock lane. The interface is scalable with multiple instantiations of this block. One clock for every four serial data lanes is provided for phase alignment across multiple lanes.

The AR1411HS video output I/F is designed based on AR1411HS's HiSPi™.

## Basic Features

Following are the features of HiSPi™ in the AR140.

- A low voltage, low power consumption driver
- 12-bit/10-bit compression mode switchable
- Data rate of 700 Mbps(12-bit)/583Mbps(10-bit) and 350 MHz DDR clock at 29.16 MHz EXTCLK
- 24 data lanes plus 6 clock lanes
- Embedded sync codes
- Each lane outputs individual pixel signals
- Output common voltage: 0.2V typical

**Table 20: HiSPi™ Format**

| Parameter | Specification | Comments |
|---|---|---|
| Image data interface HiSPi™ | Data: 24 lanes<br>Clock: 6 lanes | 700 Mbps (bit rate 12 x Master clock)<br>583 Mbps (bit rate 10 x Master clock) |
| | Data rate compression mode | Data rate 12-bit/10-bit compression mode switchable |



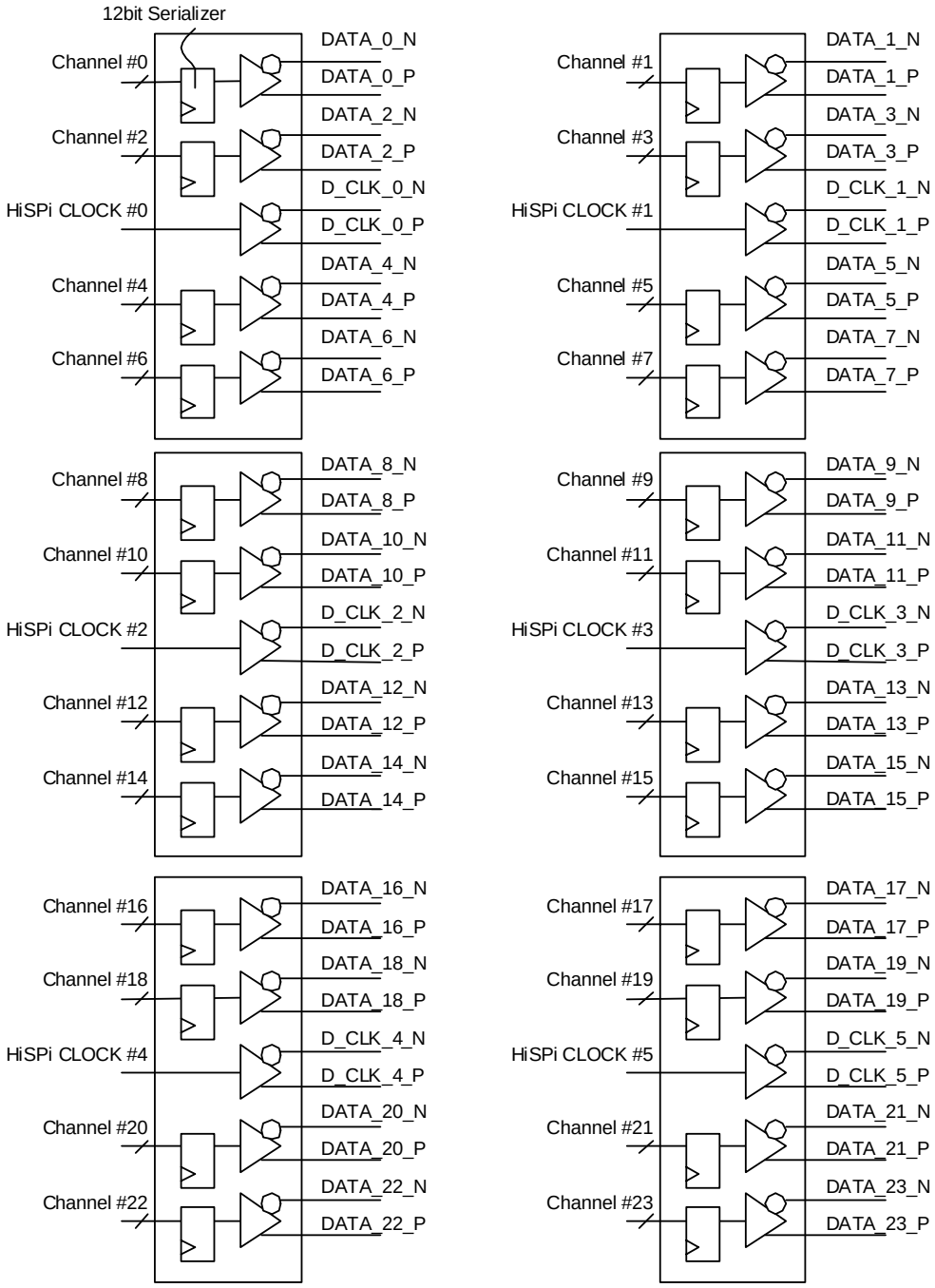
Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Transmitter PHY Structure

The 24 data output lanes are laid out in the 6 physical blocks. One block corresponds to one PHY and each block consists of 4 data lanes and one clock lane. The output data is synchronized to a DDR clock in the same block. Latching data by the clock in the corresponding block is required to receiver.

Pixel data rate from each lane is identical to the EXTCLK frequency.

**Figure 16: 24-Lane HiSPi™ Output**



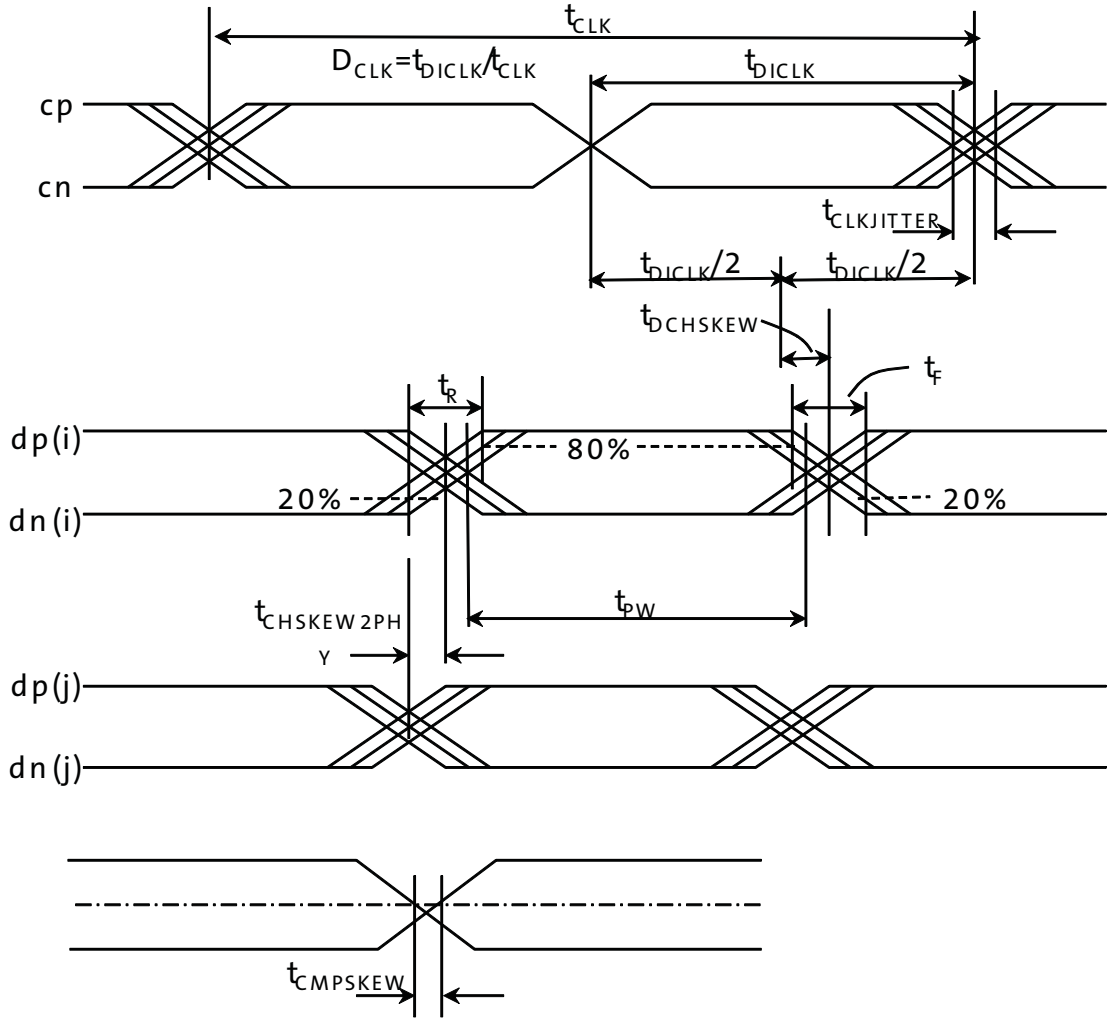



Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

## AC Specifications

The external master clock and output digital format of the AR1411HS are specified at EXTCLK and 12-bit pixel resolution, respectively. Therefore, the typical data clock frequency and data rate per lane are also specified at 12x EXTCLK (DDR) and EXTCLK x 24 bps/Hz, respectively.

**Figure 17: AC Parameters**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Table 21: HiSPi™ Basic AC Specifications**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Data rate | $1/t_{DICLK}$ | 280 | | 700 | Mbps | 12-bit output |
| Clock period | $t_{CLK}$ | 2.86 | | 7.14 | ns | |
| Data period | $t_{DICLK}$ | 1.43 | | 3.57 | ns | |
| Data Eye width | $t_{PW}$ | – | | 0.6 | UI | |
| Clock jitter | $t_{CLKJITTER}$ | – | – | 100 | ps | |
| Rise time | $t_R$ | 150 ps | 230 ps | 0.25UI | | |
| Fall time | $t_F$ | 150 ps | 230 ps | 0.25UI | | |
| Clock duty | $D_{CLK}$ | 45 | | 55 | % | |
| Clock to data skew | $t_{DCHSKEW}$ | -0.1 | | 0.1 | UI | |
| Data to data skew in any two PHY | $t_{CHSKEW2PHY}$ | – | – | 2.1 | UI | |
| Complementary skew in differential pair | $t_{CMPSKEW}$ | -100 | – | 100 | ps | |

Notes: 1. 1 UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Measured by probe card.

## DC Specifications

### Measurement Method

The measurements for CLOCK and all the data channels were observed with DATA using the single-ended scope probe in differential and common-mode. DATA was set to the square wave in the HiSPi™ test pattern generator.

**Figure 18: DC Parameters Transceiver**

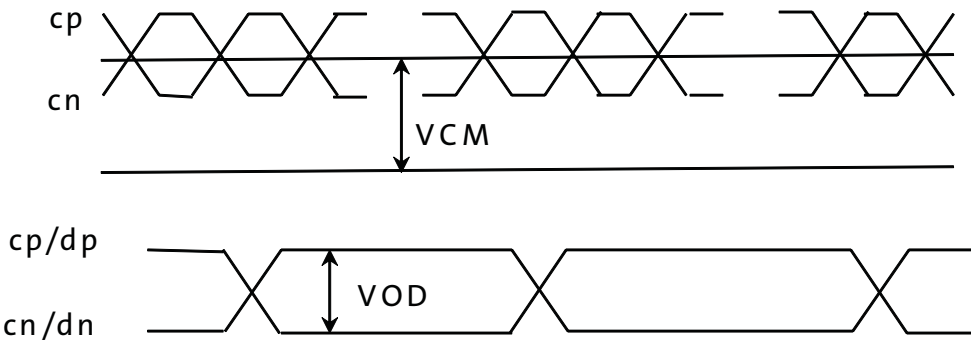



**Table 22: AR1411HS HiSPi™ DC Performance**

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| VDD_HiSPi | HiSPi™ power supply | 0.35 | 0.4 | 0.45 | V | |
| VOD | Input differential voltage | 360*VDD_HiSPi | 500*VDD_HiSPi | 550*VDD_HiSPi | mV | RIN = 100Ω |
| VCM | Input common mode range | 450*VDD_HiSPi | 500*VDD_HiSPi | 640*VDD_HiSPi | mV | RIN = 100Ω |
| RIN | Termination resistor | – | 100 | – | Ω | |
| Output impedance | Output impedance | 35 | 50 | 70 | Ω | |


Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## DLL Timing Adjustment

Within the PHY there is a DLL connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

The DLL operation is guaranteed only at a specified data rate of 700 Mbps. The integrity of the serial data cannot be guaranteed if the DLL settings are changed while the PHYs are streaming.

Changing DLL settings in wait_trigger is recommended. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter and skew.

**Figure 19: Block Diagram of DLL Timing Adjustment**

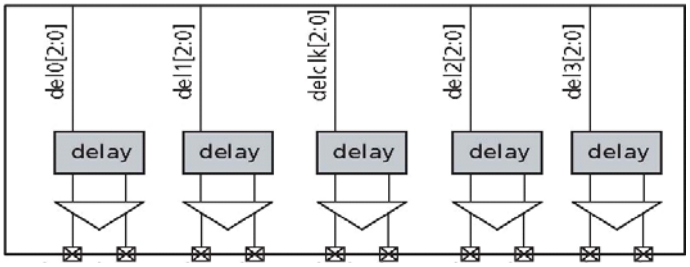
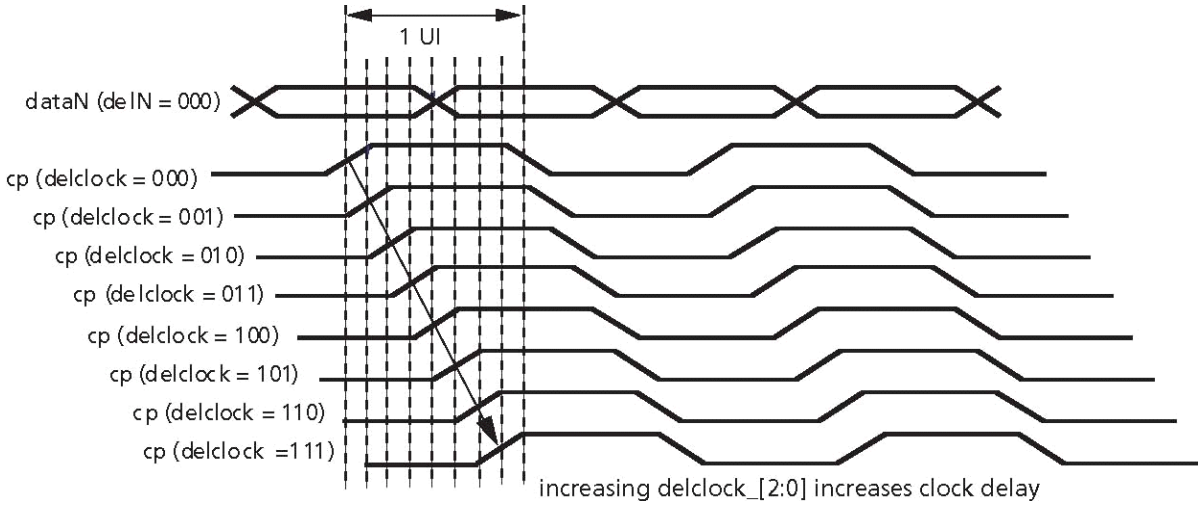



**Figure 20: Delaying the clock_lane with Respect to data_lane**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 21: Delaying the data_lane with Respect to clock_lane**

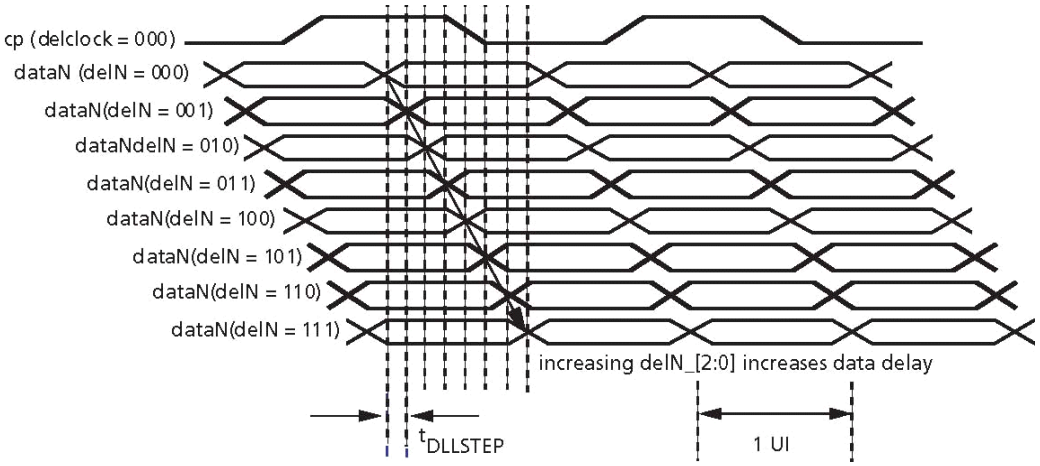



**Table 23: DLL Timing Adjuster Control Register Setting**

| Name | Bit | Default | |
|---|---|---|---|
| del_data_lane0 | 2:0 | 0 | Delay control for data lane #0 |
| del_data_lane1 | 2:0 | 0 | Delay control for data lane #1 |
| del_data_lane2 | 2:0 | 0 | Delay control for data lane #2 |
| del_data_lane3 | 2:0 | 0 | Delay control for data lane #3 |
| del_data_lane4 | 2:0 | 0 | Delay control for data lane #4 |
| del_data_lane5 | 2:0 | 0 | Delay control for data lane #5 |
| del_data_lane6 | 2:0 | 0 | Delay control for data lane #6 |
| del_data_lane7 | 2:0 | 0 | Delay control for data lane #7 |
| del_data_lane8 | 2:0 | 0 | Delay control for data lane #8 |
| del_data_lane9 | 2:0 | 0 | Delay control for data lane #9 |
| del_data_lane10 | 2:0 | 0 | Delay control for data lane #10 |
| del_data_lane11 | 2:0 | 0 | Delay control for data lane #11 |
| del_data_lane12 | 2:0 | 0 | Delay control for data lane #12 |
| del_data_lane13 | 2:0 | 0 | Delay control for data lane #13 |
| del_data_lane14 | 2:0 | 0 | Delay control for data lane #14 |
| del_data_lane15 | 2:0 | 0 | Delay control for data lane #15 |
| del_data_lane16 | 2:0 | 0 | Delay control for data lane #16 |
| del_data_lane17 | 2:0 | 0 | Delay control for data lane #17 |
| del_data_lane18 | 2:0 | 0 | Delay control for data lane #18 |
| del_data_lane19 | 2:0 | 0 | Delay control for data lane #19 |
| del_data_lane20 | 2:0 | 0 | Delay control for data lane #20 |
| del_data_lane21 | 2:0 | 0 | Delay control for data lane #21 |
| del_data_lane22 | 2:0 | 0 | Delay control for data lane #22 |
| del_data_lane23 | 2:0 | 0 | Delay control for data lane #23 |
| del_clock_phy0 | 2:0 | 0 | Delay control clock for HiSPi™ #0 |
| del_clock_phy1 | 2:0 | 0 | Delay control clock for HiSPi™ #1 |
| del_clock_phy2 | 2:0 | 0 | Delay control clock for HiSPi™ #2 |
| del_clock_phy3 | 2:0 | 0 | Delay control clock for HiSPi™ #3 |
| del_clock_phy4 | 2:0 | 0 | Delay control clock for HiSPi™ #4 |
| del_clock_phy5 | 2:0 | 0 | Delay control clock for HiSPi™ #5 |



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

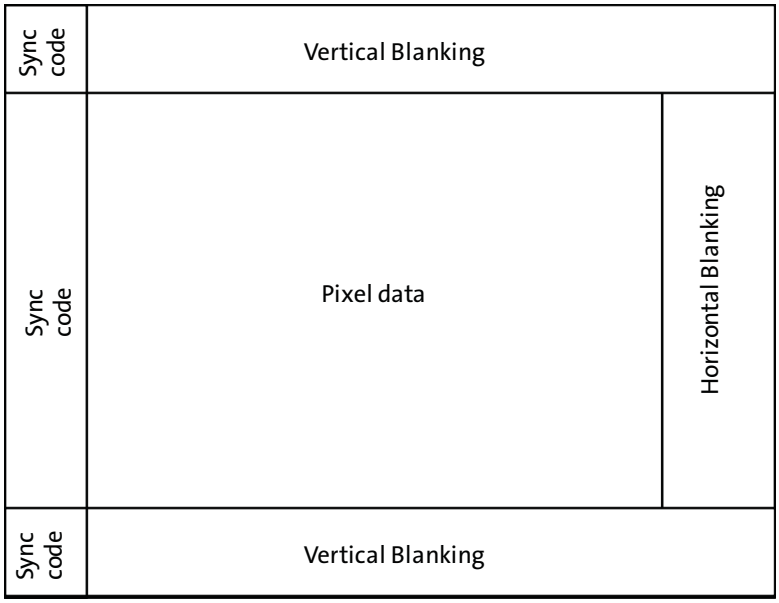
## Protocol Layer

The protocol layer is positioned between the output data path of the sensor and the physical layer. The main functions of the protocol layer are generating sync codes, formatting pixel data, inserting horizontal/vertical blanking codes, and distributing pixel data over defined data lanes.

## Protocol Fundamentals

Figure 22 illustrates the structure of a frame including sync code, active image, horizontal blanking, and vertical blanking, showing how data of a frame is transmitted across the HiSPi link.

**Figure 22: Frame Structure for HiSPi™ Transmission**



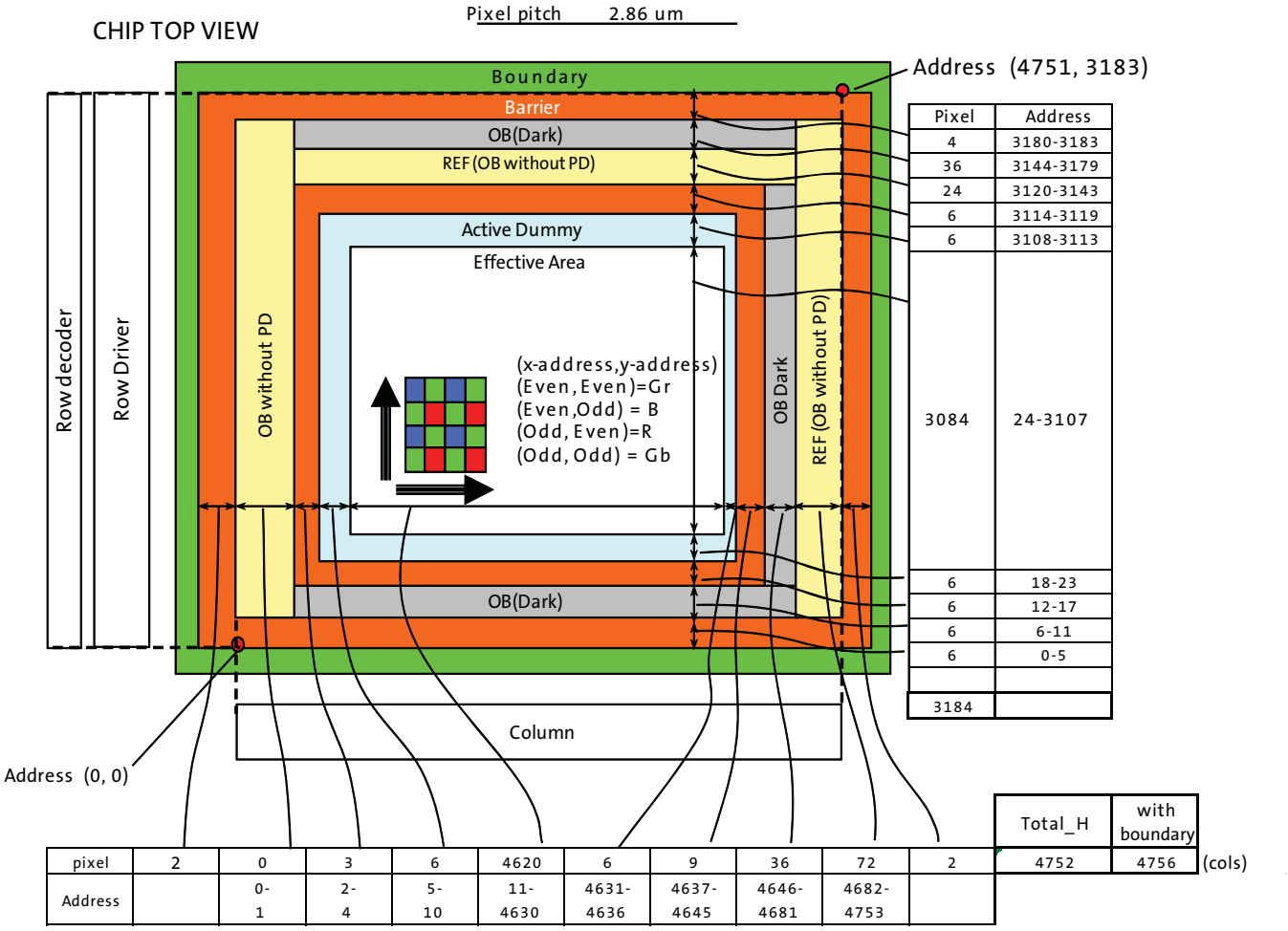


Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Pixel Readout

## Pixel Array Configuration

### Figure 23: Pixel Array Configuration



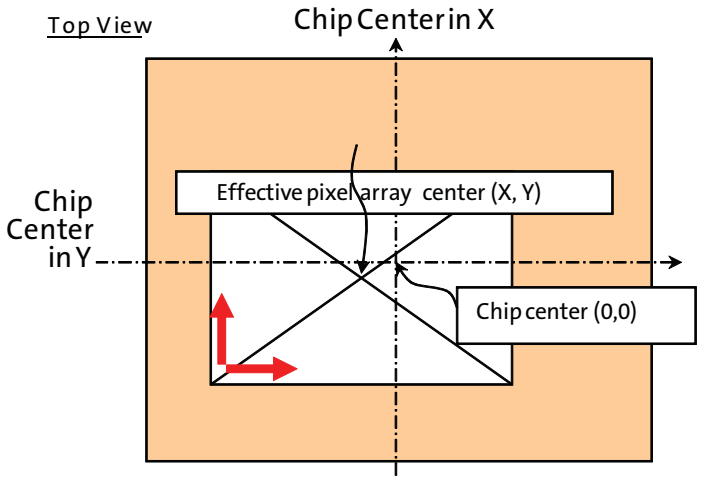


Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Pixel Array Center Offset

A typical offset of the effective pixel array center is: X=-105.680 µm, Y=-75.070 µm

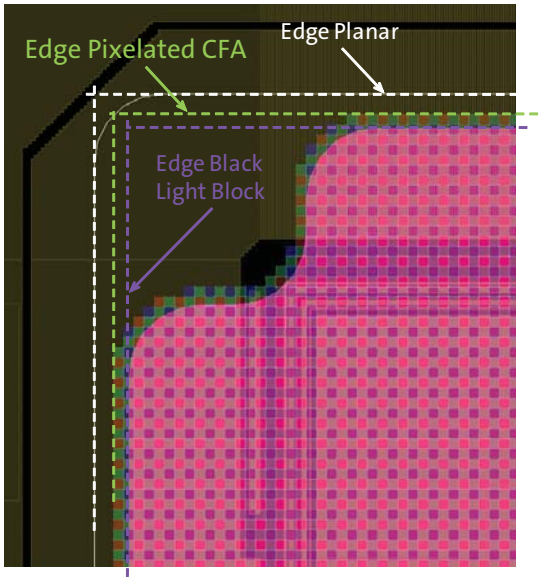
**Figure 24: Chip Center in X**




## Light Block Edge

The light block edge follows Figure 25 when coordinates are defined with respect to Die Center (0,0) in µm.

**Figure 25: Light Block Edge From Die Center**




Edge Upper Left Planar Corner: (-8599.105, 7844.105)

Edge Blue Upper Left Red Corner: (-8593.42, 7837.905)

Upper Left Blue Corner (notched): (-8589.105, 7834.105)



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Readout Mode Control

## Mode Control

### Mode Transition

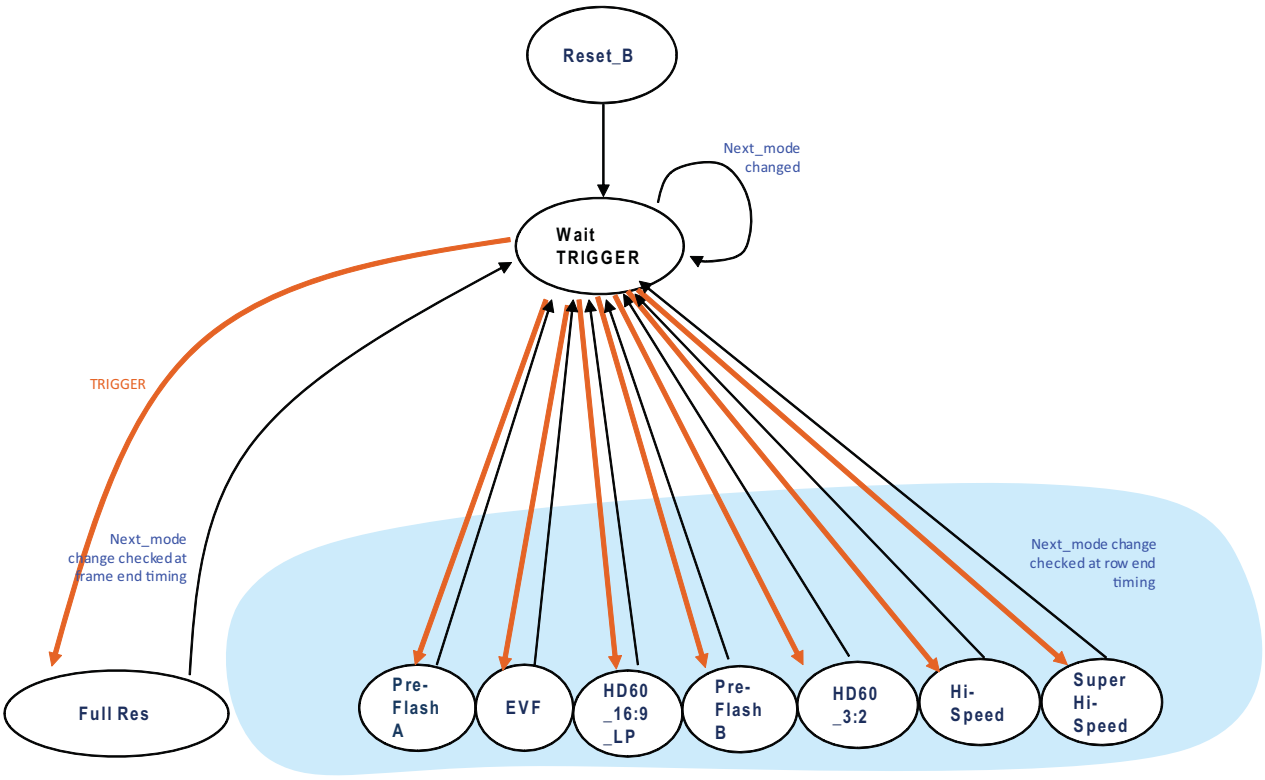
The AR1411HS has a unique feature that enables a very short shutter release lag in Full Resolution image capturing.

- During a video mode, when the user changes the register 'next_mode', the AR1411HS immediately stops reading and gets into the Wait Trigger state
- During Full Resolution Mode, when the user changes the register 'next_mode', the AR1411HS goes to Wait Trigger after readout of the current frame.
- When a rising edge of the TRIGGER pulse is detected, the AR1411HS starts the light integration when Full Resolution Mode is chosen.
- When a rising edge of the TRIGGER pulse is detected, the AR1411HS starts readout the captured image when a video mode is chosen.
- Setting up a new mode requires the time for internal ROM readout (200µs at EXTCLK=29.16 MHz) and the time for optional registers writing

**Note:** During the internal ROM readout, the communication of the two-wire serial I/F is gated, and the image sensor is neglecting any input from the serial I/F.

- TRIGGER is edge-sensitive.

**Figure 26: State Control**



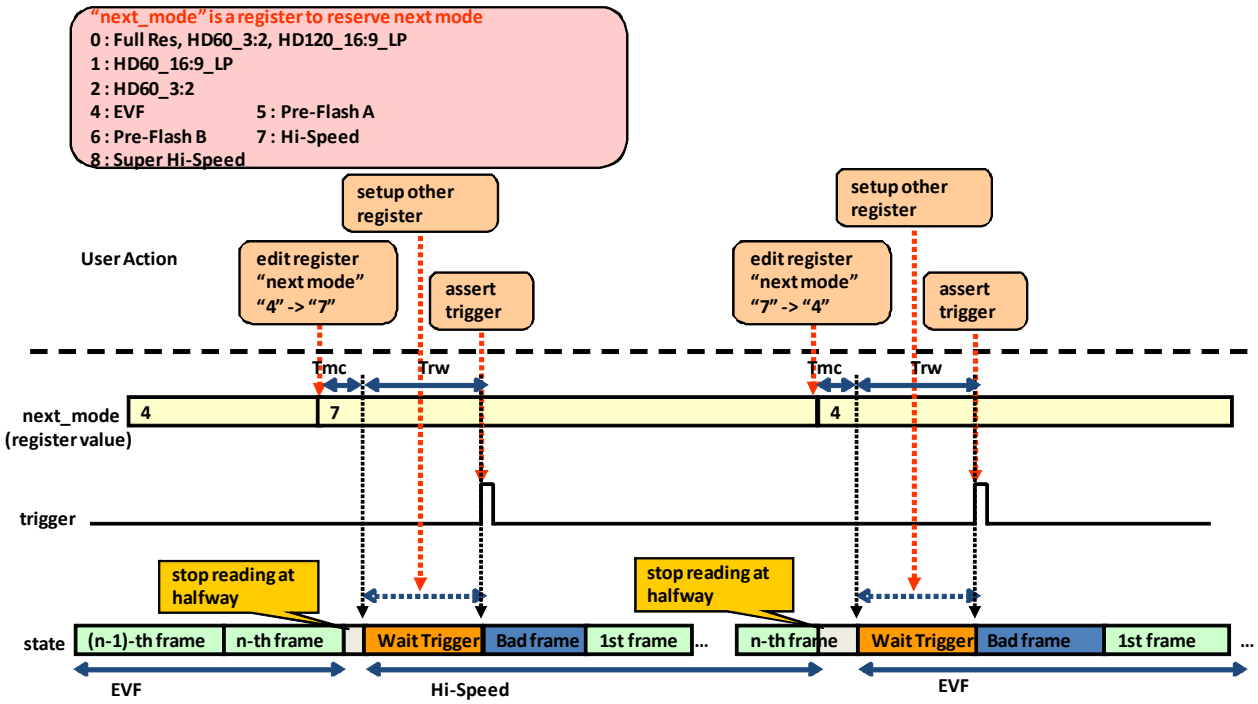

**Note:** Full Resolution mode reads out only once without changing Next_mode register. The other modes keep reading continuously until changing Next_mode register.



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

Mode Change Sequence (Example: EVF -> Full Resolution -> EVF)

**Figure 27: Mode Change Sequence from EVF to Full Resolution to EVF**



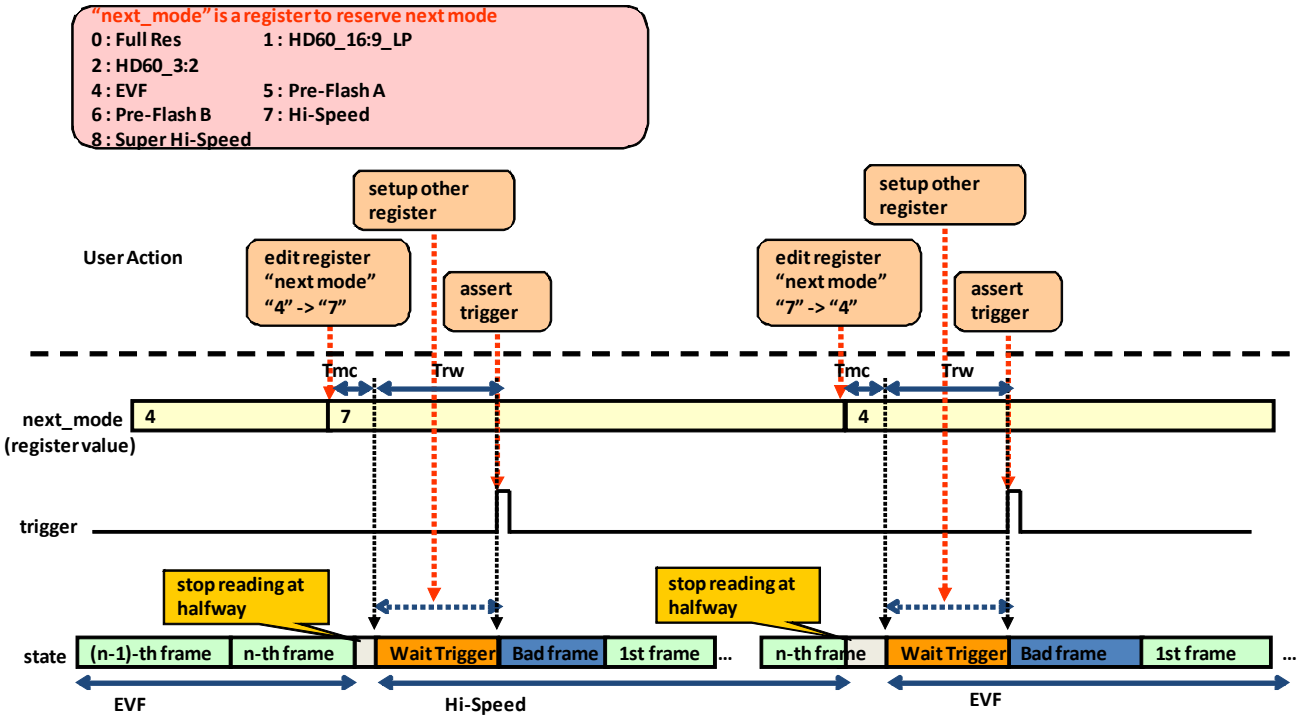

Notes:
1. $T_{mc} \geq 200$ µs at EXTCLK = 29.16 MHz
   (during this period, additional register read/write must be prohibited)
2. $T_{rw} \geq 0$ s
   (Trw can be 0 s when additional register write is not needed)



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Mode Change Sequence (Example: EVF -> Hi-Speed -> EVF)

**Figure 28: Mode Change Sequence from EVF to Hi-Speed to EVF**



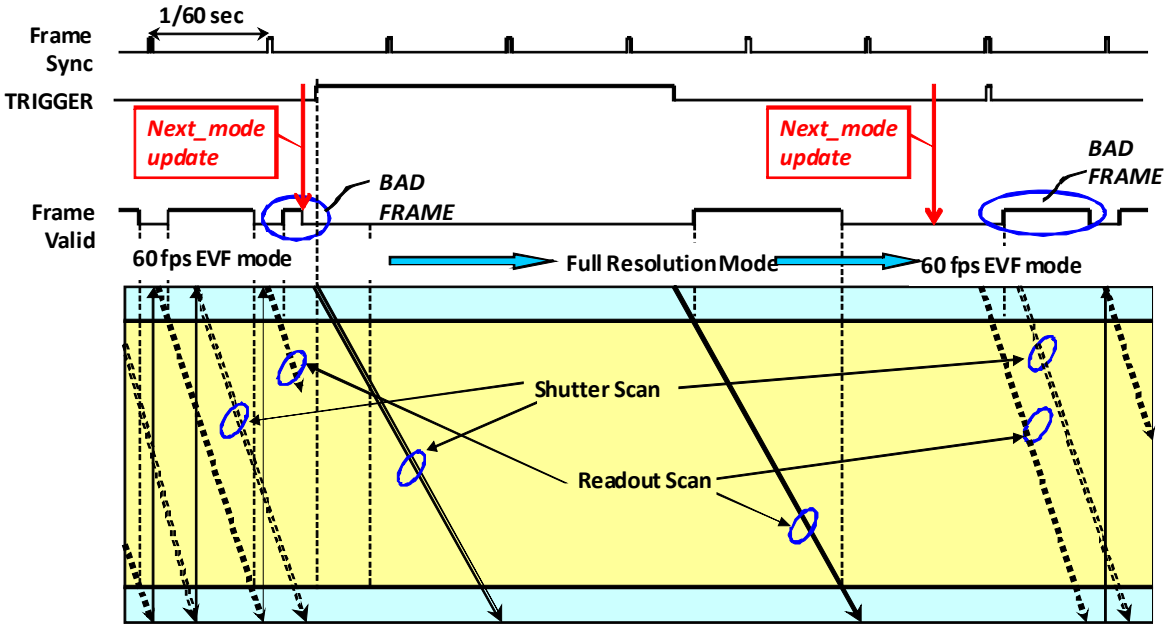

Notes:
1. $T_{mc} \geq 200\mu s$ at EXTCLK = 29.16MHz
   (during this period, additional register read/write must be prohibited)
2. $T_{rw} \geq 0$ s
   (Trw can be 0 s when additional register write is not needed)



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

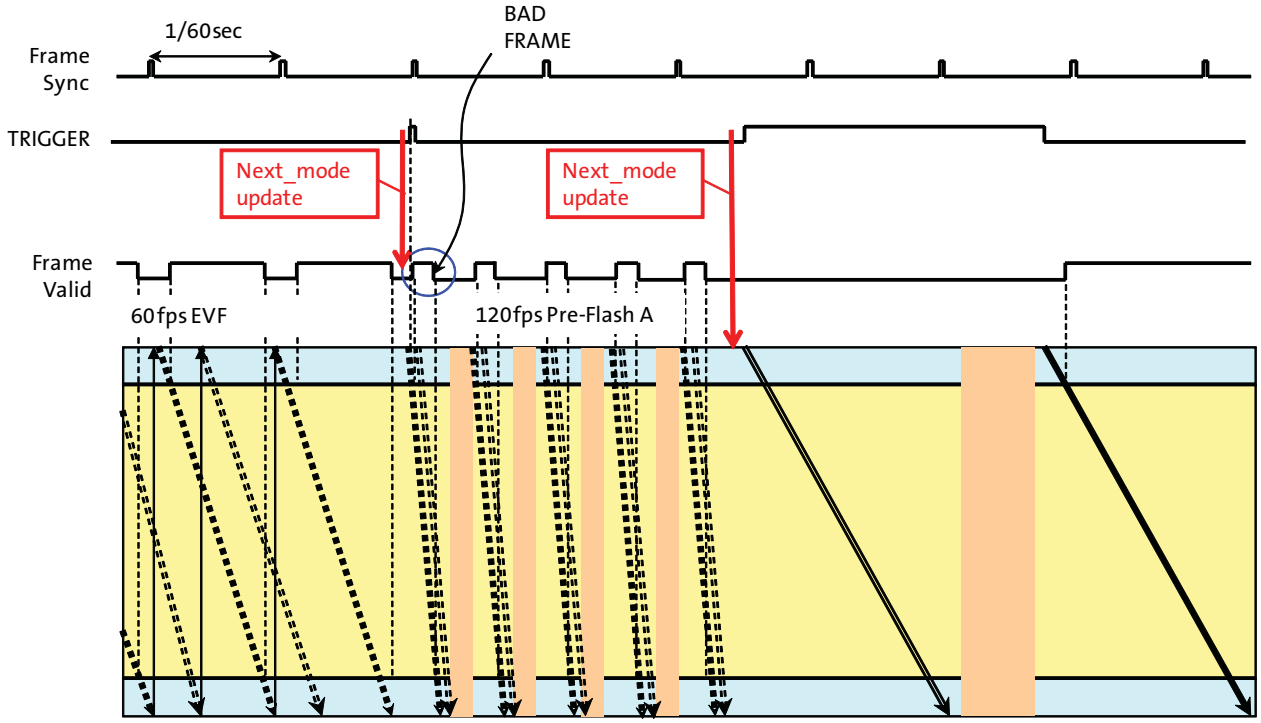
### Mode Change Example - From EVF Mode to Full Resolution Mode

**Figure 29: Mode Change Sequence and Internal Operation, from EVF to Full Resolution**




### Mode Change Example - From an EVF Mode to Full Resolution Mode via Pre-Flash A Mode

**Figure 30: Mode Change Sequence and Internal Operation, from EVF to Full Resolution via Pre-Flash A**






Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

### Consecutive Full Resolution Mode

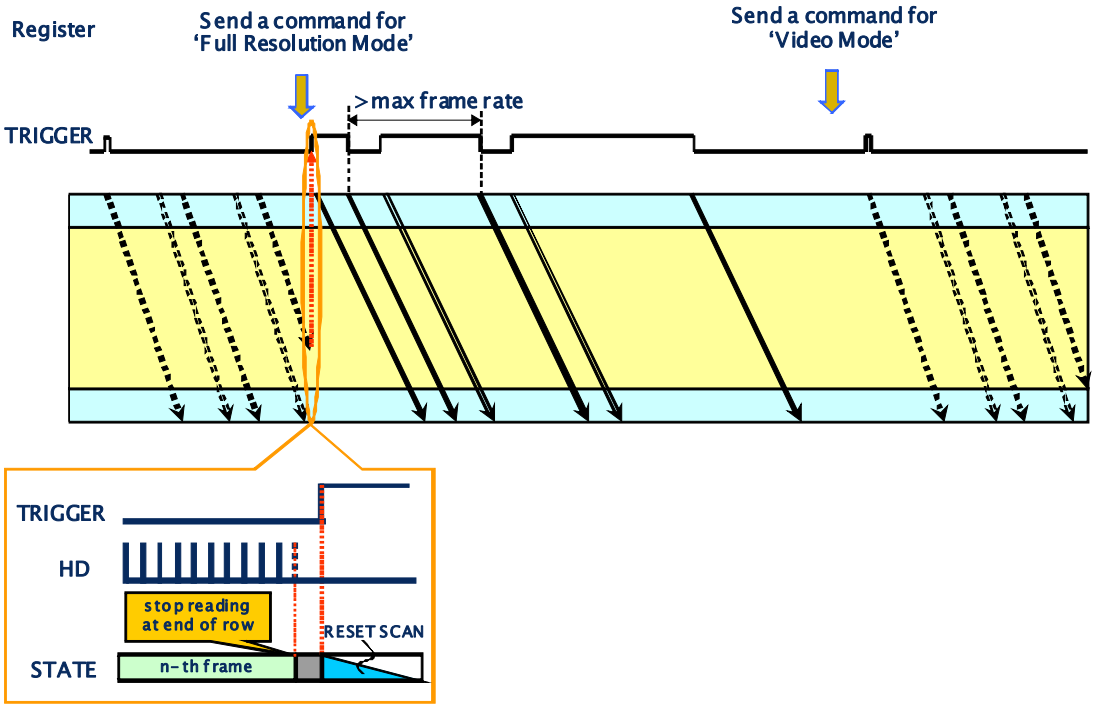
**Features**

- Supports the consecutive full resolution imaging at the maximum frame rate (60 fps with full resolution) as long as the integration time is shorter than the frame period
- Exposure time can be changed in an individual frame
- No bad frames appear in any integration time changes
- Simple control by TRIGGER input only
- No limitations on the number of consecutive frames

**TRIGGER Control for Consecutive Full Resolution Imaging**

- The command to change operation mode to a full resolution image capturing is sent and the video mode is stopped at the current row end, the sensor is getting into the 'waiting TRIGGER' status.
- Integration (Shutter scan) starts when TRIGGER rising edge is detected. Internal HD will also be restarted with a latency of 13-14 clocks following the TRIGGER rise. Then the image data readout starts when TRIGGER falling edge is detected and latched by the internal HD pulse (See Section TRIGGER).
- Once Read scan starts, the sensor gets into the waiting state to latch the next TRIGGER rise.
- Until the read scan is completed, the next TRIGGER falling edge (read start) cannot be accepted.

**Figure 31: Consecutive Full Resolution Mode**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Seamless Frame Rate / Integration Time Change

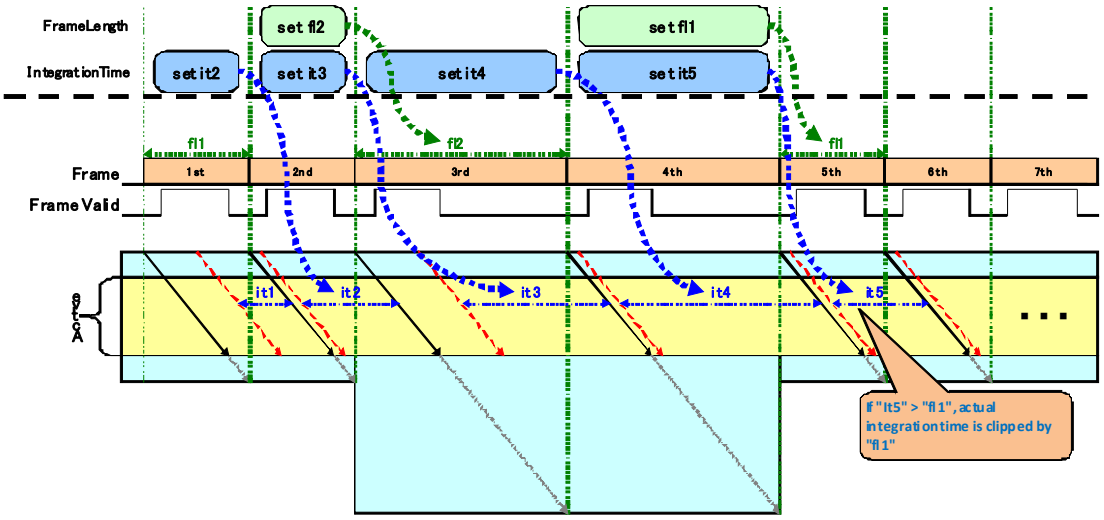
### Features

- The video frame rate varies among 120 fps, 60 fps, and 30 fps as a special feature.
- Seamless frame rate change available
- This operation is suitable for the video modes where the AR1411HS is operating as a master device.
- No extra offset time is required when the frame rate changes. Therefore, when the frame rate is changed as such 120 fps -> 60 fps -> 120 fps, Vertical Sync timing will be back to the original timing of the previous 120 fps operation.

### Control

- Both 'Coarse_integration_time' and 'Frame_length_lines' registers are updated within a frame for seamless frame rate change
- If 'Coarse_integration_time' is set larger than 'Frame line length', the integration time is clipped at the same value of 'Frame line length'.
- A new frame rate or new integration time will be reflected from the second frame counting from the frame when the registers are initially set.

**Figure 32: Seamless Frame Rate / Integration Time Change**





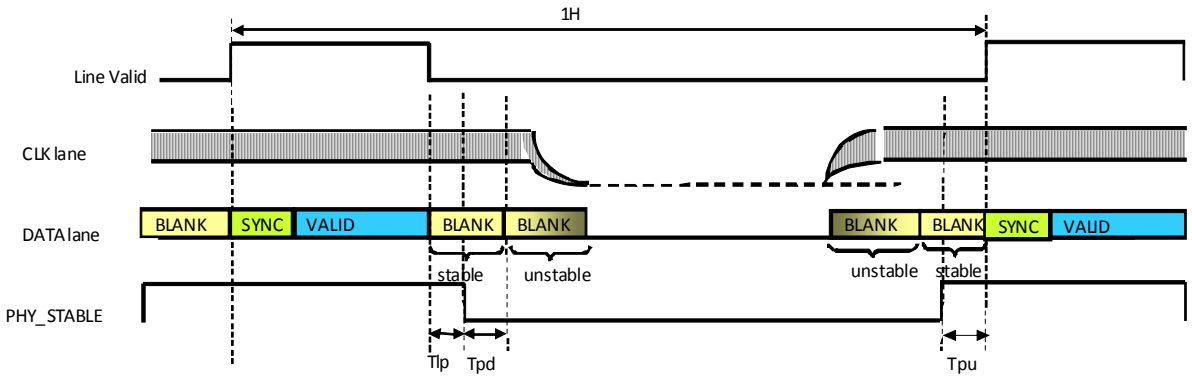

Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Power Save

HiSPi™ CLK/DATA lanes can be powered down during H-blanking inHD60_3:2, HD120_16:9_LP, EVF, Pre-Flash A and Pre-Flash B modes when power save mode is enabled. HiSPi clock is kept for at least 22 EXTCLK after Line Valid turning-off, and activated 5 EXTCLK earlier than Line Valid turning ON. Horizontal blanking in Full Resolution, Hi-Speed, and Super Hi-Speed modes is too short for the power save control sequence so that selecting power save control does not affect any operation in these modes.

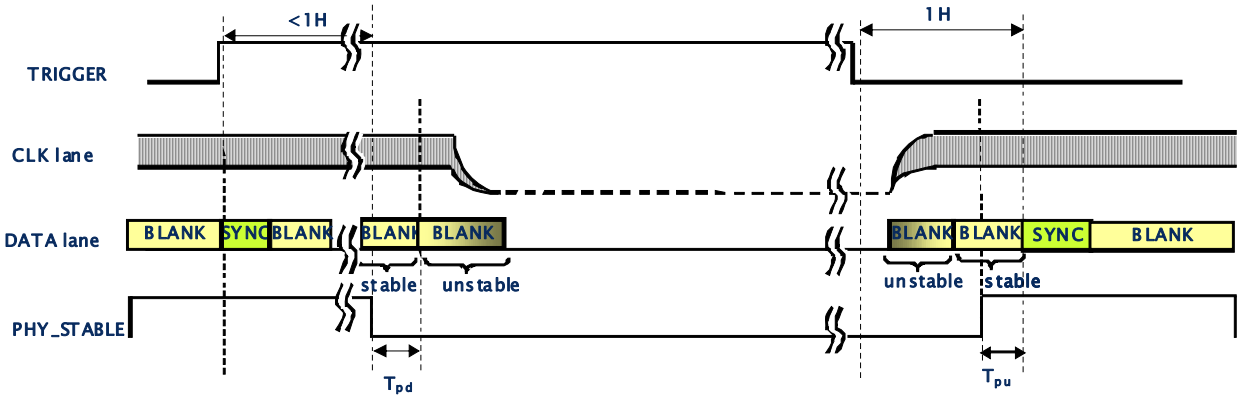
HiSPi™ CLK/DATA lanes are powered down during long integration when power save mode is enabled in Full Resolution mode. This feature is only valid in Full Resolution mode.

**Figure 33: Power Save in HD60_3:2, HD120_16:9_LP, EVF, Pre-Flash A and Pre-Flash B Modes**




Notes:
1. Tpd ≥ 2 EXTCLK duration
2. Tpu ≥ 2 EXTCLK duration
3. Tlp ≥ 8 EXTCLK duration

**Figure 34: Power Save in Full Resolution HD60_3:2_SLV, HD120_16:9_SLV Mode**




Notes:
1. Tpd ≥ 2 EXTCLK duration
2. Tpu ≥ 2 EXTCLK duration

**Note:** Power save capability is selectable by register. See “Power Save” on page 32. Power save is not applicable when TRIGGER is asserted HIGH while the previous frame is read out. In this case, the frame is operated without power saving.


Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

## Full Resolution HD120_16:9_SLV, HD60_3:2_SLVMode

Full Resolution Mode has two operating timings. Column FPN Readout Mode and Shortened REF Readout Mode. These are selected by setting the register. In both modes, image data follows the Resync code. The Resync code period can be changed by registers (row time basis).

For 59.94 fps, the sensor should detect the external TRIGGER every 4158 rows. Internal frame operation ends at the 4157th row and the sensor gets into the Wait Trigger state at the 4158th row, so that the external TRIGGER can be latched at the every 4158th row.

The difference between the two operating modes described below is the duration of REF rows. The Resync Code duration can be set via the register in a range from 0 to 156 rows.

When the Power Save function is in use in either mode, HiSPi output goes into the unknown or GND state during wait trigger status.

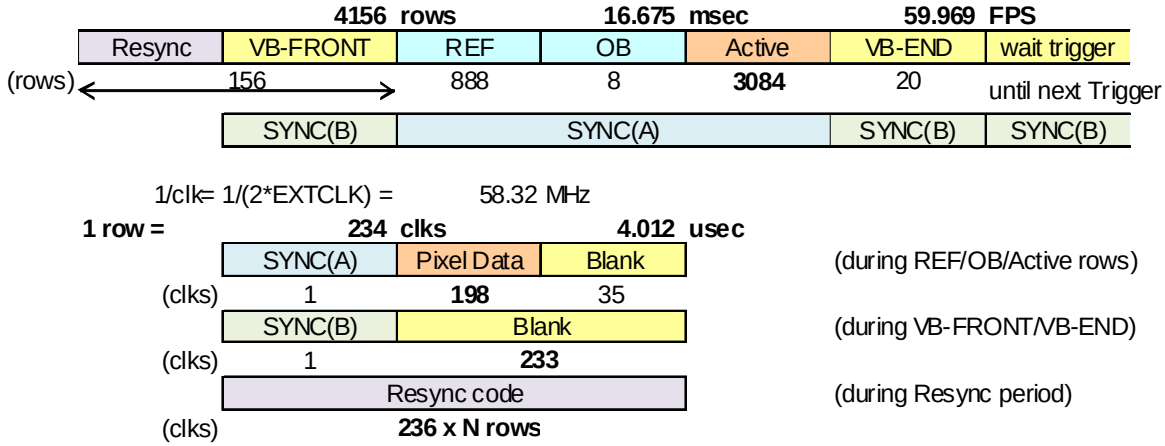
HD120_16:9_SLV mode and HD60_3:2_SLV mode are similar in operation as Full Resolution mode.

They are suitable for video capture but external trigger can control each frame timing.

### Full Res + Column FPN Readout Mode

Read out REF rows as many as possible to average column FPN data. Drawback is increase of delay time from TRIGGER fall edge to start of the Active readout.

**Figure 35: Full Resolution Mode - Column FPN Readout Mode Frame Timing**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

### Shortened REF Readout Mode

With minimized number of REF rows, delay from TRIGGER fall edge to start of the Active readout can be shortened. In addition, power can be reduce by saving power during the increased V-blanking time.

**Figure 36: Full Resolution Mode - Shortened REF Readout Mode Frame Timing Option B**

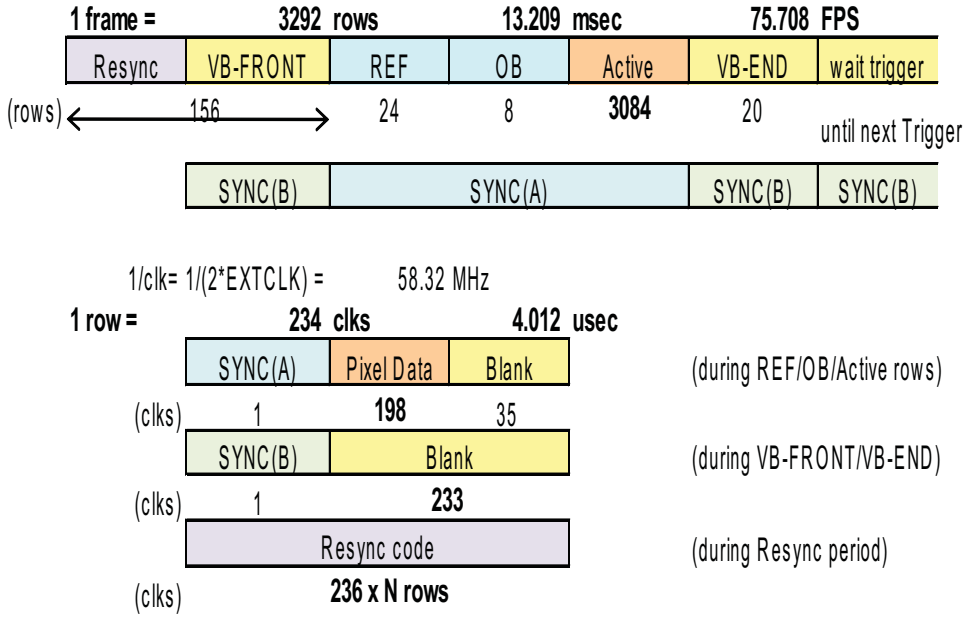
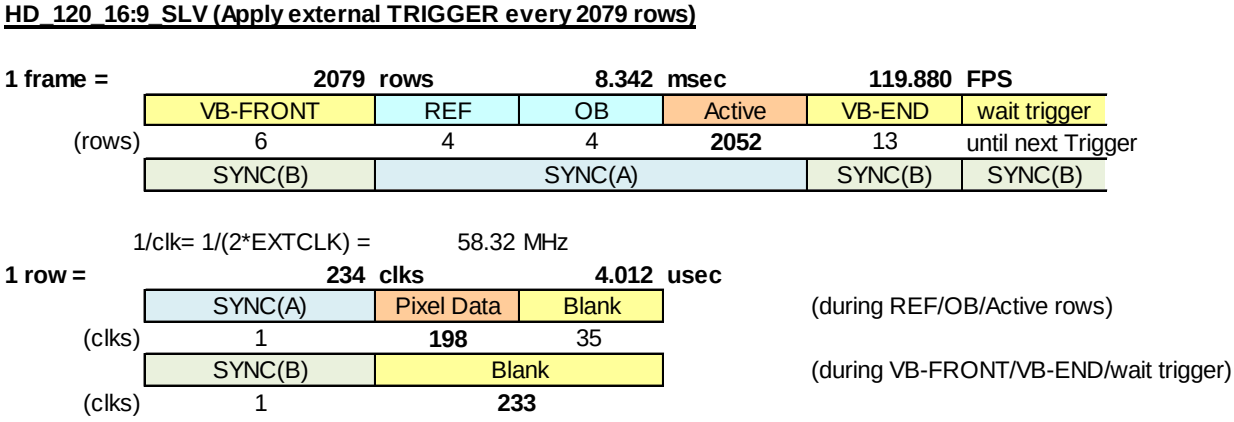


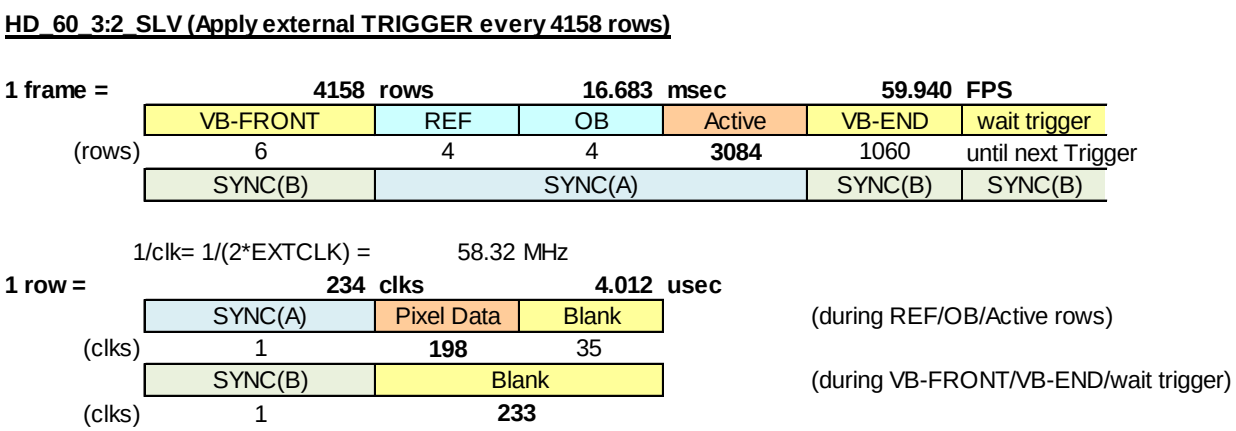

**Figure 37: HD_120_16:9_SLV Mode Frame Timing**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 38: HD_60_3:2_SLV Mode Frame Timing**




## Nesting Scan

To match the 1/80 sec frame readout time requirement, a unique row addressing feature called “Nesting Scan” is introduced in the AR1411HS.

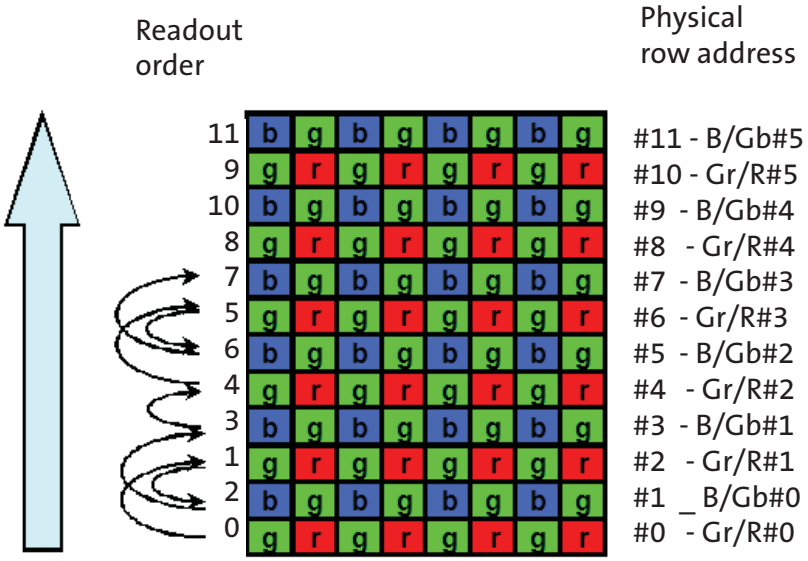
### Nesting Scan

In the Nesting Scan scheme, the two adjacent rows of the same color are read out then two adjacent rows in another color plane follow. When referring to row address sequence, the operation is as shown as:

Row #0, #2, #1, #3,…, '2n', 2(n+1)', '2n+1', '2(n+1)+1', …

By using this scheme, a faster pixel readout performance is realized. On the other hand, the Nesting Scan image output requires a special signal decoding with a backend processor.

**Figure 39: Full Resolution/HD60_3:2_SLV/HD120_3:2_SLV Mode Vertical Readout**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Video Modes

AR1411HS has 7 video modes:

- HD60_16:9_LP
- HD60_3:2
- EVF
- Pre-Flash A
- Pre-Flash B
- Hi-speed
- Super high-speed.

HD60_16:9_LP, HD60_3:2, EVF modes operate at 59.94 frames/sec.

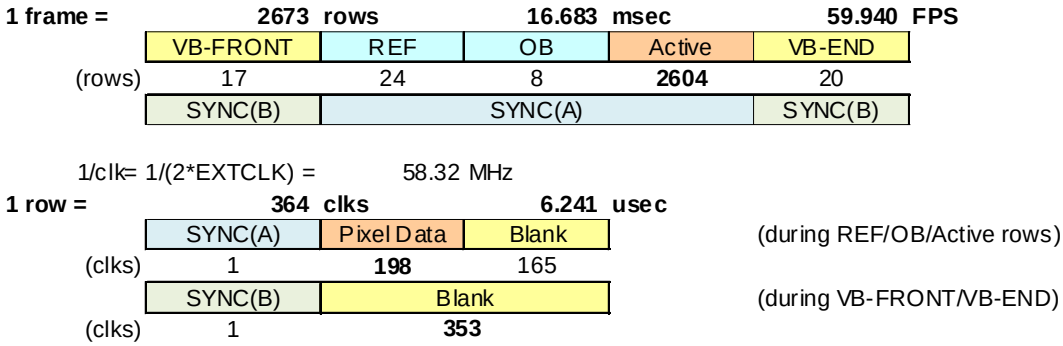
Pre-Flash A, Pre-Flash B modes operate at 119.8 frames/sec.

Hi-Speed and Super high-speed modes operate at 401.9 frames/sec and 1221.7 frames/sec.

VB-END for 20 rows was implemented in all video modes.

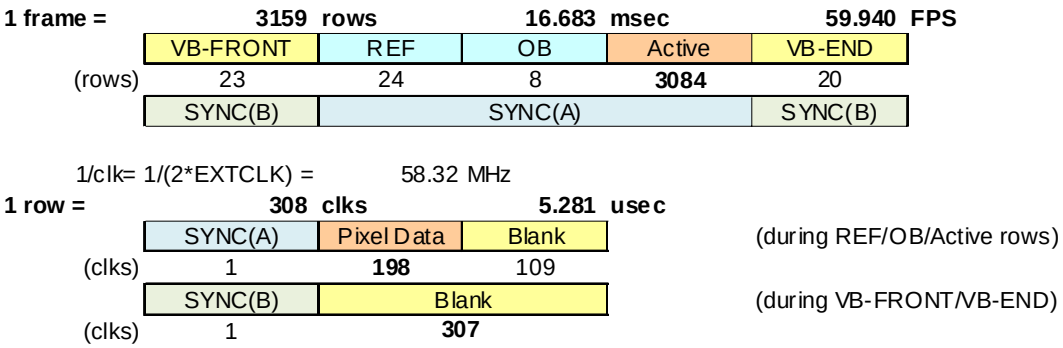
### HD60_16:9_LP Mode

**Figure 40: HD60_16:9_LP Mode Frame Timing**




### HD60_3:2 Mode

**Figure 41: HD60_3:2 Mode Frame Timing**

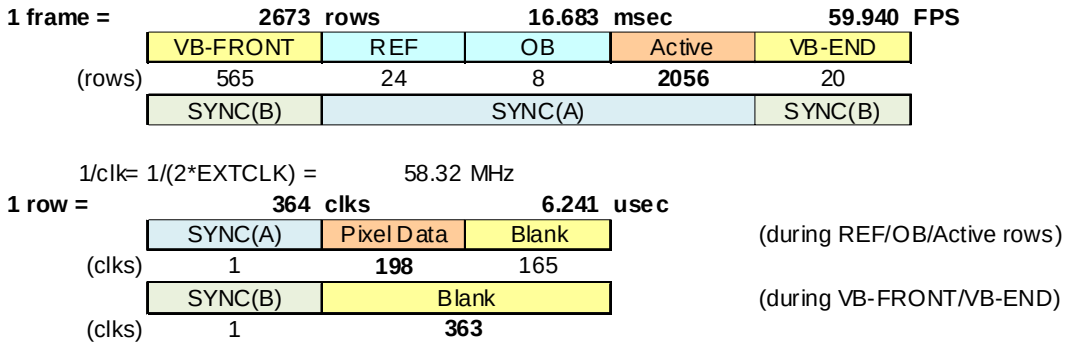




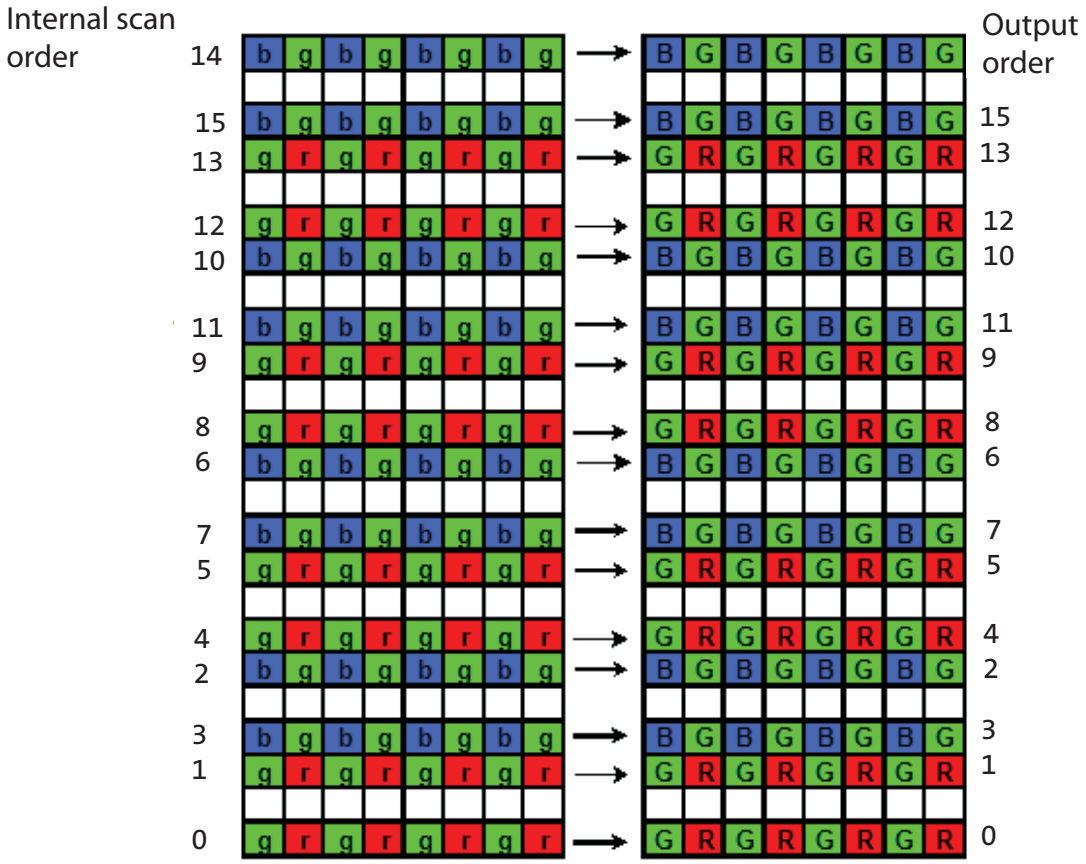

Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

## EVF Mode

### Figure 42: EVF Mode Frame Timing




### Figure 43: EVF Mode Vertical Read Out





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

### Pre-Flash A Mode

**Figure 44: Pre-Flash A Mode Frame Timing**

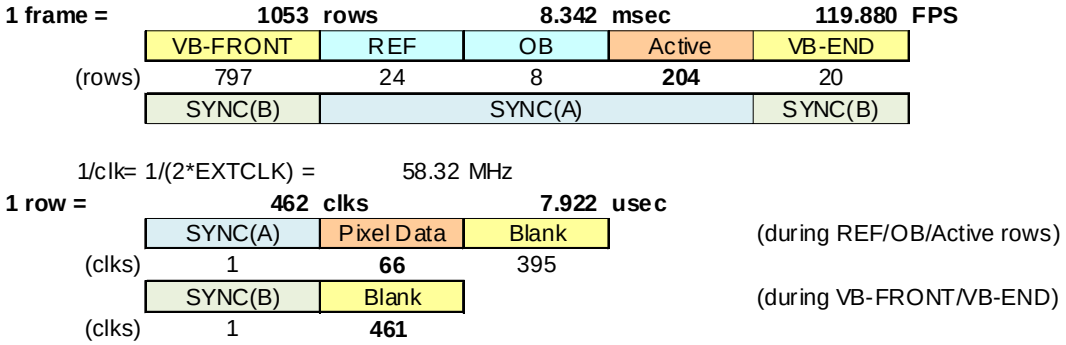
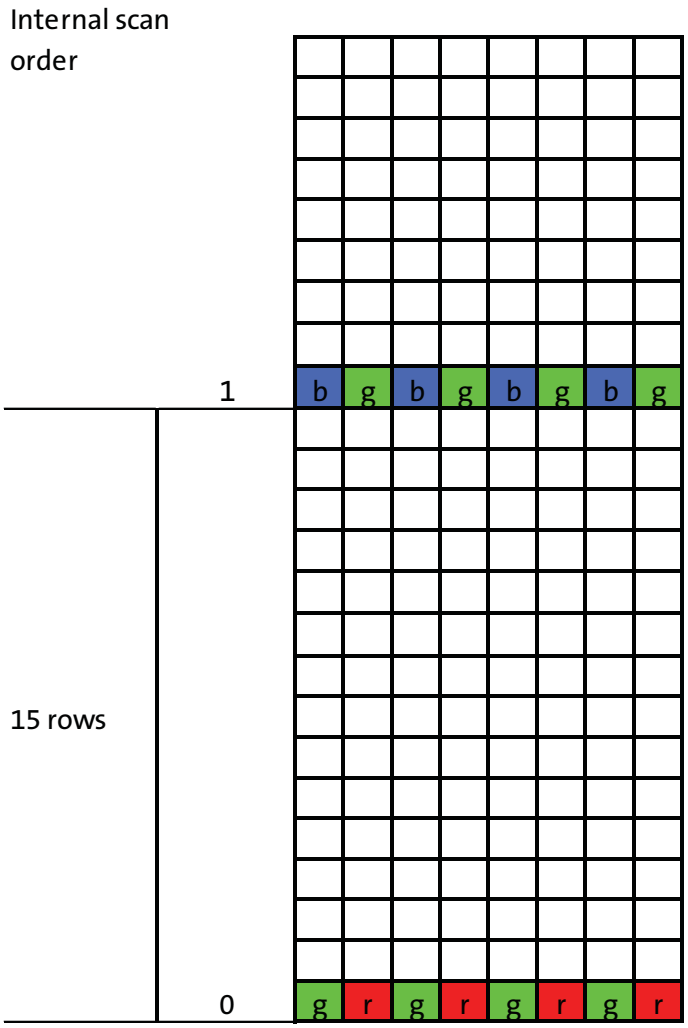



**Figure 45: Pre-Flash A Mode Vertical Read Out**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Pre-Flash B Mode

**Figure 46: Pre-Flash B Mode frame timing**

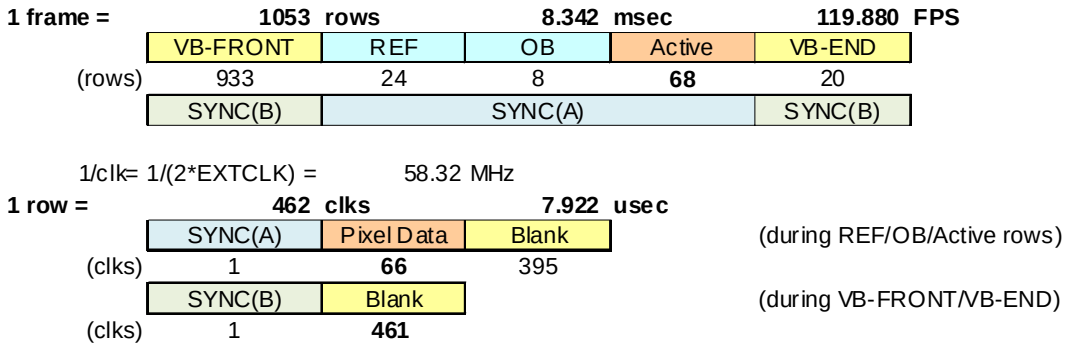
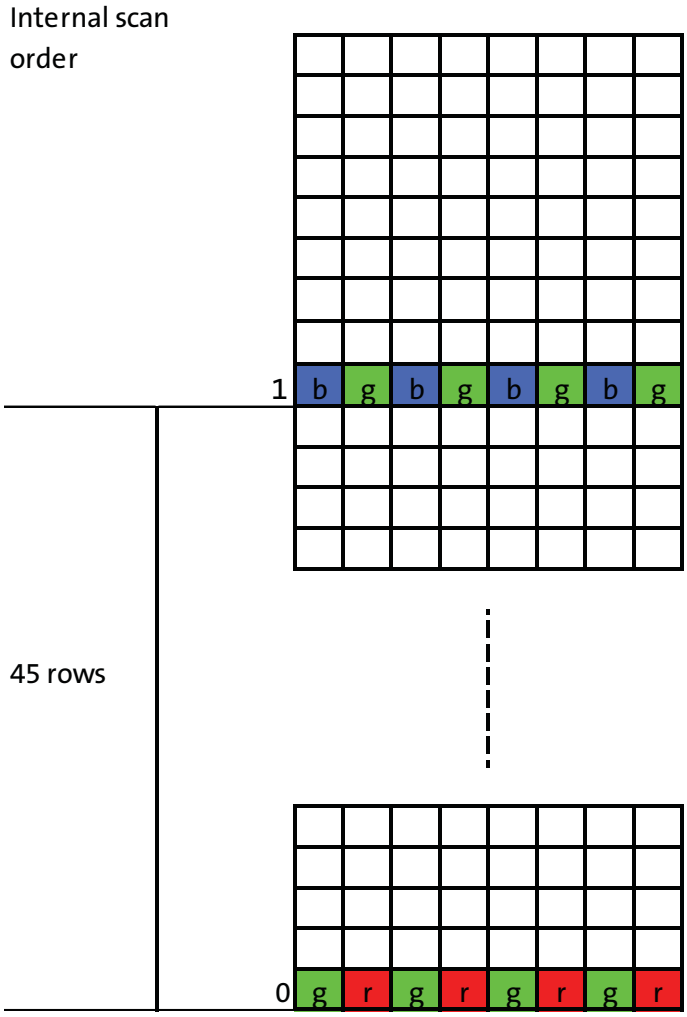


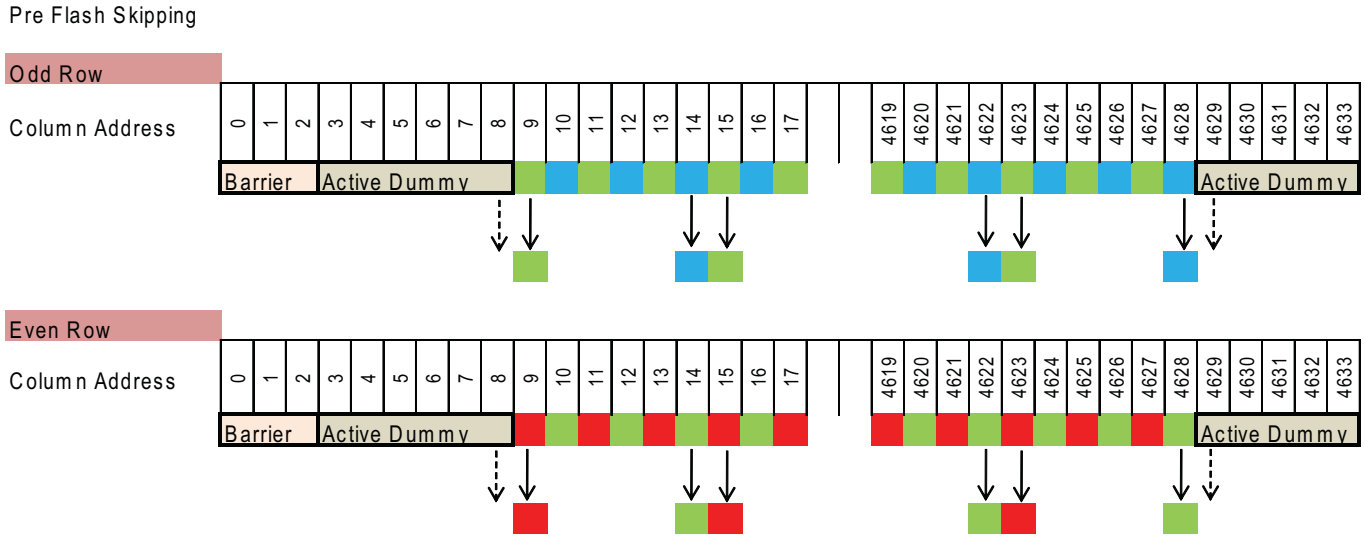

**Figure 47: Pre-Flash B Mode Vertical Read Out**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 48: Pre-Flash A Mode Horizontal Read Out**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

### Hi-Speed Mode

In Hi-Speed Mode, take care it needs to ignore last 2 red rows to keep image size.

**Figure 49: Hi-Speed Mode Frame Timing**

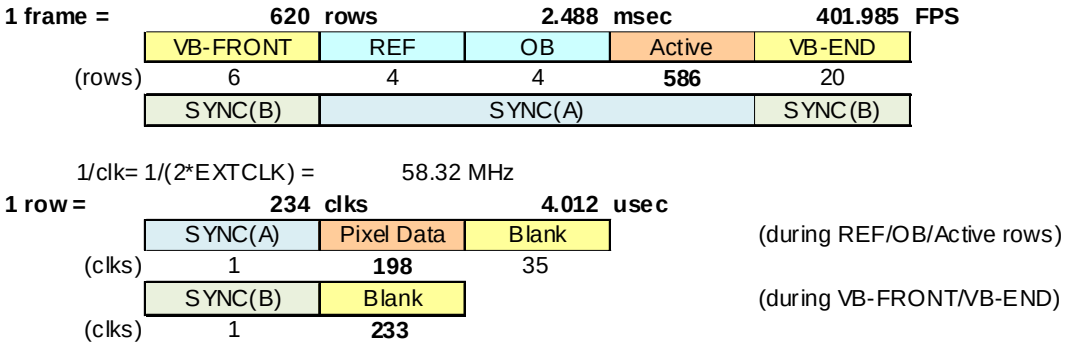
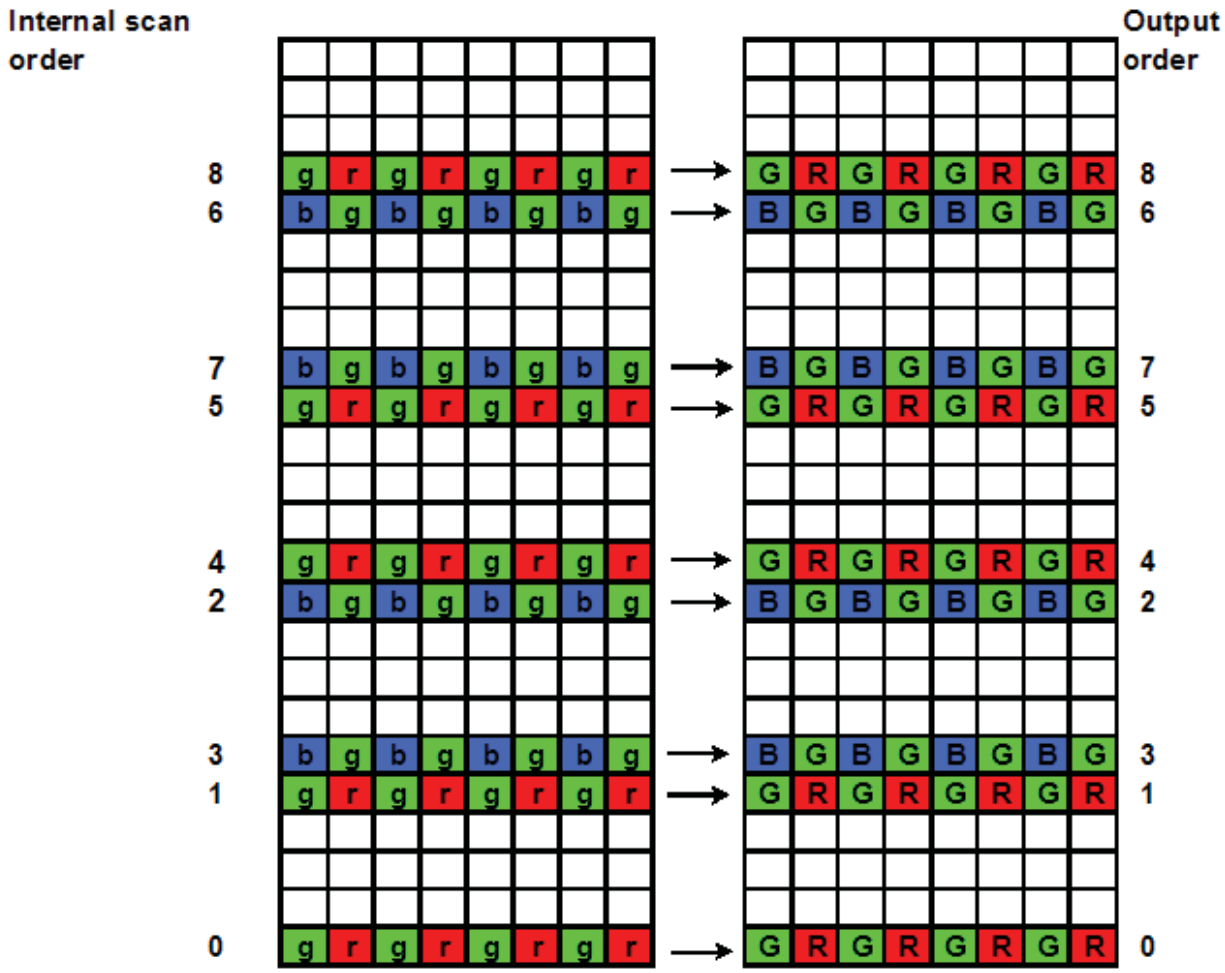



**Figure 50: Hi-Speed Mode Vertical Read Out**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Super Hi-Speed Mode

**Figure 51: Super Hi-Speed Mode Frame Timing**

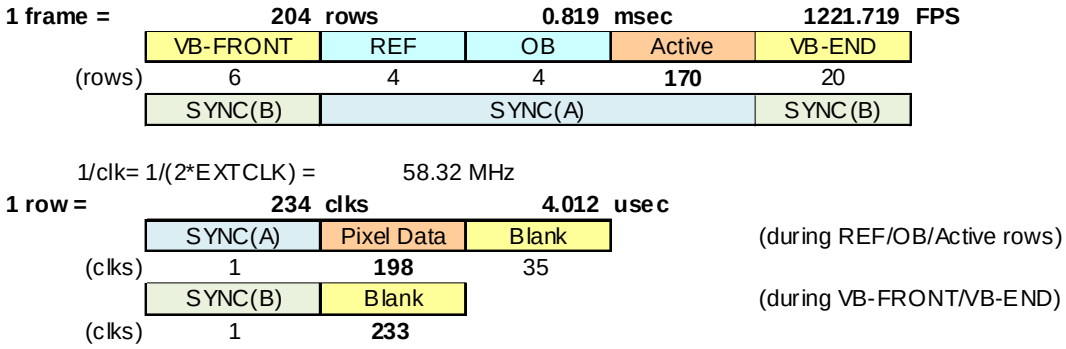
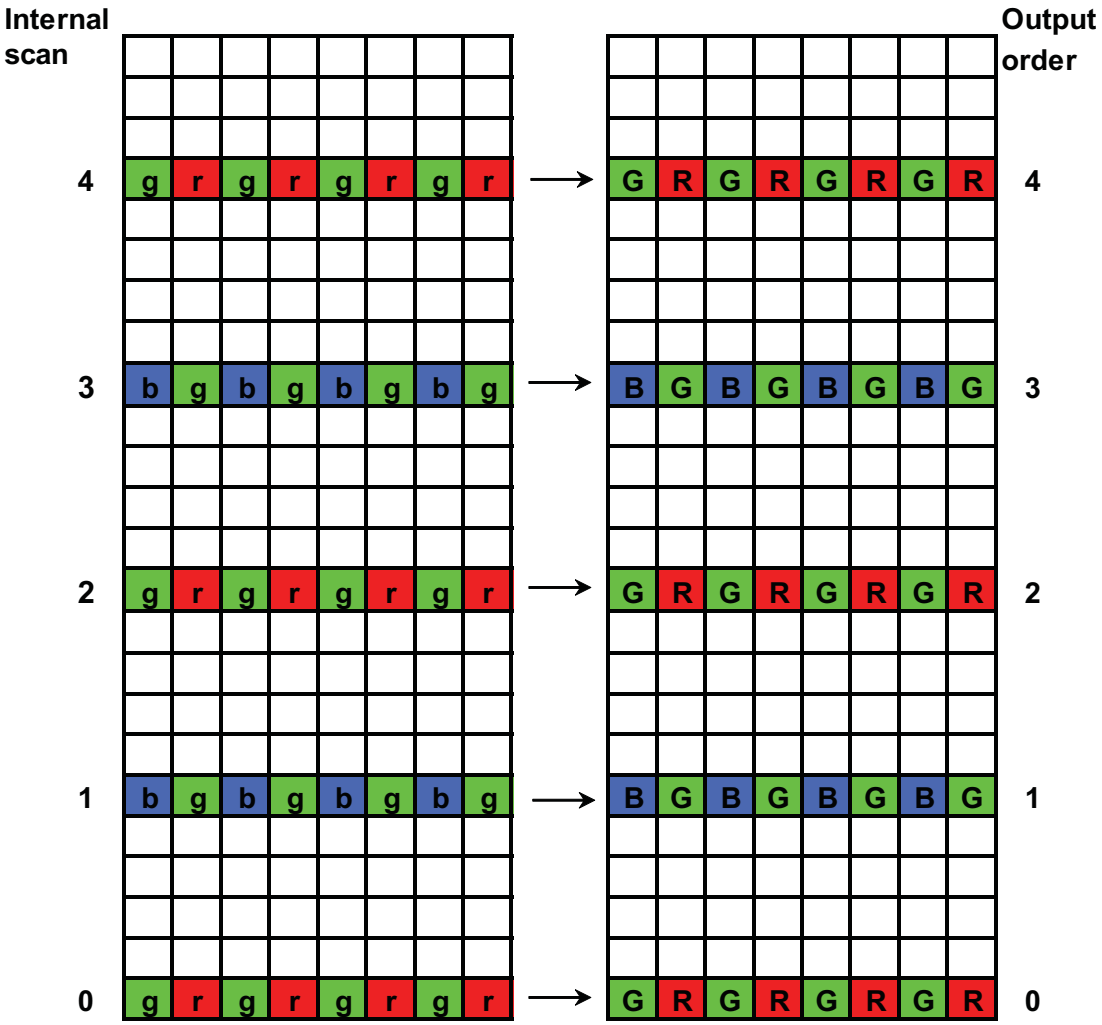



**Figure 52: Super Hi-Speed Mode Vertical Read Out**



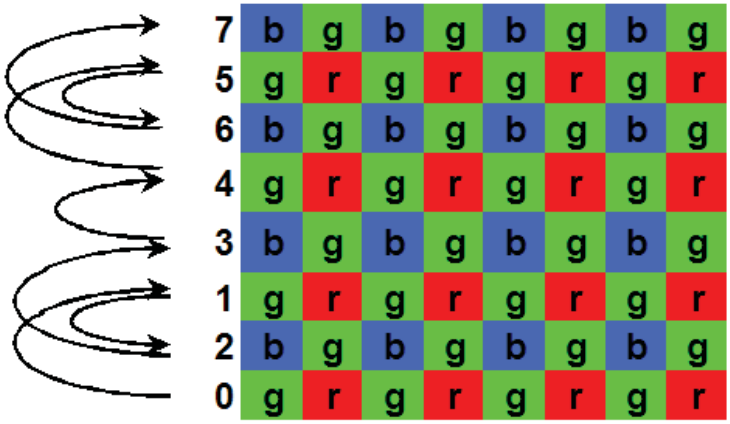


Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

### OB Without PD and OB Black Row Readout Order

All Ref rows (OB without PD rows) are read out regardless of operation modes as follows.

**Figure 53: Ref Rows Read Out**



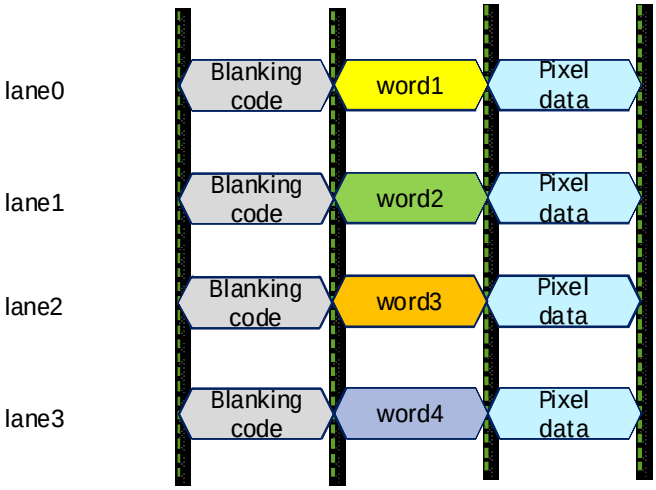

## Sync Code

In 12-bit mode, the sync code is identical to that of MT9J007CF. When 10-bit data compression mode is chosen, sync code is also reduced to 10-bit as shown in Table 26.

**Table 24: Sync Code**

| | | Word1 | Word2 | Word3 | Word4 |
|---|---|---|---|---|---|
| 12-bit | SYNC Active | 1111 1111 1111 | 0000 0000 0000 | 0000 0000 0000 | 1000 0000 0000 |
| | SYNC Blanking | 1111 1111 1111 | 0000 0000 0000 | 0000 0000 0000 | 1010 1011 0000 |
| 10-bit | SYNC Active | 11 1111 1111 | 00 0000 0000 | 00 0000 0000 | 10 0000 0000 |
| | SYNC Blanking | 11 1111 1111 | 00 0000 0000 | 00 0000 0000 | 10 1010 1100 |

**Figure 54: Sync Code Structure in a PHY**






Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

### Resync Code

When Resync Code output mode is chosen, Resync Code is asserted according to the operating mode.

- In video modes

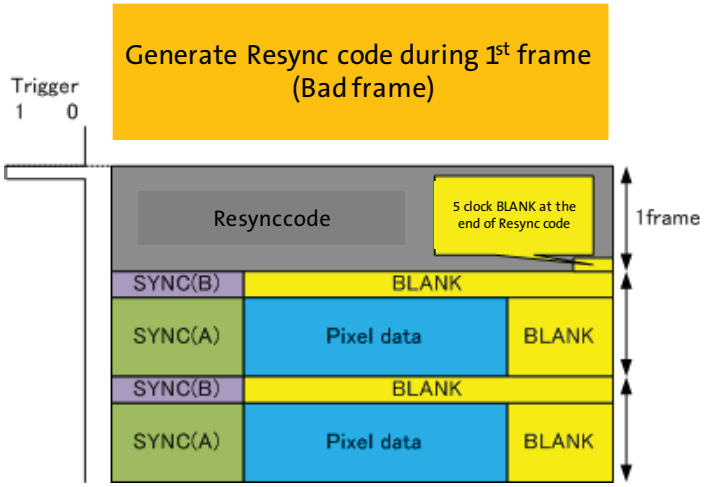
During the first frame after the TRIGGER (usually a bad frame)

- In Full Res mode

During a part of VB-front duration (variable, default value is 2672) after latch timing of the TRIGGER fall + 1row

During the Resync code duration, the HiSPi data lanes output a 0xAAA(12bit mode) and 0x2AA(10bit mode) value continuously, namely 101010…1010

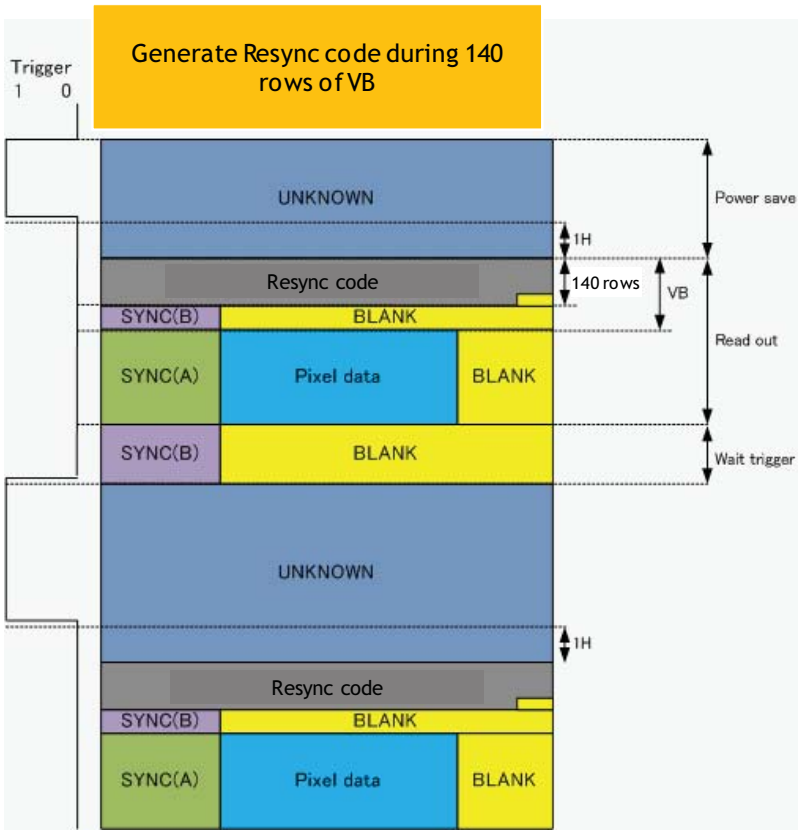
**Figure 55: Resync Code: Video Mode**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Figure 56: Resync Code: Full Resolution Mode**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Pixel Sensitivity Control

### Integration Time Control

The integration time in video mode is programmed by the electronic shutter control value in the register. Exposure time is set by

$$min(\text{coarse\_integration\_time or frame\_length\_lines} - 3) \times \text{row time (of current operating mode)} + t_{OFFSET} \quad \text{(EQ 1)}$$

**Table 25: Minimum/Maximum Integration Time**

| Mode | Minimum Trigger Width | Minimum Coarse_integration_time Register Value | Maximum Coarse_integration_time Register Value | $t_{OFFSET}$ (µs) |
|---|---|---|---|---|
| Full resolution | 3 rows | – | – | – |
| Full resolution with power save | 4 rows | – | – | – |
| HD60_16:9_SLV | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| HD60_3:2_SLV | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| EVF | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| Pre-Flash A | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| Pre-Flash B | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| Hi-Speed | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |
| Super Hi-Speed | 1 clk | 5 | frame_length_lines- 3 | ~0.2 |

On the other hand, integration time in Full resolution mode is determined by a pulse width of the external TRIGGER input.

**Table 26: Electrical Shutter Control Register Setting**

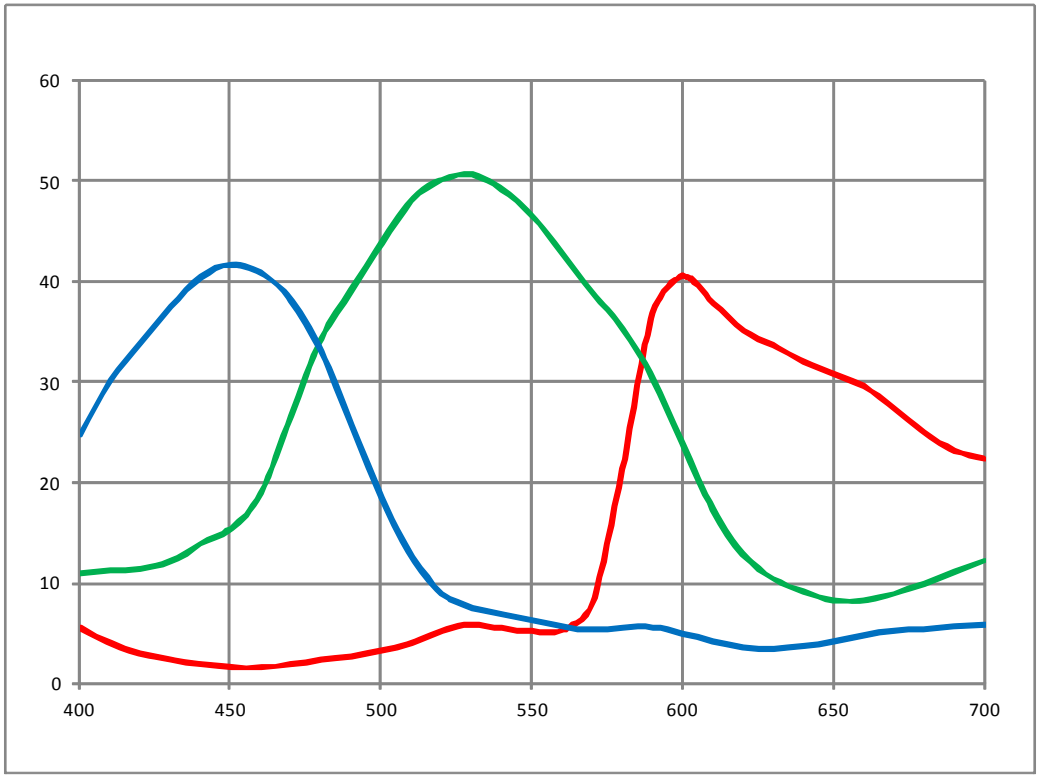
| Name | Bit | Default | |
|---|---|---|---|
| Coarse_integration_time | 15:0 | 0x03E7 | The exposure time; the time between when the rolling shutter resets a row and that row is read out, in rows. |
| Frame_length_lines | 15:0 | 0x0A71 | The number of lines per a frame including all output data such as the dark rows, vertical blanks etc. |



Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

## Pixel Performance

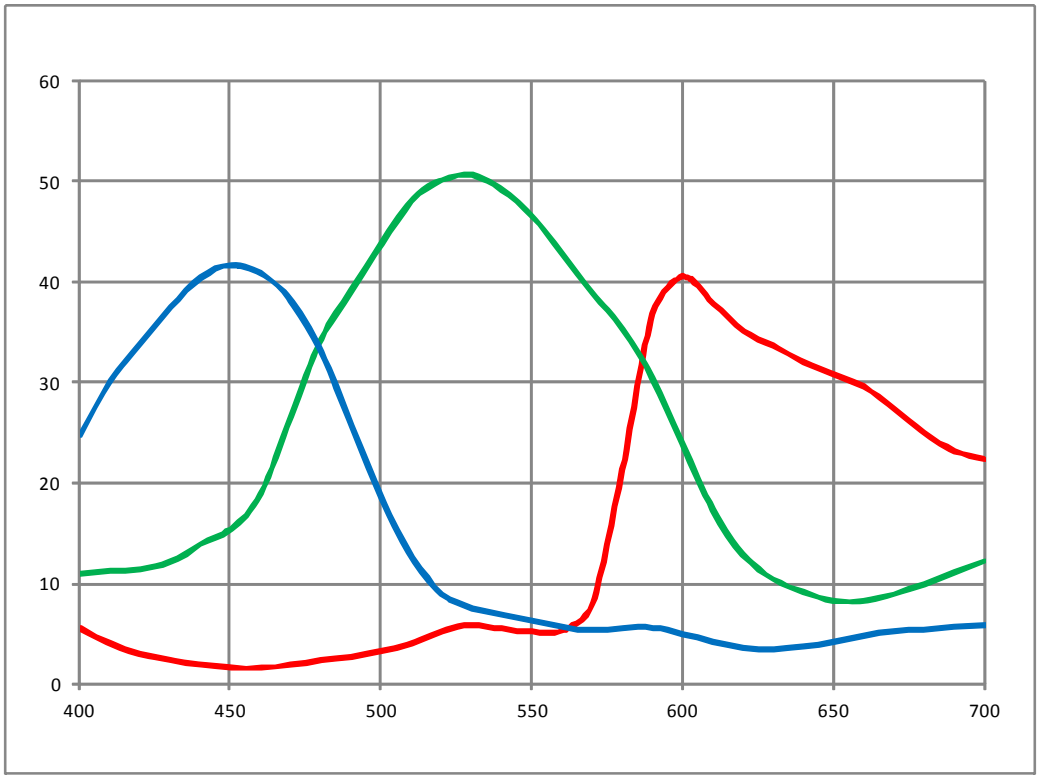
**Figure 57: Quantum Efficiency**






Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

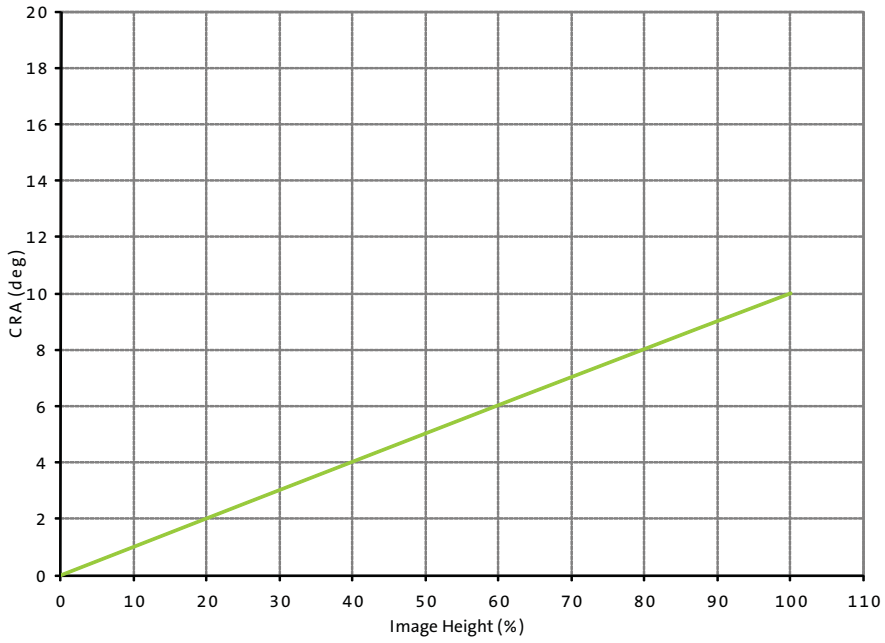
**Figure 58: Relative Spectral Response**





Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

**Table 27: Chief Ray Angle**




| Image Height | | CRA |
|---|---|---|
| (%) | (mm) | (deg) |
| 0 | 0 | 0 |
| 5 | 0.397 | 0.51 |
| 10 | 0.794 | 1.01 |
| 15 | 1.191 | 1.52 |
| 20 | 1.589 | 2.02 |
| 25 | 1.986 | 2.53 |
| 30 | 2.383 | 3.03 |
| 35 | 2.780 | 3.54 |
| 40 | 3.177 | 4.04 |
| 45 | 3.574 | 4.54 |
| 50 | 3.972 | 5.04 |
| 55 | 4.369 | 5.55 |
| 60 | 4.766 | 6.05 |
| 65 | 5.163 | 6.55 |
| 70 | 5.560 | 7.04 |
| 75 | 5.957 | 7.54 |
| 80 | 6.355 | 8.04 |
| 85 | 6.752 | 8.53 |
| 90 | 7.149 | 9.03 |
| 95 | 7.546 | 9.52 |
| 100 | 7.943 | 10.01 |

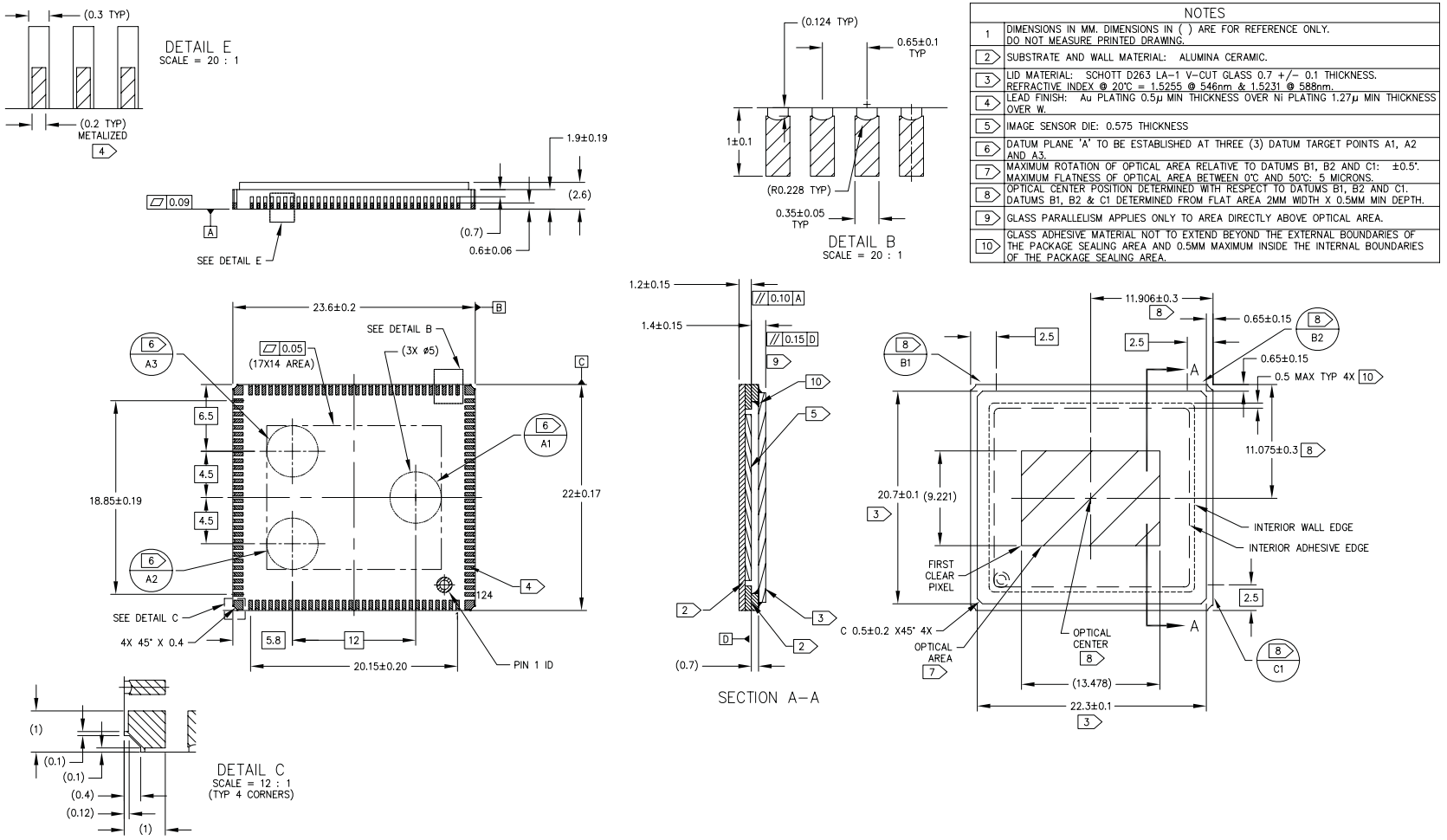

Aptina reserves the right to change products or specifications without notice..
©2013 Aptina Imaging Corporation All rights reserved.

# Mechanical Specification

## Package

The image sensor chip is assembled in 124-pin ceramic lead-free chip carrier (CLCC) package as shown in Figure 59.

### Figure 59: Package Schematic





Aptina reserves the right to change products or specifications without notice.
©2013 Aptina Imaging Corporation All rights reserved.

## Revision History

**Rev. A . . . . . 2/12/13**

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com
Aptina, Aptina Imaging, the Aptina logo, DR-Pix, and HiSPi are the property of Aptina Imaging Corporation
All other trademarks are the property of their respective owners.
Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.