1/2.3-Inch 18Mp CMOS Digital Image Sensor

AR1820HS Data Sheet, Rev. D

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- 1.25µm pixel with Aptina™ A-PixHS™, which brings BSI technology together with advanced sensor architecture pixel technology
- Simple 2-wire and 3-wire serial interface
- Auto black level calibration
- Full frame 18Mpixel, 12-bits at 24 fps for HiSPi 8 Lanes, and 10-bits 15fps for MIPI 4 Lanes.
- Support Full HD with 27.5% EIS, full of view, output 2448x1378 with X binning/Y(in-pixel) summing at 60 fps.
- Support 8M 16:9 HD cropping 77% FOV, 60 fps for HiSPi 8 Lanes, and 10-bits 30fps for MIPI 4 Lanes.
- Support for external mechanical shutter
- Support 1080p120 fps cropping 78% FOV
- Support for external LED or Xenon flash
- Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left–right and top–bottom image reversal, window size, and panning
- Data interfaces: (HiSPi™): programmable to 4 or 8 lanes HiSPi, high-speed serial pixel interface differential signaling support SLVS or sub-LVDS
- (MIPI): Programmable to 2-, 3-, or 4-lane serial mobile industry processor interface.
- On-chip phase-locked loop (PLL) oscillator
- Integrated position and color-based shading correction
- Slave mode for precise frame-rate control and for synchronizing multiple sensor
- On-chip temperature sensor, controlled by two-wire serial interface
- Supports Bit-Depth Compression for lower bandwidth receivers: A-Law Compression for HiSPi 12-10-12, 12-8-12, 10-8-10 and DPCM for MIPI: 10-8-10, 10-6-10

Applications

- Digital still cameras
- Digital video cameras
- Smart phones
- PC cameras
- Tablets

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/2.3-inch (4:3)
Pixel size		1.25µm x 1.25µm A-PixHS™ BSI
Entire array format		4912H x 3684V
Primary modes		4:3 - 18M full resolution at 24 fps (HiSPi-8L), 15 fps (MIPI-4L)
		16:9 - 14M at 30 fps (HiSPi-8L), 20 fps (MIPI-4L)
		16:9 - 8M at 60 fps (HiSPi-8L), 30 fps (MIPI-4L)
		16:9 - Full HD + 27.5%EIS at 60 fps
		16:9 - Full HD at 120 fps
Chief ray angle		0°, 11.4°, and 31°
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS) with global reset release (GRR)
Input clock frequency		6 - 54 MHz
Interface and maximum data rate		MIPI (4/3/2Lanes) or HiSPi (8/4-lanes) with 800 Mbps/lane
ADC resolution		12-bit, on-chip
Pixel data format		12/10-bit per pixel (RAW12 or RAW10)
Analog gain		1x – 8x
Responsivity		0.62 V/lux-sec (545nm)
Dynamic range		65.8 dB
SNRmax		36.3dB
Supply voltage	Analog (V_{AA})	2.7 - 3.1V (2.8V nominal)
	Digital (V_{DD})	1.14 - 1.3V (1.2V nominal)
	Pixel (V_{AA_PIX})	2.7 - 3.1V (2.8V nominal)
	Digital (V_{DD_1V8})	1.7 - 1.9V (1.8V nominal)
	I/O (V_{DD_IO})	1.7 - 1.9V (1.8V nominal) or 2.7 - 3.1V (2.8V nominal)
	Serial interface (V_{DD_TX})	0.3 - 0.6 V (0.4V nominal for HiSPi) 1.14 - 1.3 V (1.2V nominal for MIPI)
Power consumption		Refer to Table 3 on page 2
Package		10x10mm, 60 balls iBGA and Recon die

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Aptina without notice. Products are only warranted by Aptina to meet Aptina's production data sheet specifications.

Table 1: Key Performance Parameters

Parameter	Value
Operating temperature	-30°C to +70°C (at junction)
Storage temperature	-30°C to +80°C (at junction)

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
AR1820HSSC00SHEA0	0° CRA, HiSPi, plastic iBGA
AR1820HSSC12SHEA0	11.4° CRA, HiSPi/MIPI, plastic iBGA
AR1820HSSC31SMD20	31° CRA, MIPI, Recon die

Modes of Operation and Power Consumption

Table 3: HiSPi Modes of Operation and Power Consumption

Mode	Active Readout Window (col x row)	Sensor Output Resolution (col x row)	Readout Mode	FOV	FPS	Typical Power Consumption (mW)
4:3 Snapshot Mode						
Full Resolution - 18Mp	4912x3684	4912x3684	Full mode	100%	24	495
4:3 Video Mode						
Low Power Preview 1	4896x3688	1224x922	x-ana-bin2scale2 y-ana-sum2skip2	>99%	60	275
Low Power Preview 2	4896x3672	1632x1224	x-ana-skip2+scaling1.5 y-ana-skip3	>99%	60	319
Low Power Preview3	4896x3672	1632x448	x-ana-skip2+dig-scale 1.5 y-ana-skip8	>99%	30	TBD
HS-QVGA	4896x3664	306x229	x-ana-bin2skip2+x-dig-scale4 y-ana-skip16	99%	400	461
16:9 Video Mode						
14M HD	4912x2764	4912x2764	Full mode	100% HD aspect	30	457
8M HD	3768x2124	3768x2124	Full mode	>77% HD aspect	60	606
HD 1080p60 + 20+%EIS	4896x2756	2448x1378	x-ana-bin2 y-ana-sum2	>99% HD aspect	60	364
Ultra-Fast HD 1080p120	3840x2160	1920x1080	x-ana-bin2 y-ana-sum2	>78% HD aspect	120	498

Notes: 1. 800 Mbps/lane max. HiSPi 8-lane data transfer rate.
2. Nominal voltages with external regulator.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 4: MIPI Modes of Operation and Power Consumption

Mode	Active Readout Window (col x row)	Sensor Output Resolution (col x row)	Readout Mode	FOV	FPS	Typical Power Consumption (mW)
4:3 Snapshot Mode						
Full Resolution 18Mp	4912x3684	4912x3684	Native	100%	15	445
16Mp	4800x3520	4800x3520	Native	>97%	16	TBD
4:3 Video Mode						
Low Power Preview 1	4896x3688	1224x922	x-ana-bin2scale2 y-ana-sum2skip2	>99%	60	410
Low Power Preview 2	4896x3672	1632x1224	x-ana-skip2+scaling1.5 y-ana-skip3	>99%	60	335
16:9 Video Mode						
14M HD	4912 x 2764	4912 x 2763	Native	100% HD aspect	20	406
8M QuadHD 1	3840x2160	3840x2160	native crop	>77% HD aspect	32	434
8M QuadHD 2	4096x2160	4096x2160	native crop	>83% HD aspect	30	434
HD 1080p60 + 20+%EIS	4896x2756	2448x1378	x-ana-bin2 y-ana-sum2	>99% HD aspect	60	438
Ultra-Fast HD 1080p120	3840x2160	1920x1080	x-ana-bin2 y-ana-sum2	>78% HD aspect	120	472

Notes: 1. 800 Mbps/lane max. MIPI 4Lane data transfer rate.
2. Measured at nominal voltage considering dynamic power saving.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table of Contents

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

List of Figures

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

List of Tables

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

General Description

The Aptina™ AR1820HS is a 1/2.3-inch CMOS active-pixel digital imaging sensor with 1.25µmx1.25µm A-PixHS™ BSI Pixel, which brings Aptina's backside illuminated (BSI) pixel technology, together with an advanced high-speed sensor architecture to enable a new class of high performance high speed and low power cameras. It can support 18-megapixel (4912H x 3684V) digital still images at 24 fps and a 1080p plus additional 27 percent pixels for electronic image stabilization (2448H x 1378V) in digital video mode at 60 fps and 1080p120 fps. The AR1820HS sensor is programmable through a simple two-wire serial (or new 3-wire) interface, and has very low power consumption.

The AR1820HS digital image sensor die features Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

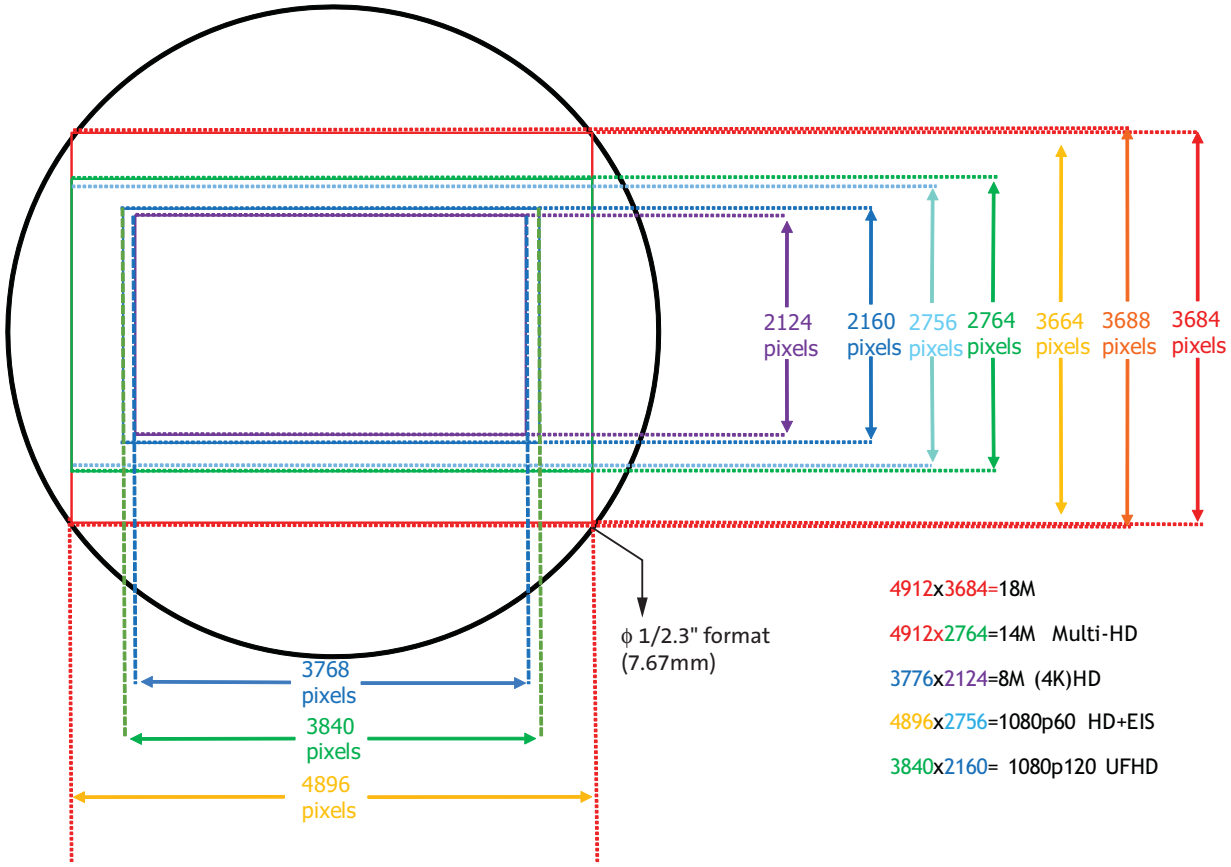
When operated in its default mode (4:3 still-mode), the sensor generates a full resolution image at 24 frames per second (fps) using the HiSPi serial interface. An on-die analog-to-digital converter (ADC) generates a 12-bit value for each pixel.

Functional Overview

In order to meet higher frame rates in AR1820HS sensor, the architecture has been re-designed. The analog core has a column parallel architecture with four data paths. Digital block has been re-architected to have four data paths.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 1: Optical Format - High-Resolution Still Image Capture + Full HD Video



The core of the sensor is an 18Mp active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing gain), and then through an ADC. The output from the ADC is a 10- or 8-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

The pixel array contains optically active and light-shielded ("dark") pixels. The dark pixels are used to provide data for on-chip offset-correction algorithms ("black level" control).

The sensor contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers can be accessed through a two-wire serial interface.

The output from the sensor is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

The control registers, timing and control, and digital processing functions shown in Figure 1 on page 11 contain the following logical parts:

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

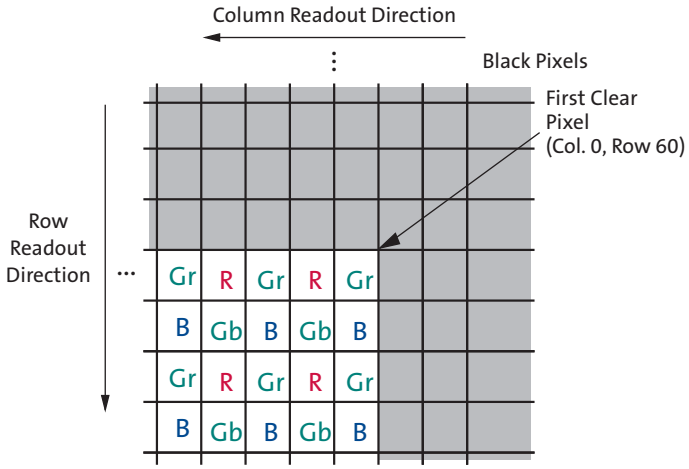
- A digital shading correction block to compensate for color/brightness shading introduced by the lens or chief ray angle (CRA) curve mismatch.
- Additional functionality is provided. This includes a horizontal image scaler, a limiter, a data compressor, and a serializer.

A flash output signal is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time. Additional I/O signals support the provision of an external mechanical shutter.

Pixel Array

The sensor core uses a Bayer color pattern, as shown in Figure 2. The even-numbered rows contain green and red pixels; odd-numbered rows contain blue and green pixels. Even-numbered columns contain red and green pixels; odd-numbered columns contain blue and green apixels.

Figure 2: Pixel Color Pattern Detail (Top Right Corner)

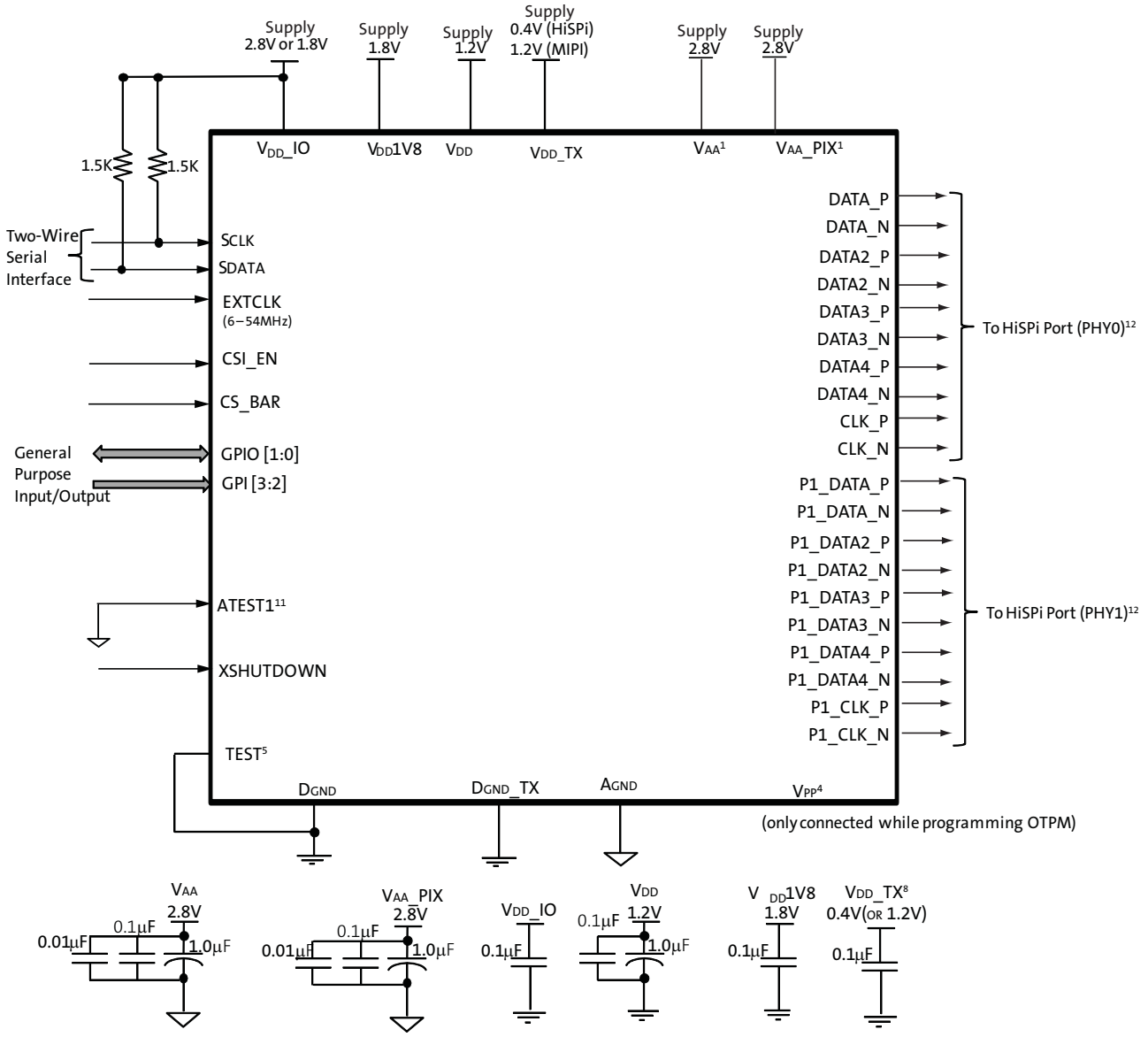


Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Typical Connections

The chip supports HiSPi or MIPI output protocol. HiSPi can be configured in 8 or 4 lanes. There are no parallel data output ports. MIPI can be configured as 2, 3, or 4 Lanes, but 8 Lanes MIPI is not available. There are no parallel data output ports.

Figure 3: Typical Application Circuit—HiSPi Connection



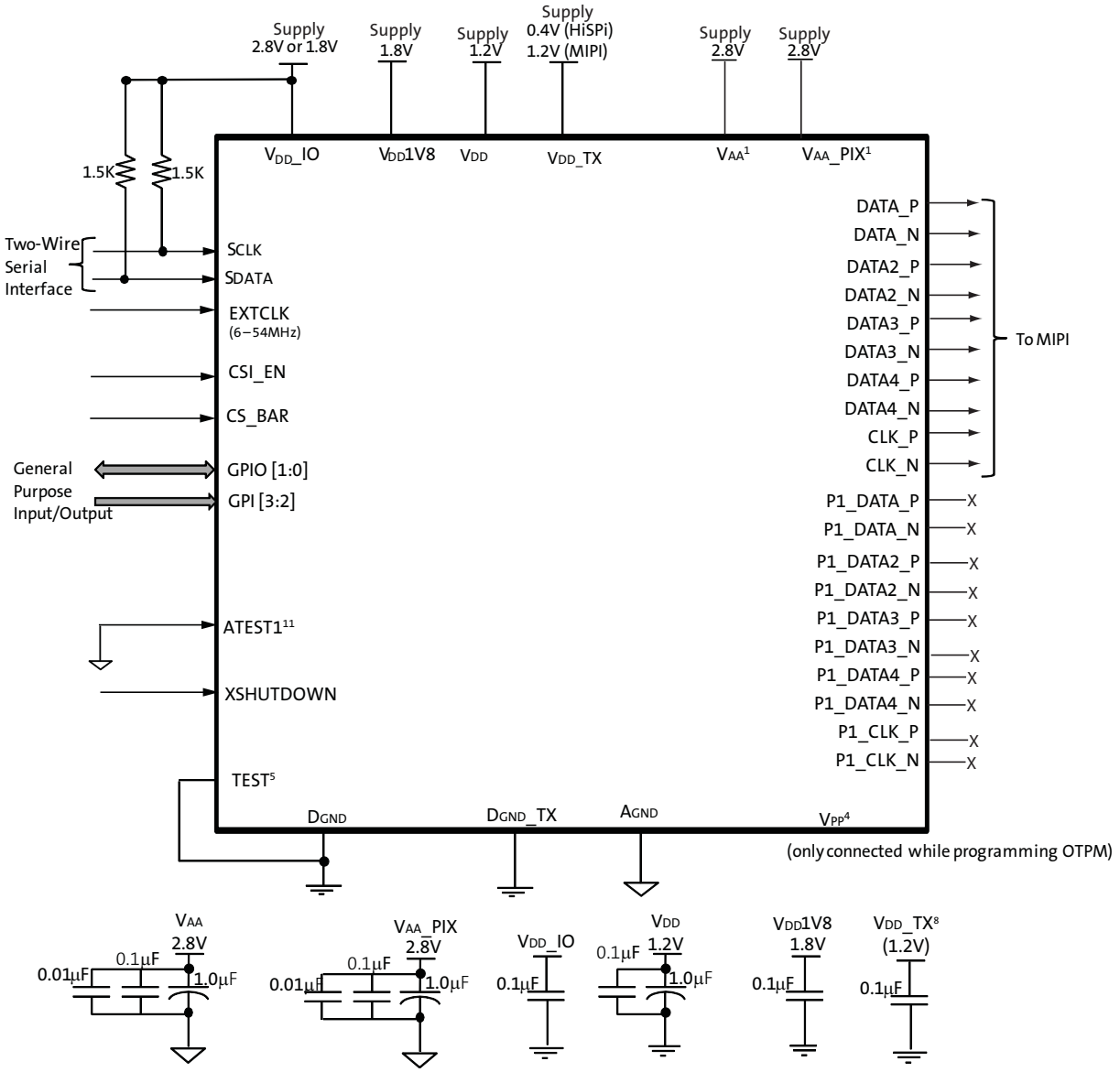
Notes:
1. All power supplies must be adequately decoupled. The order of preference is as follows: 2.8V supply - 1.0µF, 0.1µF and then 0.01µF; 1.2V supply - 1.0µF and 0.1µF; 1.8V supply - 0.1µF
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VPP, 6-7V, is used for programming OTPM. This pad is left unconnected if OTPM is not to be used.
5. TEST pin must be tied to DGND.
6. VDD_1V8 can be combined with VDD_IO,ONLY if VDD_IO = 1.8V (subLVDS mode).

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

7. V_{DD}_IO must be set to 1.8V when subLVDS is being used
8. Supply 0.4V to V_{DD}_TX without internal regulator, it can optionally program to be supplied by 1.2V with internal regulator enable (higher power consumption).
9. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the AR1820HS demo headboard schematics for circuit recommendations.
10. TEST signals must be tied to D_{GND} for normal sensor operation
11. ATEST1 must be connected to the ground.
12. Termination for HiSPi (DATA[4:1]_P, DATA[4:1]_N, P1_DATA[4:1]_P, P1_DATA[4:1]_N) and CLK (CLK_P, CLK_N, P1_CLK_P, P1_CLK_N,) is 100 Ω .

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 4: Typical Application Circuit—MIPI Connection



1. All power supplies must be adequately decoupled. The order of preference is as follows: 2.8V supply - 1.0µF, 0.1µF and then 0.01µF; 1.2V supply - 1.0µF and 0.1µF; 1.8V supply - 0.1µF
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VPP, 6-7V, is used for programming OTPM. This pad is left unconnected if OTPM is not to be used.
5. TEST pin must be tied to DGND.
6. VDD_1V8 can be combined with VDD_IO,ONLY if VDD_IO = 1.8V (sub-LVDS mode).
7. VDD_IO can be set to 1.8V or 2.8 (higher power)

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

8. Supply 1.2V to VDD_TX.
9. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the AR1820HS demo headboard schematics for circuit recommendations.
10. TEST signals must be tied to DGND for normal sensor operation
11. ATEST1 must be connected to the ground.
12. Termination for MIPI (DATA[4:1]_P, DATA[4:1]_N,) and CLK (CLK_P, CLK_N) is 100Ω

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Signal Descriptions

AR1820HS has 60 pads; pin connections are solder balls in a grid pattern on the package bottom. It has only serial outputs. The part may be configured as HiSPi or MIPI with different bit depths. The pad description is tabulated in Table 5:

Table 1: Pad Descriptions

Pad Name	Pad Type	Description
Sensor Control		
EXTCLK	Input	Master clock input; PLL input clock. 6 MHz - 54 MHz.
GPIO0	Input/Output	General Input and one Output function include: a. (Default Output) Flash b. (Input) all options in GPI2 Default function is output flash, but the output driver is disable after reset . If not used, can be left floating.
GPIO1	Input/Output	General Input and 2 Output functions include: a. (Default Output) Shutter b. (Output) 3-D daisy chain communication output c. (Input) all options in GPI2 Default function is output shutter, but the output driver is disable after reset . If not used, can be left floating.
GPI2	Input	General Input; After reset, these pads are powered down by default. Functions include: a. SADDR, second two-wire serial interface device address b. Trigger signal for Slave Mode c. Standby
GPI3	Input	General Input; After reset, these pads are powered-down by default; this means that it is not necessary to bond to these pads. Functions include: a. 3-D daisy chain communication input b. All options in GPI2
ATEST1	Input	Must be conected to ground.
TEST	Input	Must be conected to ground
Two-wire Serial Interface		
SCLK	Input	Serial clock for access to control and status registers.
SDATA	I/O	Serial data for reads from and writes to control and status registers.
Serial Output		
DATA[4:1]P	Output	Differential serial data (positive) for PHY0.
DATA[4:1]N	Output	Differential serial data (negative) for PHY0.
CLK_P	Output	Differential serial clock (positive) for PHY0.
CLK_N	Output	Differential serial clock (negative) for PHY0.
P1_DATA[4:1]P	Output	Differential serial data (positive) for PHY1.
P1_DATA[4:1]N	Output	Differential serial data (negative) for PHY1.
P1_CLK_P	Output	Differential serial clock (positive) for PHY1.
P1_CLK_N	Output	Differential serial clock (negative) for PHY1.
XSHUTDOWN	Input	Asynchronous active LOW reset. When asserted, data output stops and all internal registers are restored to their factory default settings. This pin will turn off the digital power domain and is the lowest power state of the sensor. Must be high during normal operation.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 1: Pad Descriptions

Pad Name	Pad Type	Description
Three-wire Serial Interface		
CS_BAR	Input	CS_BAR = 0 to enable 3-wire interface
CS_EN	Input	CSI_EN should be "1" in order to enable 3-wire interface.
Power		
VPP	Supply	High-voltage pin for programming OTPM for production. This pin can be left floating during normal operation.
VAA[4:1], VAA_PIX, AGND[4:1], AGND_PIX, VDD_IO_[3:1], VPP, DGND[5:1] VDD[6:1], VDD_TX, DGND_TX[2:1], VDD_1V8	Supply	Power supply. The domains are specified in the next table. The brackets indicate the number of individual pins.

There are standard GPI and GPIO pads, 2 each. Chip can also be communicated to through the two-wire serial interface.

The chip has four unique power supply requirements: 0.4V, 1.2V, 1.8V,and 2.8V. These are further divided and in all there are seven power domains and five independent ground domains from the ESD perspective.

Table 2: Independent Power and Ground Domains

Pad Name	Power Supply	Description	Note
Supply			
VDD_IO	1.8 or 2.8	IO and HiSPi IO	VDD_IO must be set to 1.8V when subLVDS is being used
VAA	2.8	Analog core	Separate from other 2.8V if possible
VAA_PIX	2.8	Pixel array	Separate from other 2.8V if possible
VDD	1.2	Digital core	
VDD_PHY	1.2	PHY core	
VDD_1V8	1.8	OTPM core	
VDD_TX	0.4 or 1.2	Serial interface	Separate from other 1.2V
VDD_PLL	1.2	PLL	
Ground			
AGND	0	Analog ground	
AGND_PIX	0	Pixel ground	
DGND	0	Digital ground	
DGND_TX	0	Serial Interface Ground	

Note: VPP is used for programming OTPM, not for normal sensor operation. This pad is left unconnected if OTPM.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 3: Usage Case for Power Rail and Internal Regulator

Case #	Serial interface		Internal Regulator	R 0X31BE [3:2]	V_{DD_IO}	V_{DD_TX}	V_{DD1p8}	V_{AA}	V_{AA_PIX}	V_{DD}	V_{DD_PHY}	V_{DD_PLL}
1	HISPI	SLVS	enable	0x00	2.8	1.2	1.8	2.8	2.8	1.2	1.2	1.2
2	HISPI	SLVS	enable	0x00	1.8	1.2	1.8	2.8	2.8	1.2	1.2	1.2
3	HISPI	SLVS	disable	0x01	2.8	0.4	1.8	2.8	2.8	1.2	1.2	1.2
4	HISPI	SLVS	disable	0x01	1.8	0.4	1.8	2.8	2.8	1.2	1.2	1.2
5	HISPI	sub-LVDS	disable always	0x10	1.8	1.2	1.8	2.8	2.8	1.2	1.2	1.2
6	MIPI		disable always	0x01	2.8	1.2	1.8	2.8	2.8	1.2	1.2	1.2
7	MIPI		disable always	0x01	1.8	1.2	1.8	2.8	2.8	1.2	1.2	1.2

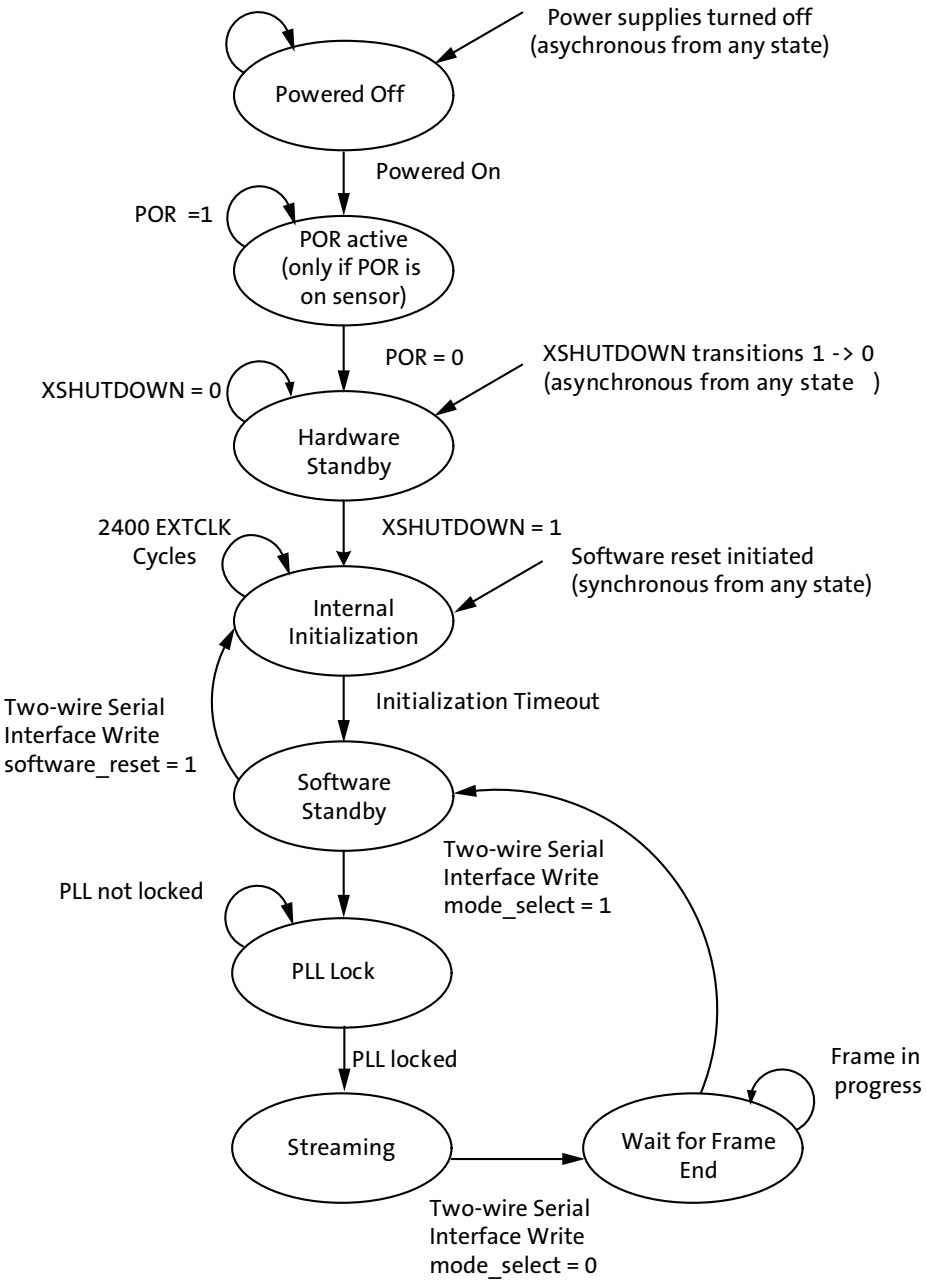
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

System States

The system states of the AR1820HS are represented as a state diagram in Figure 5 and described in subsequent sections. The effect of XSHUTDOWN on the system state and the configuration of the PLL in the different states are shown in Table 8 on page 21.

The sensor's operation is broken down into three separate states: hardware standby, software standby, and streaming. The transition between these states might take a certain amount of clock cycles as outlined in Table 8.

Figure 5: AR1820HS System States



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 4: XSHUTDOWN and PLL in System States

State	EXTCLKs	PLL
Powered off	x	VCO powered down
POR active	x	
Hardware standby	0	
Internal initialization	1	
Software standby		
PLL Lock		VCO powering up and locking, PLL output bypassed
Streaming		VCO running, PLL output active
Wait for frame end		

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Sensor Initialization

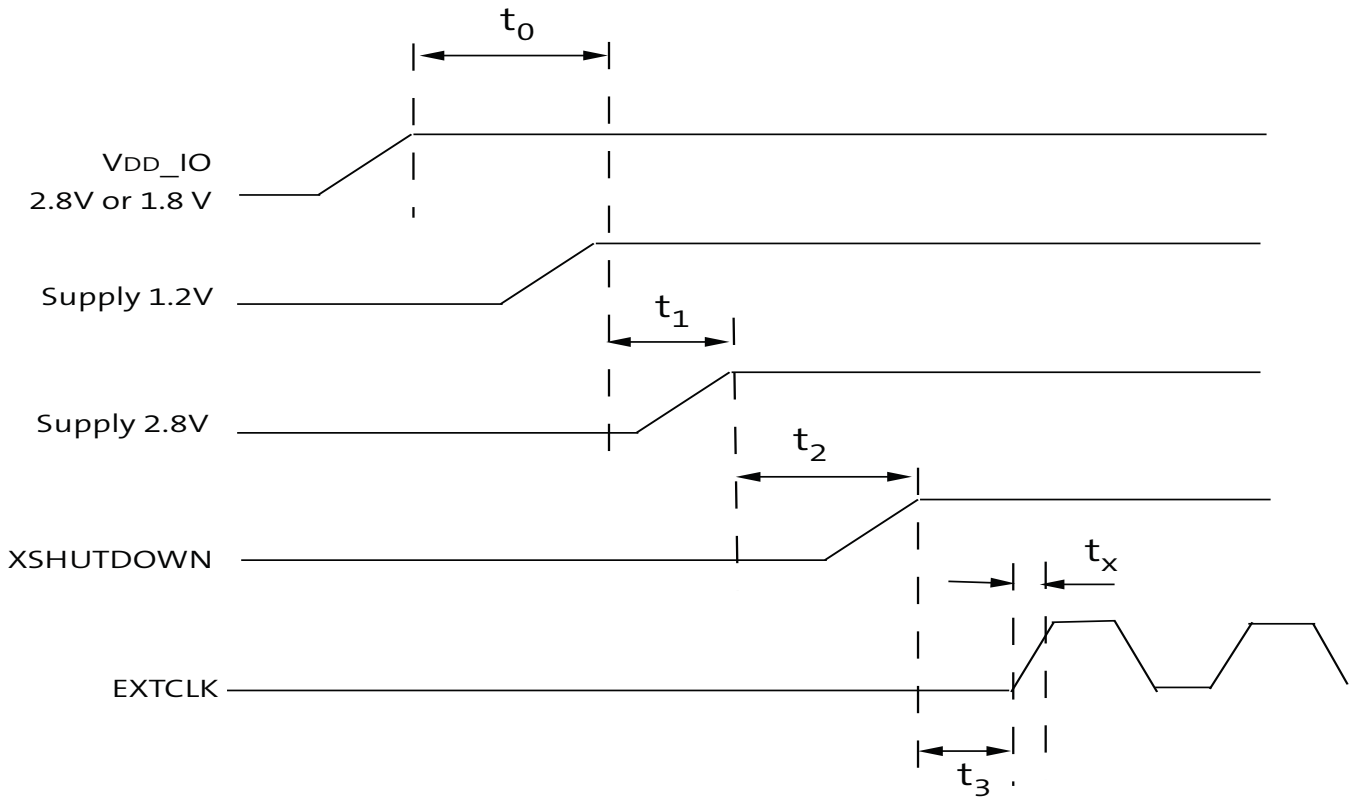
Power On Sequence

AR1820HS has three voltage supplies divided into several domains. The three voltages are 1.2V, 1.8V, and 2.8V. For proper operation of the chip, a power-up sequence is recommended as shown in Figure 6.

Since VDD_IO supply controls the XSHUTDOWN, it should be turned on first. The sequence of powering up the other two domains is not very critical. But it is still recommended to follow the below sequence for best performance:

1. Power up the VDD_IO supply (VDD_IO is either 2.8V or 1.8V) and VDD_1V8.
2. After 200µs activate the 1.2V power supply domains including VDD, VDD_HISPI, VDD_PLL, VDD_TX(0.4 or 1.2V)
3. After another 200µs activate the 1.8V and 2.8V supply domains including VAA, VAA_PIX.
4. After the last power supply is stable set XSHUTDOWN to the HIGH value of the VDD_IO supply.
5. After XSHUTDOWN is stable wait 200µs and then enable EXTCLK.
6. After XSHUTDOWN being pulled up, wait 2750 µs and then start I^2C.

Figure 6: Recommended Power-up Sequence



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 5: Power-up Sequence

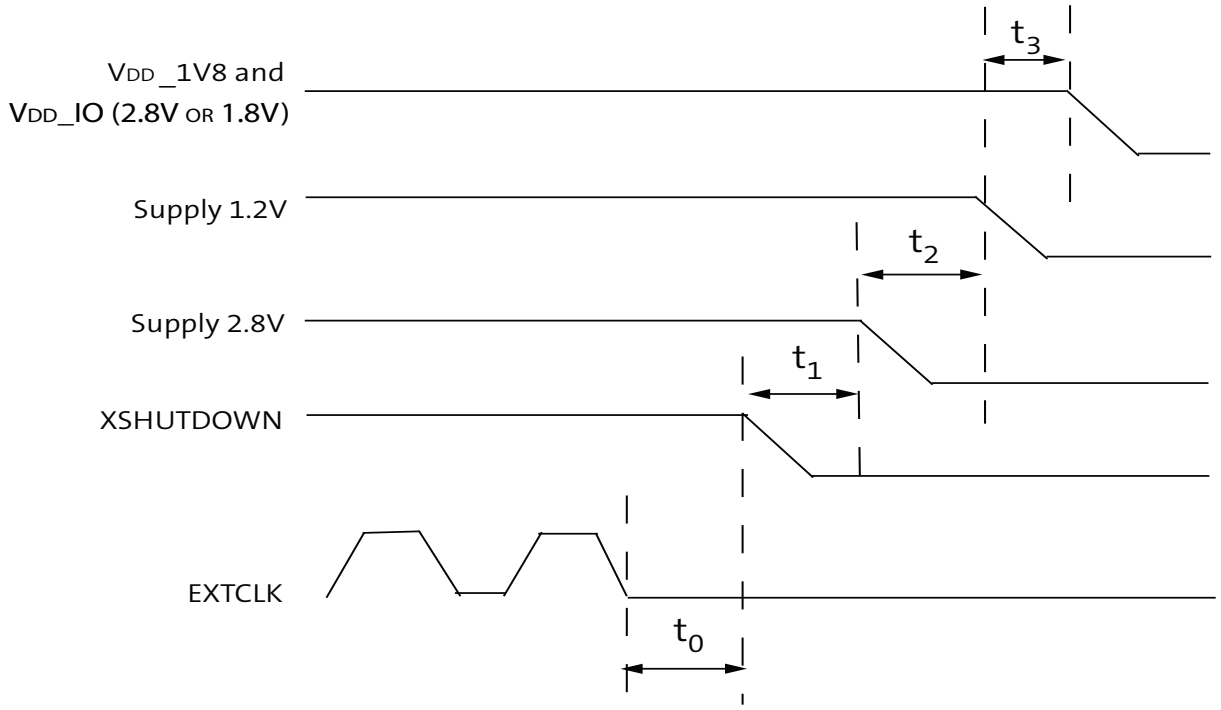
Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_IO and VDD_1V8to supply 1.2V	t_0	0.2	–	500	ms
Supply 1.2V to supply 2.8V/1.8V	t_1	0	200	500	ms
Supply 2.8V/1.8V to XSHUTDOWN	t_2	0.2	–	500	ms
XSHUTDOWN to EXTCLK	t_3	100	–	–	µs
External clock rise/fall time	t_x	–	30	–	ns

Power Down Sequence

The recommended power-down sequence for the AR1820HS is shown in Figure 7. The three power supply domains (1.2V, 1.8V, and 2.8V) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0.
2. After disabling the internal clock EXTCLK, disable XSHUTDOWN.
3. After XSHUTDOWN is LOW disable the 2.8V/1.8V supply (including VAA, VAA_PIX).
4. After the 2.8V/1.8V supply is LOW disable the 1.2V supply(including VDD, VDD_HISPI, VDD_PLL, VDD_TX (0.4 or VDD_1V8 and 1.2V)).
5. After the 1.2V supply is LOW disable the VDD_IO supply (VDD_IO is either 2.8V or 1.8V).

Figure 7: Recommended Power-Down Sequence



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 6: Power-Down Sequence

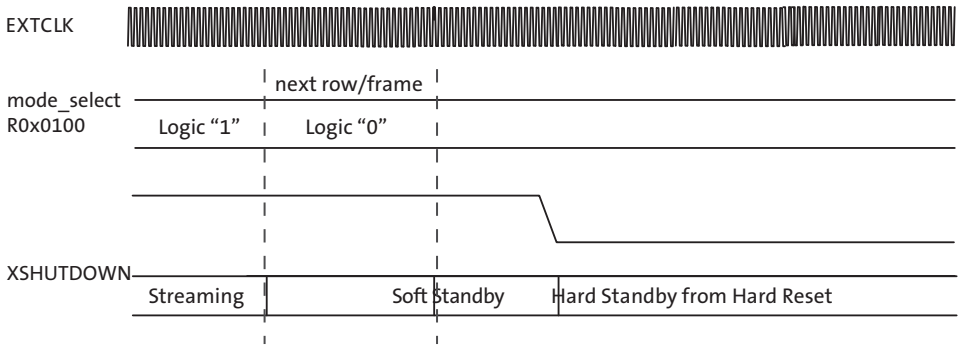
Definition	Symbol	Minimum	Typical	Maximum	Unit
EXTCLK to XSHUTDOWN	t_0	100	–	–	µs
XSHUTDOWN to supply 2.8V/1.8V	t_1	200	–	–	µs
Supply 2.8V/1.8V to supply 1.2V	t_2	0	200	–	µs
Supply 1.2V to VDDD_IO	t_3	200	–	–	µs

Hard Standby and Hard Reset

The hard standby state is reached by the assertion of the XSHUTDOWN pad (hard reset). Register values are not retained by this action, and will be returned to their default values once hard reset is completed. The minimum power consumption is achieved by the hard standby state. The details of the sequence are described below and shown in Figure 8.

1. Disable streaming if output is active by setting mode_select 0x301A[2] = 0.
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Assert XSHUTDOWN (active LOW) to reset the sensor.
4. The sensor remains in hard standby state if XSHUTDOWN remains in the logic “0” state.

Figure 8: Hard Standby and Hard Reset



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Soft Standby and Soft Reset

The AR1820HS can reduce power consumption by switching to the soft standby state when the output is not needed. Register values are retained in the soft standby state. The details of the sequence are described below and shown in Figure 9.

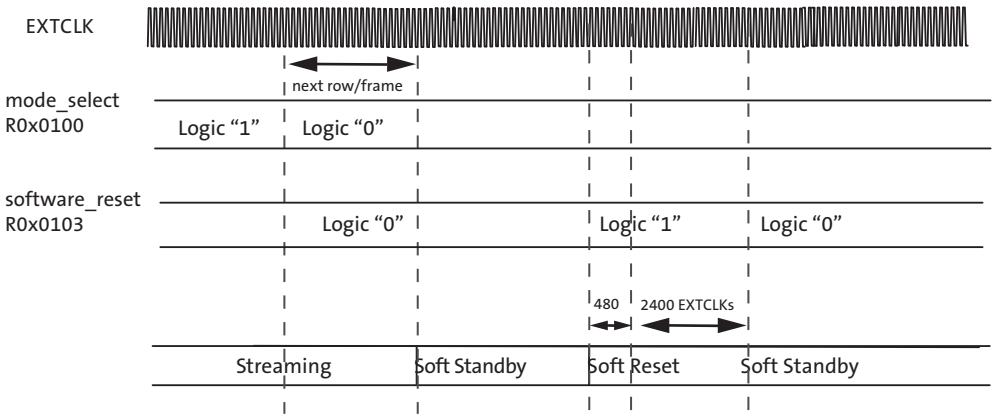
Soft Standby

1. Disable streaming if output is active by setting mode_select 0x301A[2] = 0.
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.

Soft Reset

1. Follow the soft standby sequence list above.
2. Set software_reset = 1 (R0x3021) to start the internal initialization sequence.
3. After 2400 EXTCLKs, the internal initialization sequence is completed and the current state returns to soft standby automatically.

Figure 9: Soft Standby and Soft Reset



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Two-Wire Serial Register Interface

A two-wire serial interface bus enables read/write access to control and status registers within the AR1820HS. The two-wire serial interface is fully compatible with the I^2C standard.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR1820HS uses SCLK as an input only and therefore never drives it LOW. The electrical and timing specifications are further detailed on "Two-Wire Serial Register Interface" on page 85.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. For example, the default slave addresses used by the AR1820HS for the HiSPi configured sensor are 0x6C (write address) and 0x6D (read address) in accordance with the HiSPi specification. Secondary slave addresses of 0x6E (write address) and 0x6F (read address) can be selected by enabling and asserting the SADDR signal through the GPI pad.

An alternate slave address can also be programmed through R0x31FC

.

Table 7: Primary and Secondary Slave Addresses

Part Number and Description	Default Primary Slave Address		Default Seconary Slave Address	
	Write Address	Read Address	Write Address	Read Address
AR1820HSSC00SHEA0 0° CRA, HiSPi, plastic iBGA	0x6C	0x6D	0x6E	0x6F
AR1820HSSC12SHEA0 11.4° CRA, HiSPi, plastic iBGA	0x6C	0x6D	0x6E	0x6F
AR1820HSSC31SMD20 31° CRA, MIPI, RECON	0x6E	0x6F	0x6C	0x6D

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and

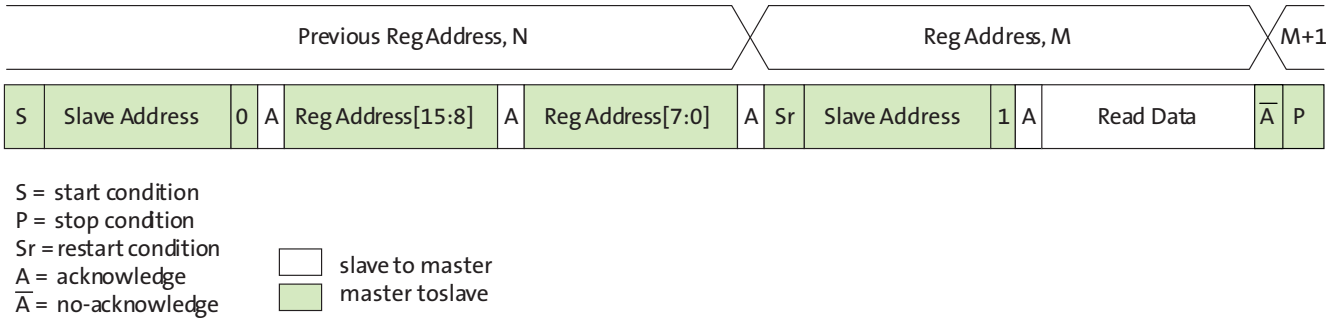
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 10 on page 28) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 10 shows how the internal register address maintained by the AR1820HS is loaded and incremented as the sequence proceeds.

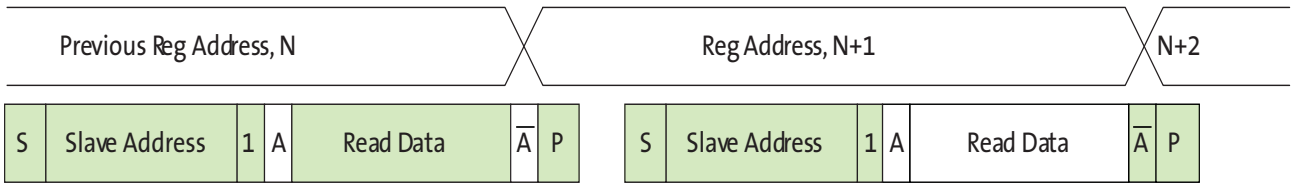
Figure 10: Single READ from Random Location



Single READ from Current Location

This sequence (Figure 11) performs a read using the current value of the AR1820HS internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

Figure 11: Single READ from Current Location

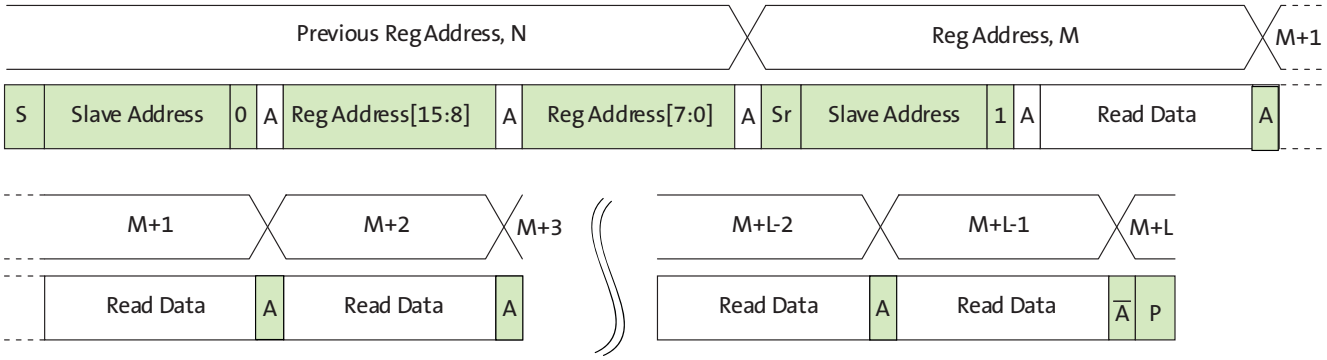


Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Sequential READ, Start from Random Location

This sequence (Figure 12) starts in the same way as the single READ from random location (Figure 10). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

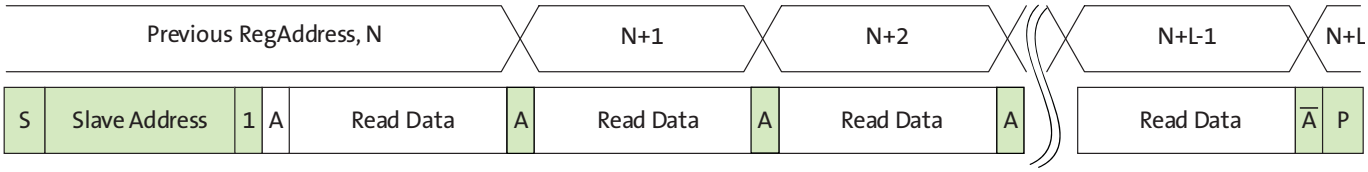
Figure 12: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 13) starts in the same way as the single READ from current location (Figure 11 on page 28). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

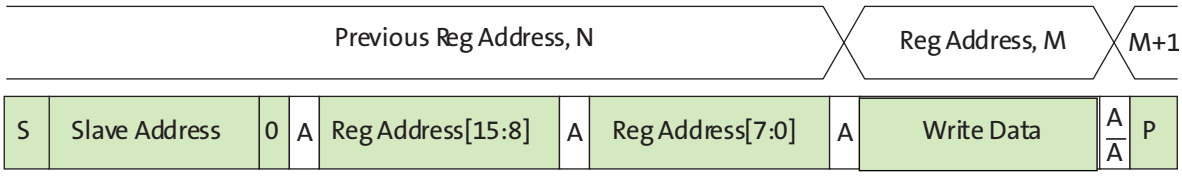
Figure 13: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 14) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

Figure 14: Single WRITE to Random Location

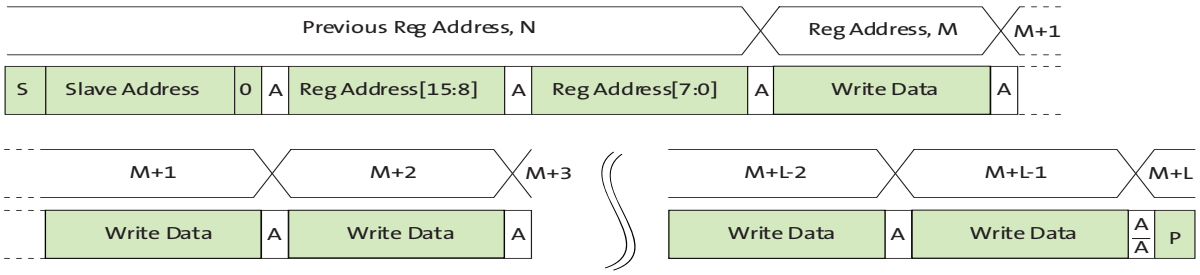


Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Sequential WRITE, Start at Random Location

This sequence (Figure 15) starts in the same way as the single WRITE to random location (Figure 14). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 15: Sequential WRITE, Start at Random Location



Three-Wire Serial Interface

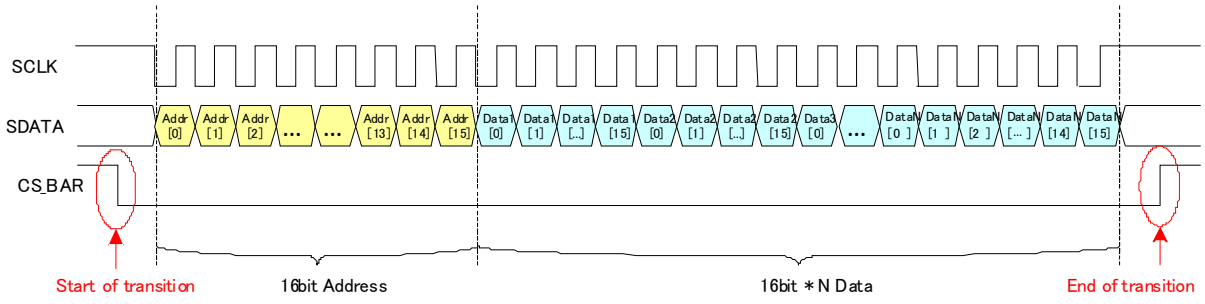
The three-Wire interface is designed to allow higher speed host register writes. The maximum operation frequency for the three-wire interface is 10 MHz.

CS_BAR is used to enable the three-wire interface when CS_BAR = 0.

CSI_EN should be "1" in order to enable full speed for the three-wire interface.

The three-wire interface supports register writes only, no register read; register read is supported by I^2C.

Figure 16: Timing Diagram for Three-Wire Serial Interface



The CS_BAR signal is the indicator for three-wire interface is using, so, during CS_BAR = 0, SDATA and SCLK input for I^2C logic is disabled.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Registers

The AR1820HS provides a 16-bit register address space accessed through a serial interface (“Two-Wire Serial Register Interface” on page 26). Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 12. The remainder of this section describes these registers in detail.

Table 8: Address Space Regions

Address Range	Description
0x0000–0x0FFF	Configuration registers (read-only and read-write dynamic registers)
0x1000–0x1FFF	Parameter limit registers (read-only static registers)
0x2000–0x2FFF	Image statistics registers (none currently defined)
0x3000–0x3FFF	Manufacturer-specific registers (read-only and read-write dynamic registers)

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR1820HS uses 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is a 2-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Register Aliases

A consequence of the internal architecture of the AR1820HS is that some registers are decoded at multiple addresses. Some registers in “configuration space” are also decoded in “manufacturer-specific space.” To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0202 is coarse_integration_time and R0x3012 is coarse_integration_time_. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the chip_version_reg register are referred to as chip_version_reg[3:0] or R0x0000–1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x0100 (mode_select) has only one operational bit, R0x0100[0]. This bit is aliased to R0x301A–B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Byte Ordering

Registers that occupy more than one byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the data bus. For example, the chip_version_reg register is R0x0000–1. In the register table the default value is shown as 0x4B00. This means that a read from address 0x0000 would return 0x4B, and a read from address 0x0001 would return 0x00. When reading this register as two 8-bit transfers on the serial interface, the 0x4B will appear on the serial interface first, followed by the 0x00.

Address Alignment

All register addresses are aligned naturally. Registers that occupy 2 bytes of address space are aligned to even 16-bit addresses, and registers that occupy 4 bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 13.

Table 9: Data Formats

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = –128, 0xFFFF = –0.0039065
UFIX16	Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Register Behavior

Registers vary from “read-only,” “read/write,” and “read, write-1-to-clear.”

Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing R0x3004–5 (x_addr_start) partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the AR1820HS double-buffers many registers by implementing a “pending” and a “live” version. Reads and writes access the pending register. The live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the “Frame Sync’d” column shows which registers or register fields are double-buffered in this way.

Using grouped_parameter_hold

Register grouped_parameter_hold (R0x301A[15]) can be used to inhibit transfers from the pending to the live registers. When the AR1820HS is in streaming mode, this register should be written to “1” before making changes to any group of registers where a set of changes is required to take effect simultaneously. When this register is written to “0,” all transfers from pending to live registers take place on the next frame start.

An example of the consequences of failing to set this bit follows:

An external auto exposure algorithm might want to change both gain and integration time between two frames. If the next frame starts between these operations, it will have the new gain, but not the new integration time, which would return a frame with the wrong brightness that might lead to a feedback loop with the AE algorithm resulting in flickering.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x300C) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.
Y—Yes. Changing the register value might produce a bad frame.
YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to “1.”

Changes to Integration Time

If the integration time is changed while FV is asserted for frame *n*, the first frame output using the new integration time is frame *(n + 2)*. The sequence is as follows:

1. During frame *n*, the new integration time is held in the pending register.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

2. At the start of frame (*n* + *1*), the new integration time is transferred to the live register. Integration for each row of frame (*n* + *1*) has been completed using the old integration time.
3. The earliest time that a row can start integrating using the new integration time is immediately after that row has been read for frame (*n* + *1*). The actual time that rows start integrating using the new integration time is dependent upon the new value of the integration time.
4. When frame (*n* + *2*) is read out, it will have been integrated using the new integration time.

If the integration time is changed on successive frames, each value written will be applied for a single frame; the latency between writing a value and it affecting the frame readout remains at two frames.

Changes to Gain Settings

Usually, when the gain settings are changed, the gain is updated on the next frame start. When the integration time and the gain are changed at the same time, the gain update is held off by one frame so that the first frame output with the new integration time also has the new gain applied. In this case, a new gain should not be set during the extra frame delay. There is an option to turn off the extra frame delay by setting extra_delay (R0x3018).

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Clocking

Default setup gives a physical 76.8 MHz internal clock for an external input clock of 25 MHz.

The sensor contains a phase-locked loop (PLL) for timing generation and control. The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and a set of dividers to generate the output clocks. The PLL structure is shown in Figure 17.

Figure 1: Clocking Configuration

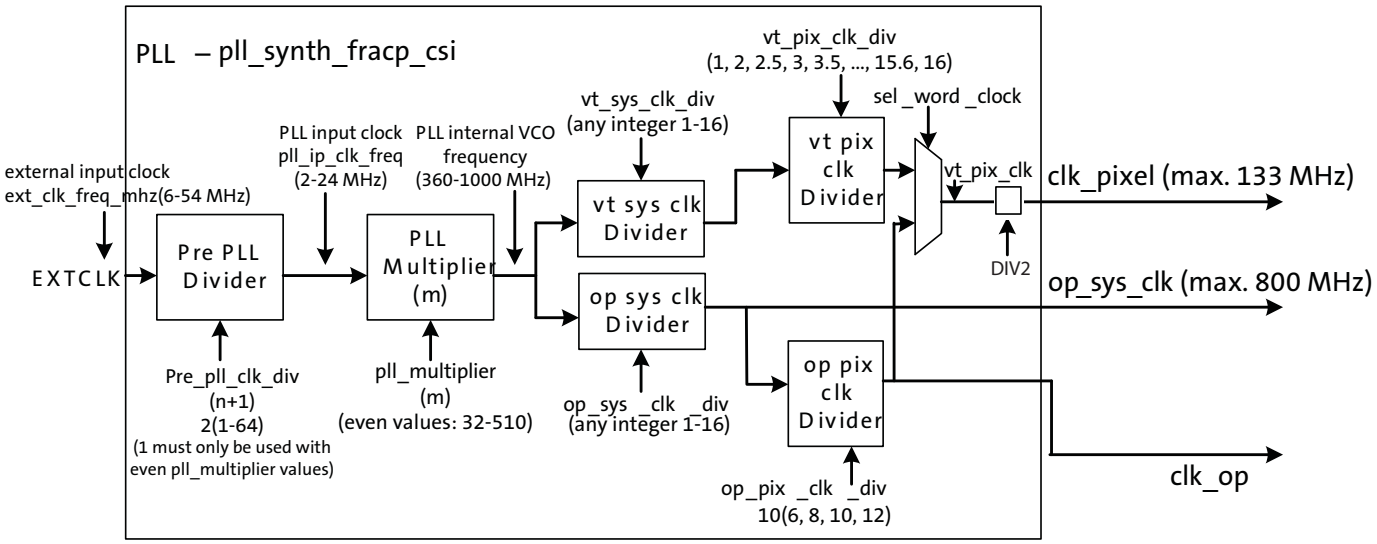


Figure 17 shows the different clocks and the names of the registers that contain or are used to control their values. The figure shows the default setting for each divider/multiplier control register and the range of legal values for each divider/multiplier control register. The vt_pix_clk is divided by two to compensate for the fact that the design has 2 digital data paths. This divider should always remain turned on.

The usage of the output clocks is shown below:

- clk_pixel (vt_pix_clk / row_speed[2:0]) is used by the sensor core to read out and control the timing of the pixel array. The sensor core produces one 10-bit pixel each vt_pix_clk period. The line length (line_length_pck) is controlled in increments of the clk_pixel period (clk_pixel max at 133 MHz).
- clk_op (op_pix_clk / row_speed[10:8]) is used to load parallel pixel data from the output FIFO to the serializer. The output FIFO generates one pixel each op_pix_clk period.
- op_sys_clk is used to generate the serial data stream on the output. The relationship between this clock frequency and the op_pix_clk frequency is dependent upon the output data format.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

The output clock frequencies can be calculated as:

$$clk\_pix\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times vt\_sys\_clk\_div \times vt\_pix\_clk\_div \times row\_speed[2:0] \times 2^{DIV2}} \quad \text{(EQ 1)}$$

$$clk\_op\_freq\_mhz = \frac{ext\_clk\_freq\_mhz * pll\_multiplier}{pre\_pll\_clk\_div*op\_sys\_clk\_div*op\_pix\_clk\_div} \quad \text{(EQ 2)}$$

$$op\_sys\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz * pll\_multiplier}{pre\_pll\_clk\_div * op\_sys\_clk\_div} \quad \text{(EQ 3)}$$

PLL Clocking

The PLL divisors should be programmed while the AR1820HS is in the software standby state. After programming the divisors, it is necessary to wait for the VCO lock time before enabling the PLL. The PLL is enabled by entering the streaming state.

An external timer will need to delay the entrance of the streaming mode by 1 millisecond so that the PLL can lock.

The effect of programming the PLL divisors while the AR1820HS is in the streaming state is undefined.

Clock Control

The AR1820HS uses an aggressive clock-gating methodology to reduce power consumption. The clocked logic is divided into a number of separate domains, each of which is only clocked when required.

When the AR1820HSenters a soft standby state, almost all of the internal clocks are stopped. The only exception is that a small amount of logic is clocked so that the two-wire serial interface continues to respond to read and write requests.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Features

Shading Correction (SC)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The AR1820HS has an embedded shading correction module that can be programmed to counter the shading effects on each individual Red, GreenB, GreenR, and Blue color signal.

The Correction Function

Color-dependent solutions are calibrated using the sensor/lens system and an image of an evenly illuminated, featureless gray calibration field. From the resulting image, register values for the color correction function (coefficients) can be derived.

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$Pcorrected(row, col) = Psensor(row,col) * f(row,col) \quad \text{(EQ 4)}$$

where *P* are the pixel values and *f* is the color dependent correction functions for each color channel.

Each function includes a set of color-dependent coefficients defined by registers R0x3600–3726. The function's origin is the center point of the function used in the calculation of the coefficients. Using an origin near the central point of symmetry of the sensor response provides the best results. The center point of the function is determined by poly_origin_c (R0x3782) and poly_origin_r (R0x3784) and can be used to counter an offset in the system lens from the center of the sensor array.

One-Time Programmable Memory (OTPM)

The AR1820HS features 6.4Kbits of one-time programmable memory (OTPM) for storing shading correction coefficients, individual module, and sensor specific information. OTPM can be accessed through two-wire serial interface. The AR1820HS uses the auto mode for fast OTPM programming and read operations.

To read out the OTPM, 1.8V supply is required. As a result, a dedicated DVDD_1V8 pad has been implemented.During the programming process, a dedicated pin for high voltage needs to be provided to perform the anti-fusing operation. This voltage (VPP) would need to be 6.5V. The completion of the programming process will be communicated by a register through the two-wire serial interface.

If the VPP pin does not need to be bonded out as a pin on the module, it should be left floating inside the module.

The programming of the OTPM requires the sensor to be fully powered and remain in software standby with its clock input applied. The information will be programmed through the use of the two-wire serial interface, and once the data is written to an internal register, the programming host machine will apply a high voltage to the programming pin, and send a program command to initiate the anti-fusing process. After the sensor has finished programming the OTPM, a status bit will be set to indicate

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

the end of the programming cycle, and the host machine can poll the setting of the status bit through the two-wire serial interface. Only one programming cycle for the 16-bit word can be performed.

Reading the OTPM data requires the sensor to be fully powered and operational with its clock input applied. The data can be read through a register from the two-wire serial interface.

Programming and Verifying the OTPM

The procedure for programming and verifying the AR1820HS OTPM follows:

1. Apply power to all the power rails of the sensor (VDD_IO, VAA, VAA_PIX, DVDD_1V2, DVDD_1V2_PHY, and DVDD_1V8). VAA must be set to 2.8V during the programming process. VPP must be initially floating. All other supplies must be at their nominal voltage.
2. Provide a 12-MHz EXTCLK clock input.
3. Set R0x301A = 0x18, to put sensor in the soft standby mode.
4. Set R0x3130 = 0xFF01 (Timing configuration)
5. Set R0x304C[15:8] = Record type (E.g. 0x30)
6. Set R0x304C[7:0] = Length of the record which is the number of OTPM data registers that are filled in.
7. Set R0x3054[9] = 0 to ensure that the error checking and correction is enabled.
8. Write data into all the OTPM data registers: R0x3800-R0x39FE.
9. Ramp up VPP to 6.5V.
10. Set the otpm_control_auto_wr_start bit in the otpm_control register R0x304A[0] = 1, to initiate the auto program sequence. The sensor will now program the data into the OTPM.
11. Poll OTPM_Control_Auto_WR_end (R0x304A [1]) to determine when the sensor is finished programming the word.
12. Verify that the otpm_control_auto_wr_success(0x304A[2]) bit is set.
13. If the above bits are not set to 1, then examine otpm_status register R0x304E[9] to verify if the OTPM memory is full and 0x304E[10] to verify if OTPM memory is insufficient.
14. Remove the high voltage (Vpp) and float Vpp pin.

Reading the OTPM

1. Apply power to all the power rails of the sensor (VDD_IO, VAA, VAA_PIX, DVDD_1V2, DVDD_1V2_PHY, and DVDD_1V8) at their nominal voltage.
2. Set EXTCLK to normal operating frequency.
3. Perform proper reset sequence to the sensor.
4. Set R0x3134=0xCD95 (Timing Configuration)
5. Set R0x304C[15:8] = Record Type (for-example, 0x30)
6. Set R0x304C[7:0] = Length of the record which is the number of data registers to be read back. This could be set to 0 during OTPM auto read if length is unknown.
7. Set R0x3054 = 0x0400
8. Initiate the auto read sequence by setting the otpm_control_auto_read_start bit (R0x304A[4]) = 1.
9. Poll the otpm_control_auto_rd_end bit (R0x304A[5]) to determine when the sensor is finished reading the word(s). When this bit becomes 1, the otpm_control_suto_rd_-success bit (R0x304A[6]) will indicate whether the memory was read successfully or not.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

10. Data can now be read back from the otpm_data registers (R0x3800-R0x39FE).

Image Acquisition Modes

The AR1820HS supports two image acquisition modes:

1. Electronic rolling shutter (ERS) mode.
   This is the normal mode of operation. When the AR1820HS is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When the ERS is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is fixed, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR1820HS switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” on page 33.
2. Global reset mode.
   This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR1820HS provides control signals to interface to that shutter. The operation of this mode is described in detail in “Global Reset Release (GRR)” on page 58.

The benefit for the use of an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

Window Control

The sequencing of the pixel array is controlled by the x_addr_start, y_addr_start, x_addr_end, and y_addr_end registers. For both parallel and serial interfaces, the output image size is controlled by the x_output_size and y_output_size registers.

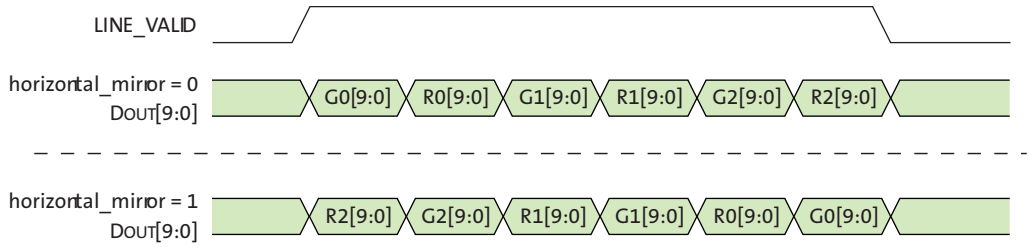
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Readout Modes

Horizontal Mirror

The horizontal_mirror bit in the image_orientation register is set by default. The result of this is that the order of pixel readout within a row is reversed, so that readout starts from x_addr_end and ends at x_addr_start. Figure 18 on page 40 shows a sequence of 6 pixels being read out with horizontal_mirror = 0 and horizontal_mirror = 1. Changing horizontal_mirror causes the Bayer order of the output image to change; the new Bayer order is reflected in the value of the pixel_order register.

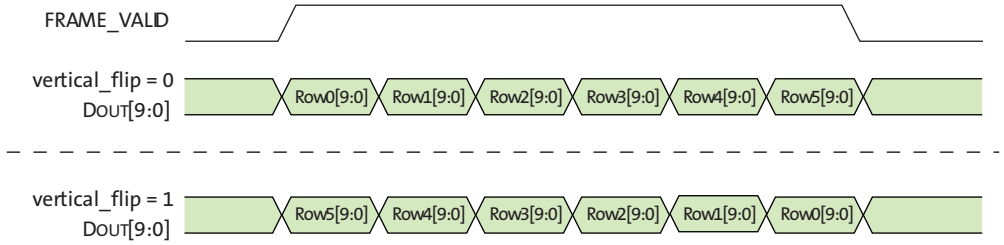
Figure 2: Effect of horizontal_mirror on Readout Order



Vertical Flip

When the vertical_flip bit is set in the image_orientation register, the order in which pixel rows are read out is reversed, so that row readout starts from y_addr_end and ends at y_addr_start. Figure 19 shows a sequence of 6 rows being read out with vertical_flip = 0 and vertical_flip = 1. Changing vertical_flip causes the Bayer order of the output image to change; the new Bayer order is reflected in the value of the pixel_order register.

Figure 3: Effect of vertical_flip on Readout Order

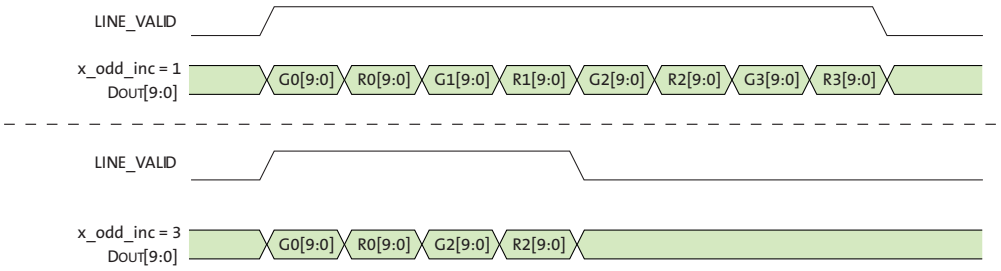


Subsampling

The AR1820HS supports subsampling. Subsampling reduces the amount of data processed by the analog signal chain in the AR1820HS thereby allowing the frame rate to be increased. Subsampling is enabled by setting x_odd_inc and/or y_odd_inc. Values of 1, 3, and 7 can be supported. Setting both of these variables to 3 reduces the amount of row and column data processed and is equivalent to the 2 x 2 skipping readout mode provided by the AR1820HS. Setting x_odd_inc = 3 and y_odd_inc = 3 results in a quarter reduction in output image size. Figure 20 on page 41 shows a sequence of 8 columns being read out with x_odd_inc = 3 and y_odd_inc = 1.

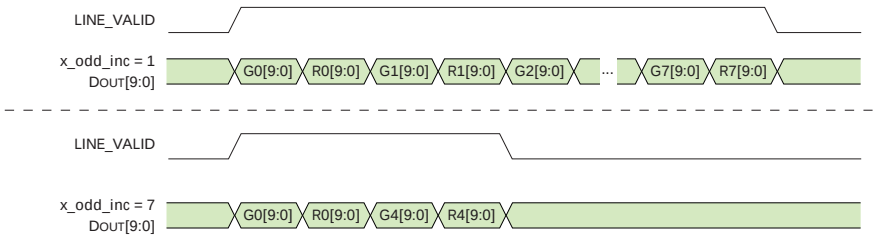
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 4: Effect of x_odd_inc = 3 on Readout Sequence



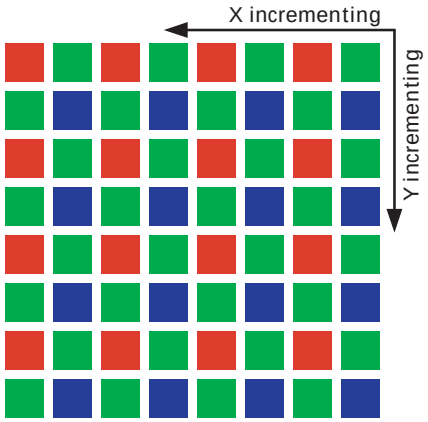
A 1/16 reduction in resolution is achieved by setting both x_odd_inc and y_odd_inc to 7. This is equivalent to 4 x 4 skipping readout mode provided by the AR1820HS. Figure 21 shows a sequence of 16 columns being read out with x_odd_inc = 7 and y_odd_inc = 1.

Figure 5: Effect of x_odd_inc = 7 on Readout Sequence



The effect of the different subsampling settings on the pixel array readout is shown in Figure 22 through Figure 24 on page 42.

Figure 6: Pixel Readout (No Subsampling)



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 7: XSkip2/YSkip2 Pixel Readout (x_odd_inc = 3, y_odd_inc = 3)

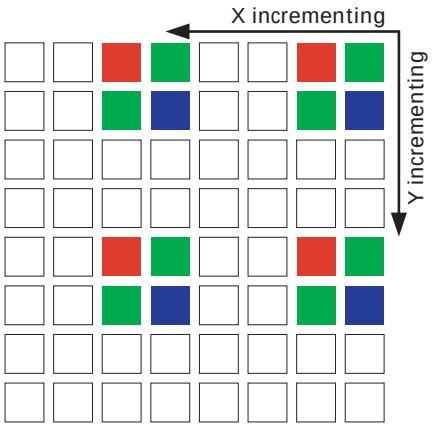
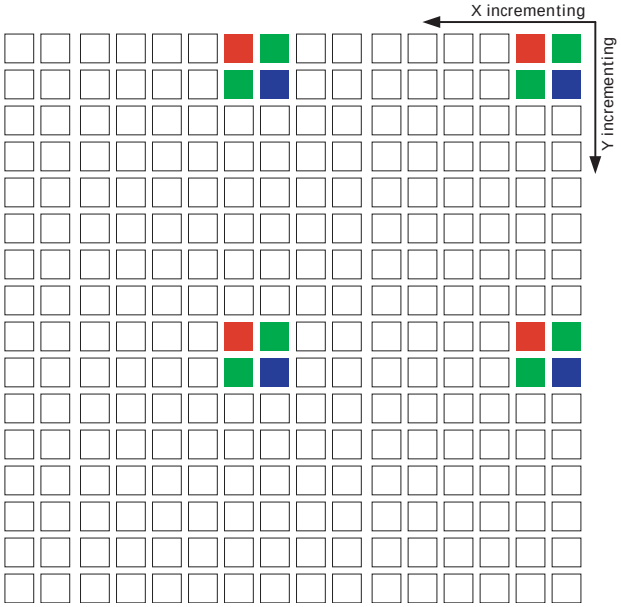


Figure 8: XSkip4/YSkip4 Pixel Readout (x_odd_inc = 7, y_odd_inc = 7)



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Programming Restrictions when Subsampling

When subsampling is enabled as a viewfinder mode and the sensor is switched back and forth between full resolution and subsampling, Aptina recommends that line_length_pck be kept constant between the two modes. This allows the same integration times to be used in each mode.

When subsampling is enabled, it may be necessary to adjust the x_addr_start, x_addr_end, y_addr_start, and y_addr_end settings: the values for these registers are required to correspond with rows/columns that form part of the subsampling sequence. The adjustment should be made in accordance with these rules:

x_skip_factor = (x_odd_inc + 1) / 2
y_skip_factor = (y_odd_inc + 1) / 2

- x_addr_start should be a multiple of x_skip_factor * 4
- (x_addr_end - x_addr_start + x_odd_inc) should be a multiple of x_skip_factor * 4
- (y_addr_end - y_addr_start + y_odd_inc) should be a multiple of y_skip_factor * 4

The number of columns/rows read out with subsampling can be found from the equation below:

- columns/rows = (addr_end - addr_start + odd_inc) / skip_factor

Table 14 shows the row or column address sequencing for normal and subsampled readout. In the 2X skip case, there are two possible subsampling sequences (because the subsampling sequence only reads half of the pixels) depending upon the alignment of the start address. Similarly, there will be four possible subsampling sequences in the 4X skip case (though only the first two are shown in Table 14).

Table 1: Row Address Sequencing During Subsampling

odd_inc = 1 (Normal)	odd_inc = 3 (2X Skip)	odd_inc = 7 (4X Skip)
start = 0	start = 0	start = 0
0	0	0
1	1	1
2		
3		
4	4	
5	5	
6		
7		
8	8	8
9	9	9
10		
11		
12	12	
13	13	
14		
15		

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

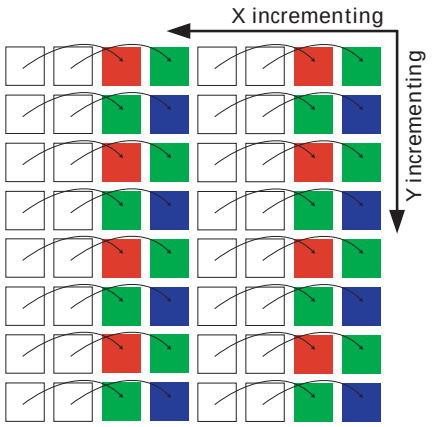
Binning

The AR1820HS supports 2 x 1 (column binning, also called x-binning). Binning has many of the same characteristics as skipping, but because it gathers image data from all pixels in the active window (rather than a subset of them), it achieves superior image quality and avoids the aliasing artifacts that can be a characteristic side effect of skipping.

Binning is enabled by selecting the appropriate subsampling settings (in read_mode, the sub-register x_odd_inc = 3 and y_odd_inc = 1 for x-binning and setting the appropriate binning bit in read_mode R0x3040[11] = 1 for x_bin_enable). As with skipping, x_addr_end and y_addr_end may require adjustment when binning is enabled. It is the first of the two columns/rows binned together that should be the end column/row in binning, so the requirements to the end address are exactly the same as in skipping mode. The effect of the different binning is shown in Figure 25 below and Figure 26 on page 45.

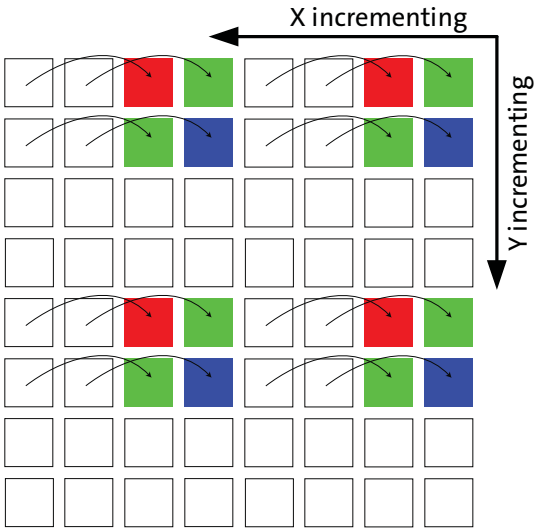
Binning can also be enabled when the 4X subsampling mode is enabled (x_odd_inc = 7 and y_odd_inc = 1 for x-binning, x_odd_inc = 7 and y_odd_inc = 7 for 4X xy-binning). In this mode, however, not all pixels will be used so this is not a 4X binning implementation. An implementation providing a combination of skip2 and bin2 is used to achieve 4X subsampling with better image quality. The effect of this subsampling mode is shown in Figure 26 on page 45.

Figure 9: X:Bin2 Pixel Readout (x_odd_inc = 3, y_odd_inc = 1, x_bin = 1)



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 10: Xbin2,Yskip2 Pixel Readout (x_odd_inc = 3, y_odd_inc = 3, x_bin = 1)



Binning address sequencing is a bit more complicated than during subsampling only, because of the implementation of the binning itself.

For a given column *n*, there is only one other column, n_bin, that can be binned with, because of physical limitations in the column readout circuitry. The possible address sequences are shown in Table 15.

Table 2: Column Address Sequencing During Binning

odd_inc = 1 (Normal)	odd_inc = 3 (2X Bin)	odd_inc = 7 (2X Skip + 2XBin)
x_addr_start = 0	x_addr_start = 0	x_addr_start = 0
0	0/2	0/4
1	1/3	1/5
2		
3		
4	4/6	
5	5/7	
6		
7		
8	8/10	8/12
9	9/11	9/13
10		
11		
12	12/14	
13	13/15	
14		
15		

There are no physical limitations on what can be binned together in the row direction. A given row *n* will always be binned with row n+2 in 2X subsampling mode and with row n+4 in 4X subsampling mode. Therefore, which rows get binned together depends upon the alignment of y_addr_start. The possible sequences are shown in Table 16 on page 46.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 3: Row Address Sequencing During Binning

odd_inc = 1 (Normal)	odd_inc = 3 (2X Bin)	odd_inc = 7 (2X Skip + 2X Bin)
x_addr_start = 0	x_addr_start = 0	x_addr_start = 0
0	0/2	0/4
1	1/3	1/5
2		
3		
4	4/6	
5	5/7	
6		
7		
8	8/10	8/12
9	9/11	9/13
10		
11		
12	12/14	
13	13/15	
14		
15		

Programming Restrictions When Binning and Summing

Binning and summing require different sequencing of the pixel array and impose different timing limits on the operation of the sensor.

As a result, when xy-subsampling is enabled, some of the programming limits declared in the parameter limit registers are no longer valid. In addition, the default values for some of the manufacturer-specific registers need to be reprogrammed. See “Minimum Number of Rows” and "Minimum Row Time" on page 50.

Subsampling / binning options:

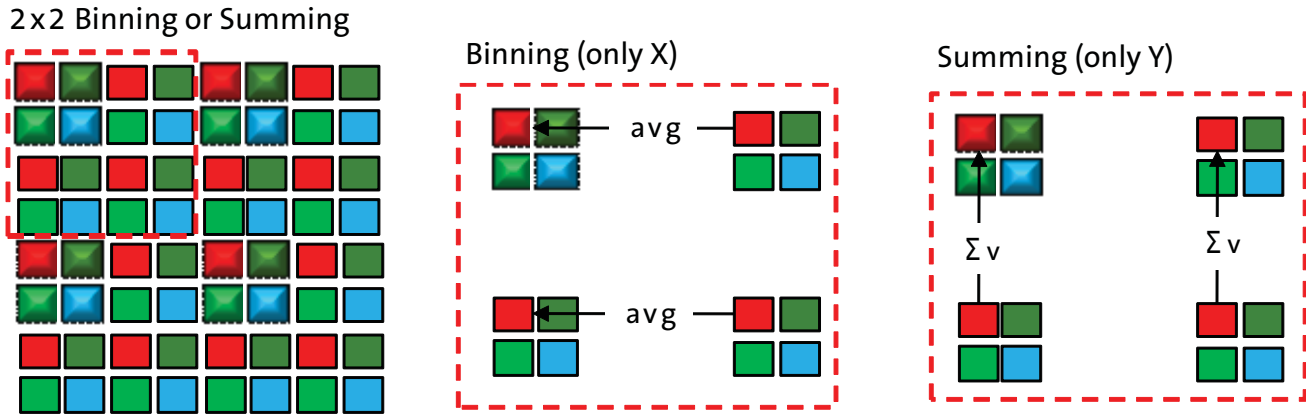
1. XskipYskip
   1a. R0x3040[11], x_bin_en: 0
   1b. R0x3040[13], row_sum: 0
2. XbinYskip
   2a. R0x3040[11], x_bin_en: 1
   2b. R0x3040[13], row_sum: 0
3. XskipYsum
   3a. R0x3040[11], x_bin_en: 0
   3b. R0x3040[13], row_sum: 1
4. XbinYsum
   4a. R0x3040[11], x_bin_en: 1
   4b. R0x3040[13], row_sum: 1

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Binning (only X) and Summing (only Y) Mode

Summing can be enabled with binning. The register x_odd_inc must be set to 3 to enable summing. Unlike binning mode where the values of adjacent same color pixels are averaged together, summing adds the pixel values together resulting in better sensor sensitivity. Summing is supposed to provide two times the sensitivity compared to the binning only mode.

Figure 11: Pixel XBinning and YSumming



Scaler

The AR1820HS sensor is capable of horizontal scaling.

The scaling factor, programmable in 1/16 steps, is used for horizontal scalers.

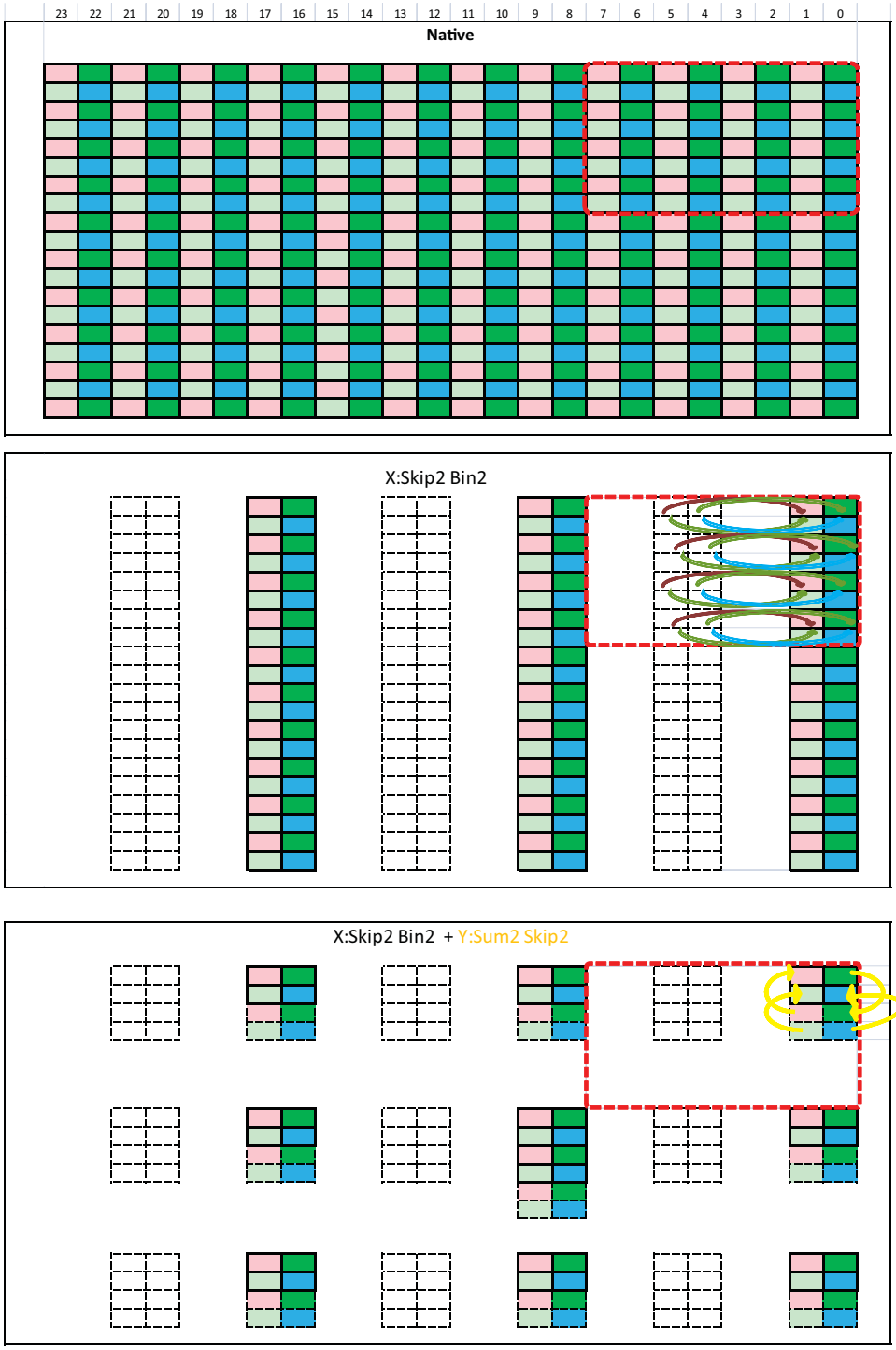
The scale factor is determined by:

- n, which is fixed at 16
- m, which is adjustable with register R0x0404
- Legal values for m are 16 through 96, giving the user the ability to scale from 1:1 (m=16) to 1:6 (m=96).

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

4X4 Sub-sampling (X:Skip2Bin2 Y:Sum2Skip2)

Figure 12: X: Skip2Bin2 Y:Sum2Skip2

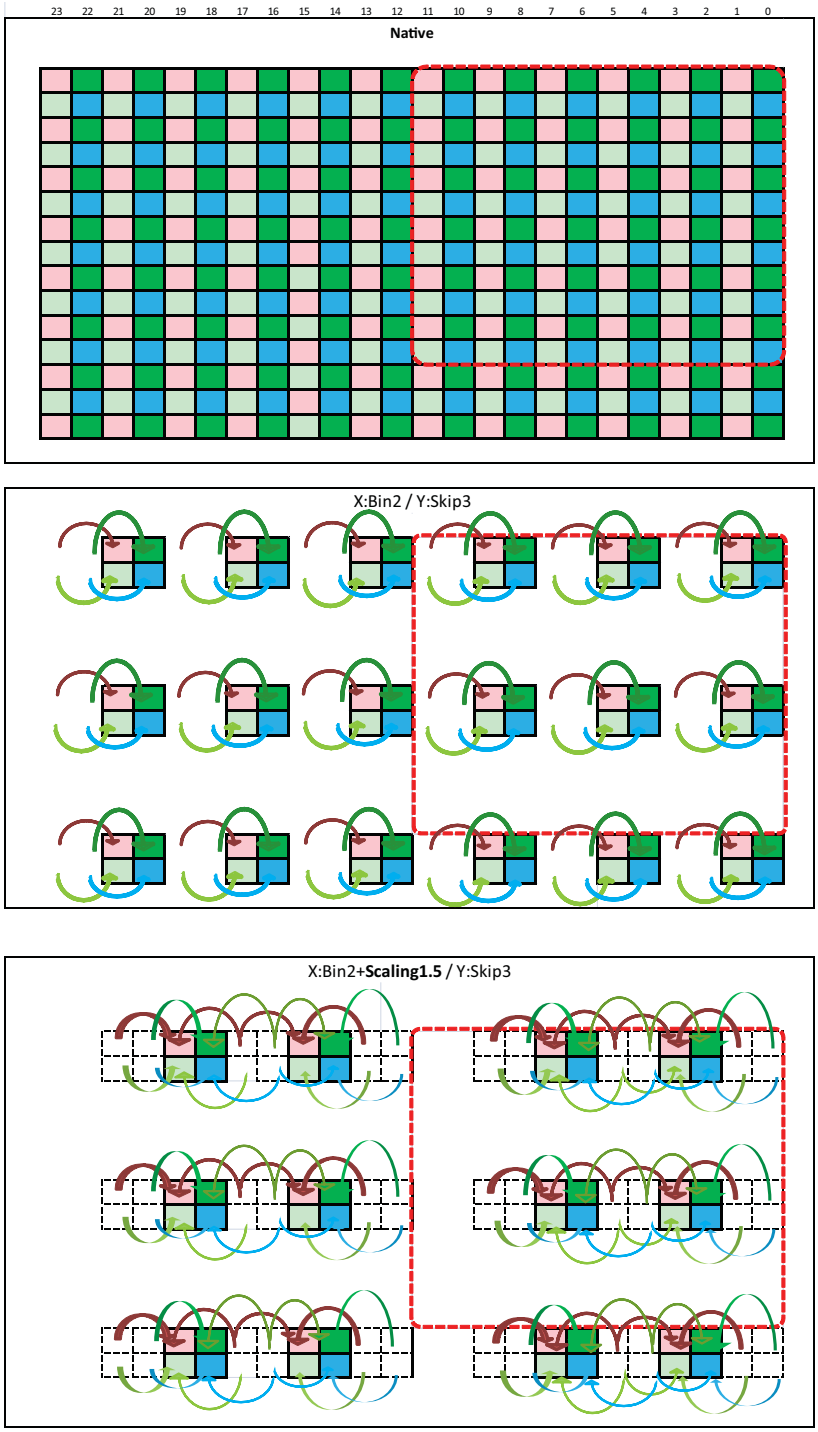


Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

3x3 sub-sampling (X:Bin2+scale1.5 / Y-skip3)

Figure 29 is to illustrate the 3x3 readout mode, however, it is a simplified figure which presents the re-sampling digital address logically, but not 100% accuracy for physical spaciously.

Figure 13: X:Bin2+scale1.5 / Y-skip3



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Frame Rate Control

The formulas for calculating the frame rate of the AR1820HS are shown below.

The line length is programmed directly in pixel clock periods through register line_length_pck. For a specific window size, the minimum line length can be found from Equation 5:

$$minimum\ line\_length\_pck = \left(\frac{x\_addr\_end - x\_addr\_start\ + 1}{subsampling\ factor} + min\_line\_blanking\_pck\right) \quad \text{(EQ 5)}$$

Note that line_length_pck also needs to meet the minimum line length requirement set in register min_line_length_pck. The row time can either be limited by the time it takes to sample and reset the pixel array for each row, or by the time it takes to sample and read out a row. Values for min_line_blanking_pck are provided in “Minimum Row Time” on page 50.

The frame length is programmed directly in number of lines in the register frame_line_length. For a specific window size, the minimum frame length can be found in Equation 6:

$$minimum\ frame\_length\_lines = \left(\frac{y\_addr\_end - y\_addr\_start\ + 1}{subsampling\ factor} + min\_frame\_blanking\_lines\right) \quad \text{(EQ 6)}$$

The frame rate can be calculated from these variables and the pixel clock speed as shown in Equation 7:

$$frame\ rate = \frac{vt\_pixel\_clock\_mhz\ x\ 1\ x\ 10^6}{line\_length\_pck\_x\ frame\_length\_lines} \quad \text{(EQ 7)}$$

If coarse_integration_time is set larger than frame_length_lines the frame size will be expanded to coarse_integration_time + 1.

Minimum Row Time

Enough time must be given to the output FIFO so it can output all data at the set frequency within one row time.

There are therefore two checks that must all be met when programming line_length_pck:

- line_length_pck ≥ min_line_length_pck in Table 17.
- The row time must allow the FIFO to output all data during each row. That is, line_length_pck ≥ (x_output_size * 2 + 0x005E) * “vt_pix_clk period” / “op_pix_clk period”

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Minimum Number of Rows

The minimum number of active rows in the image is 2, so min_frame_length_lines will always equal (min_frame_blanking_lines + 2).

The number of min_Frame_blanking_lines will be changed according to the mode.

Table 4: Minimum Number of Rows and Blanking Numbers

	Value
min_frame_blanking_lines	Hex.: 0x54 (Dec.:53)
min_frame_length_lines	Hex.: 0x37 (Dec.:55)

Integration Time

The integration (exposure) time of the AR1820HS is controlled by the coarse_integration_time register.

The limits for the coarse integration time are defined by:

$$coarse\_integration\_time\_min \leq coarse\_integration\_time \quad (EQ\ 8)$$

The actual integration time is given by:

$$integration\_time = \frac{(coarse\_integration\_time \times line\_length\_pck)}{(vt\_pix\_clk\_freq\_mhz \times 10^{6}) \times 4} \quad (EQ\ 9)$$

It is required that:

$$coarse\_integration\_time \leq (frame\_length\_lines - coarse\_integration\_time\_max\_margin) \quad (EQ\ 10)$$

Note: For AR1820HS, "coarse_integration_time_max_margin" should be 1.

If this limit is broken, the frame time will automatically be extended to (coarse_integration_time + coarse_integartion_time_max_margin) to accommodate the larger integration time.

In binning mode, frame_length_lines should be set larger than coarse_integration_time by at least 3 to avoid column imbalance artifact.

Flash Timing Control

The AR1820HS supports both xenon and LED flash timing through the FLASH output signal. The timing of the FLASH signal with the default settings is shown in Figure 30 (xenon) and Figure 31 on page 52 (LED). The flash and flash_count registers allow the timing of the flash to be changed. The flash can be programmed to fire only once, delayed by a few frames when asserted, and (for xenon flash) the flash duration can be programmed.

Enabling the LED flash will cause one bad frame, where several of the rows only have the flash on for part of their integration time. This can be avoided either by first enabling mask bad frames (R0x301A[9] = 1) before the enabling the flash or by forcing a restart (R0x301A[1] = 1) immediately after enabling the flash; the first bad frame will then be masked out, as shown in Figure 31. Read-only bit flash[14] is set during frames that are correctly integrated; the state of this bit is shown in Figures 30 and Figure 31.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 14: Xenon Flash Enabled

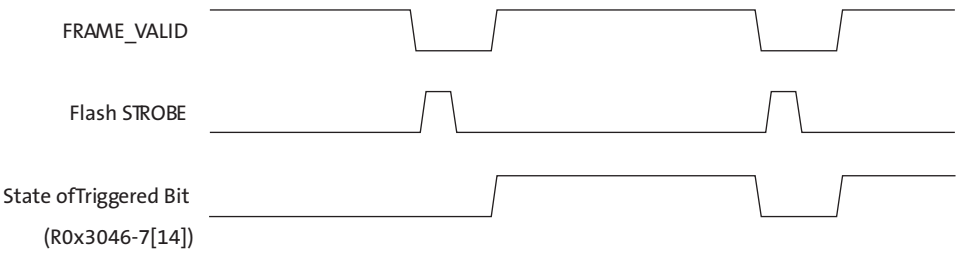
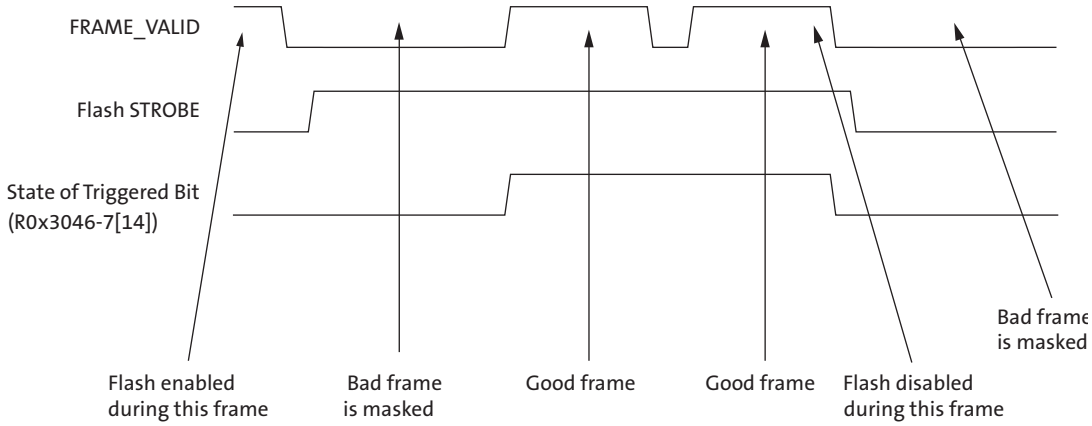


Figure 15: LED Flash Enabled



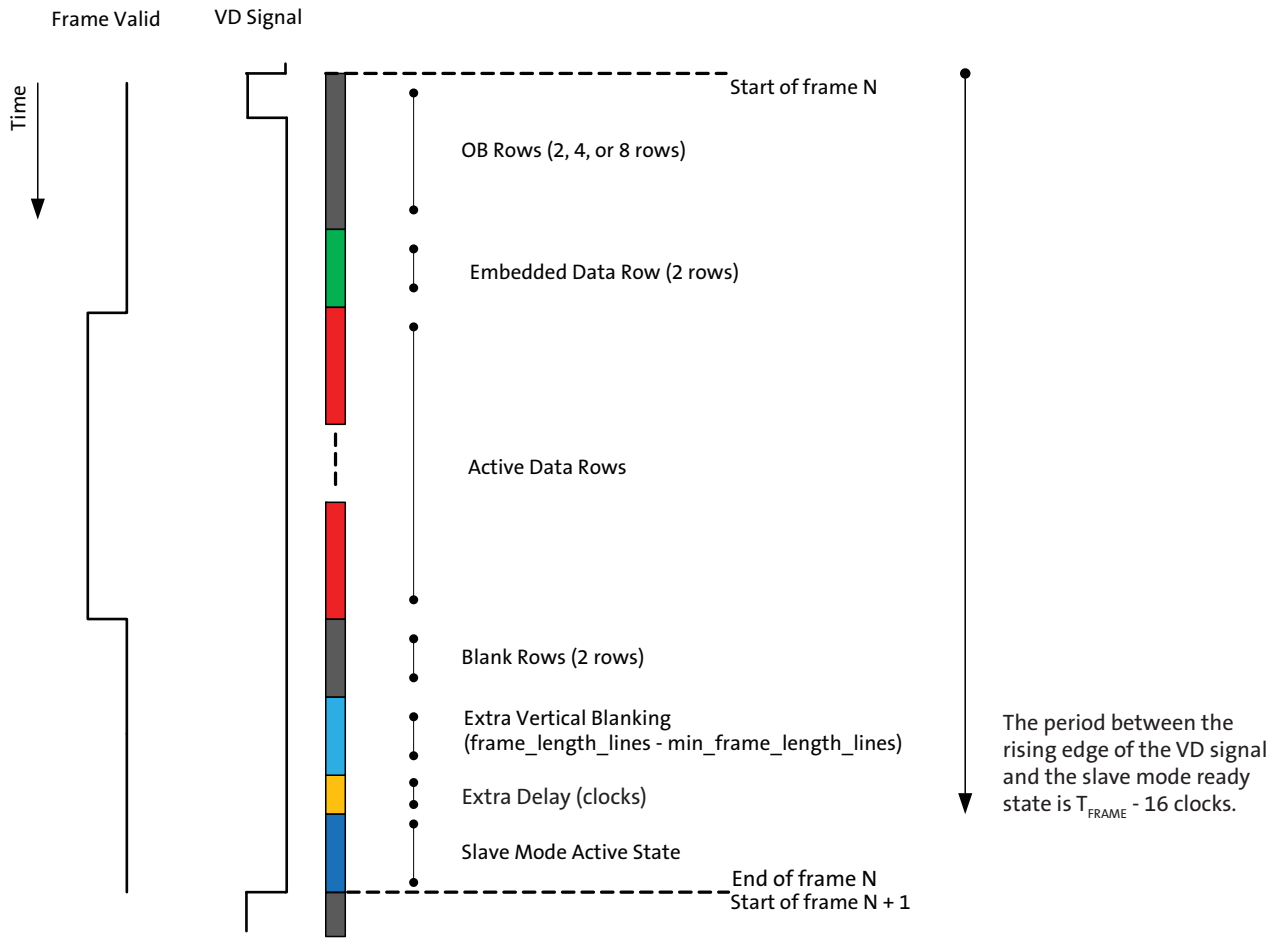
Note: An option to invert the flash output signal through R0x3046[7] is also available.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Slave Mode

The slave mode feature of the AR1820HS supports triggering the start of a frame readout from a VD signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates. The VD signal is input to the trigger pin. Both the GPI_EN (R0x301A[8]) and the SLAVE_MODE (R0x3158[15]) bits must be set to "1" to enable the slave mode.

Figure 16: Slave Mode Active State and Vertical Blanking

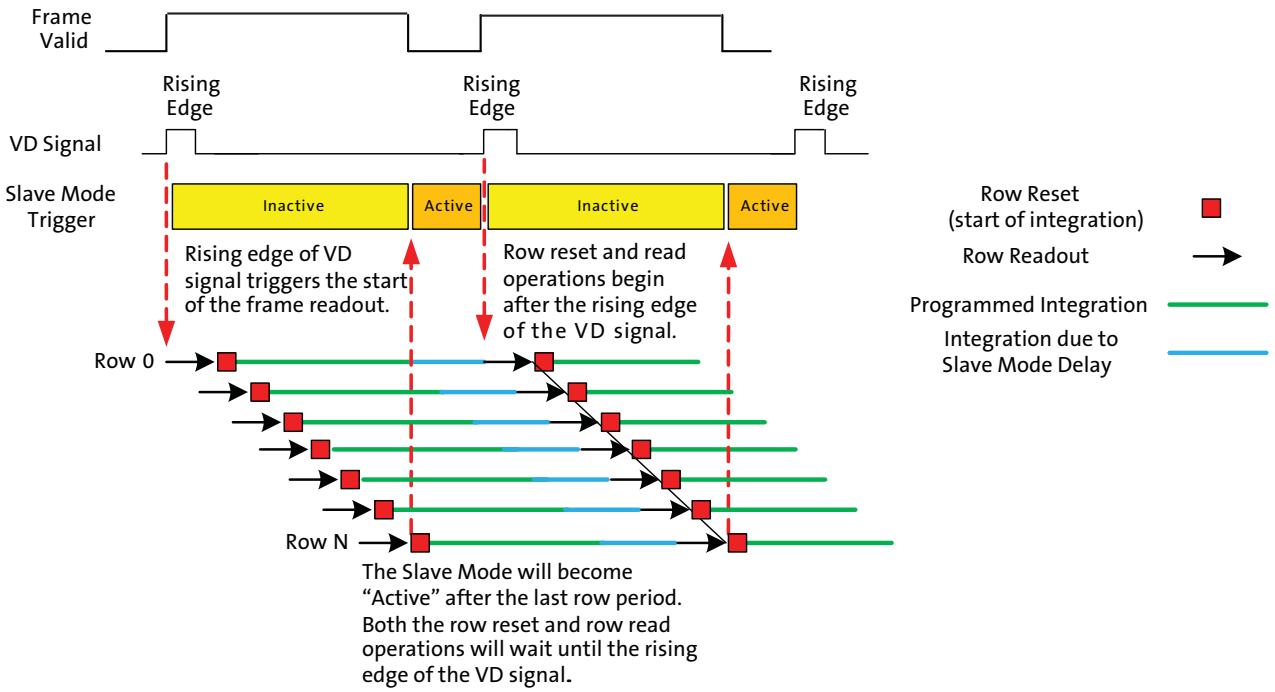


If the slave mode is disabled, the new frame will begin after the extra delay period is finished.

The slave mode will react to the rising edge of the input VD signal if it is in an active state. When the VD signal is received, the sensor will begin the frame readout and the slave mode will remain inactive for the period of one frame time minus 16 clock periods (T_{FRAME} - (16 / CLK_PIX)). After this period, the slave mode will re-enter the active state and will respond to the VD signal.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 17: Slave Mode Example with Equal Integration and Frame Readout Periods
The integration of the last row is therefore started before the end of the programmed integration for the first row.



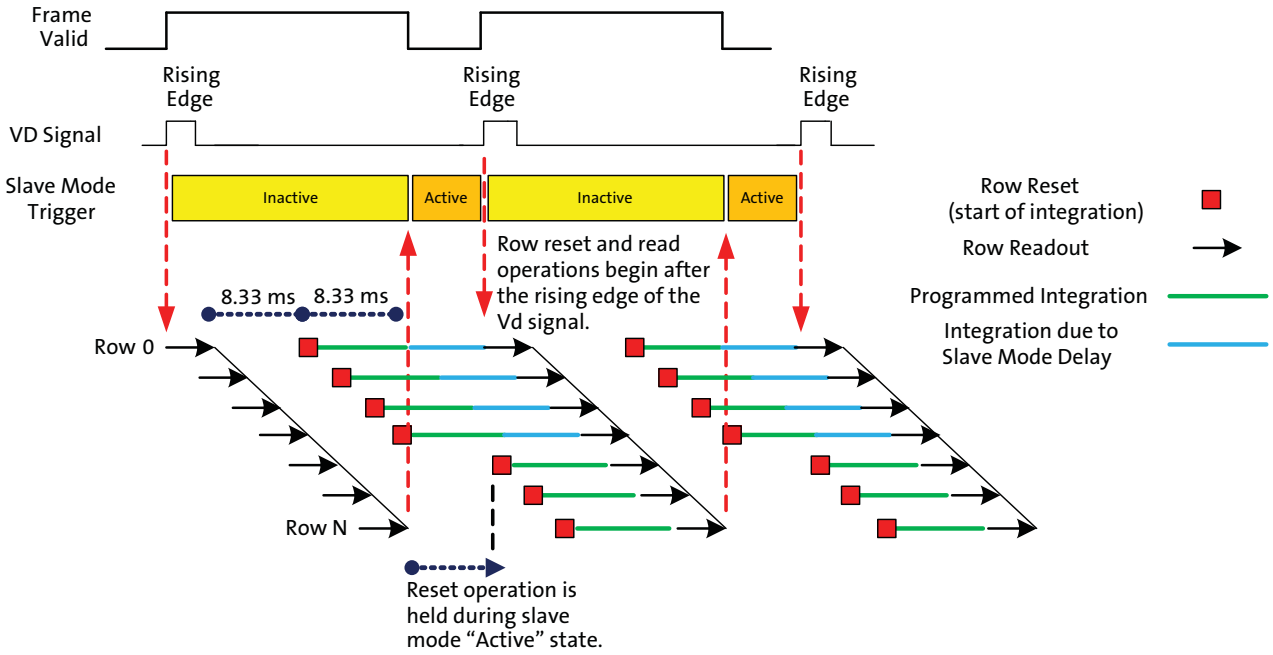
The row shutter and read operations will stop when the slave mode becomes active and is waiting for the VD signal. The following should be considered when configuring the sensor to use the slave mode:

1. The frame period (T_{FRAME}) should be configured to be less than the period of the input VD signal. The sensor will disregard the input VD signal if it appears before the frame readout is finished.
2. If the sensor integration time is configured to be less than the frame period, then the sensor will not have reset all of the sensor rows before it begins waiting for the input VD signal. This error can be minimized by configuring the frame period to be as close as possible to the desired frame rate (period between VD signals).

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 18: Slave Mode Example Where the Integration Period is Half of the Frame Readout Period

The sensor read pointer will have paused at row 0 while the shutter pointer pauses at row N/2. The extra integration caused by the slave mode delay will only be seen by rows 0 to N/2. The example below is for a frame readout period of 16.6ms while the integration time is configured to 8.33ms.



When the slave mode becomes active, the sensor will pause both row read and row reset operations.

Note: The row integration period is defined as the period from row reset to row read.

The frame-time should therefore be configured so that the slave mode "wait period" is as short as possible. In the case where the sensor integration time is shorter than the frame time, the "wait period" will only increase the integration of the rows that have been reset following the last VD pulse.

The period between slave mode pulses must also be greater than the frame period. If the rising edge of the VD pulse arrives while the slave mode is inactive, the VD pulse will be ignored and will wait until the next VD pulse has arrived.

Figure 19: Example of the Slave Mode with a Flat-field Illumination

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

The sensor frame-time is 33ms (or 30.3Hz) and the integration is 16.6ms. The left image shows the resulting output with an input VD signal 29.97Hz. The right image is the result of an input VD signal of 25Hz.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Frame Readout

The sensor readout begins with vertical blanking rows followed by the active rows. The frame readout period can be defined by the number of row periods within a frame (*frame_length_lines*) and the row period (*line_length_pck/cockpits*). The sensor will read the first vertical blanking row at the beginning of the frame period and the last active row at the end of the row period.

Figure 20: Example of the Sensor Output of a 2304 x 1296 Frame at 60 fps

The frame valid and line valid signals mentioned in this diagram represent internal signals within the sensor. The SYNC codes represented in this diagram represent the HiSPi Streaming SP protocol.

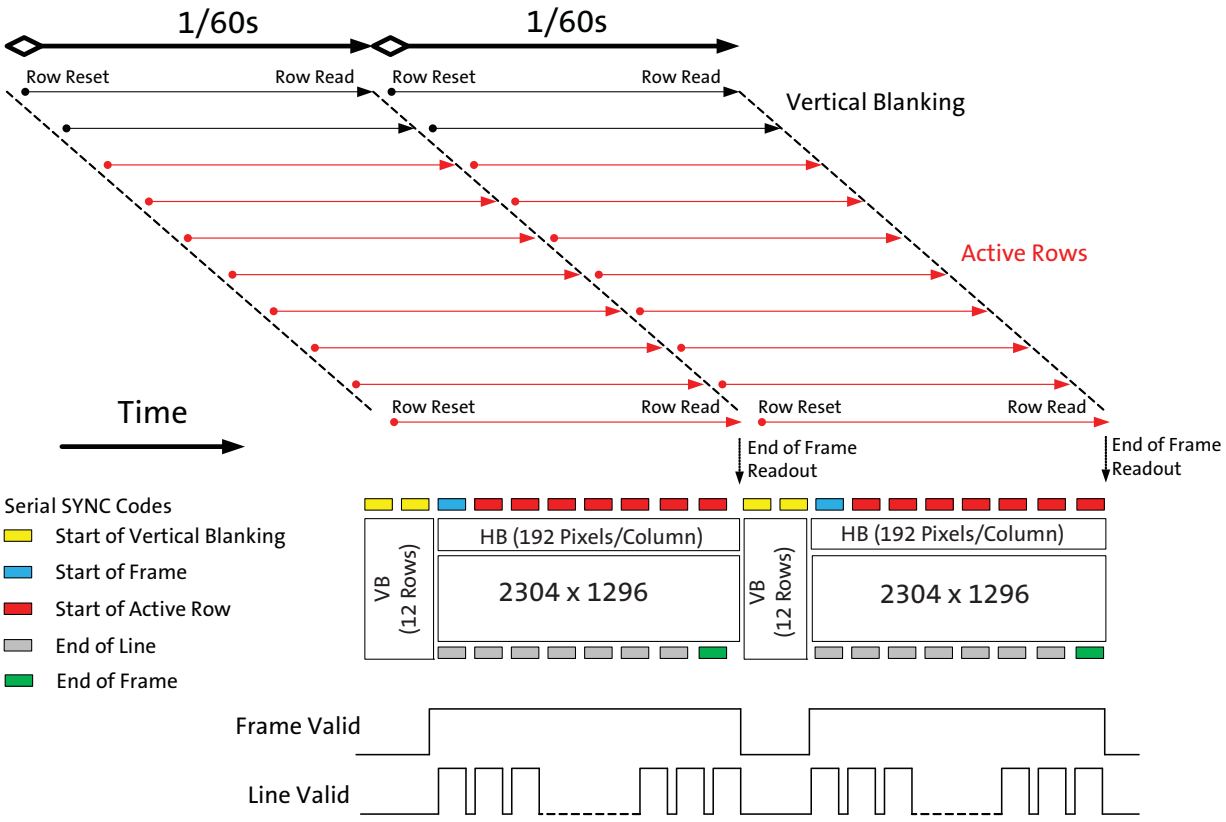


Figure 36 aligns the frame integration and readout operation to the sensor output. It also shows the sensor output using the HiSPi Streaming SP protocol. Different sensor protocols will list different SYNC codes.

Table 5: Serial SYNC Codes Included with Each Protocol Included with the AR1820HS Sensor

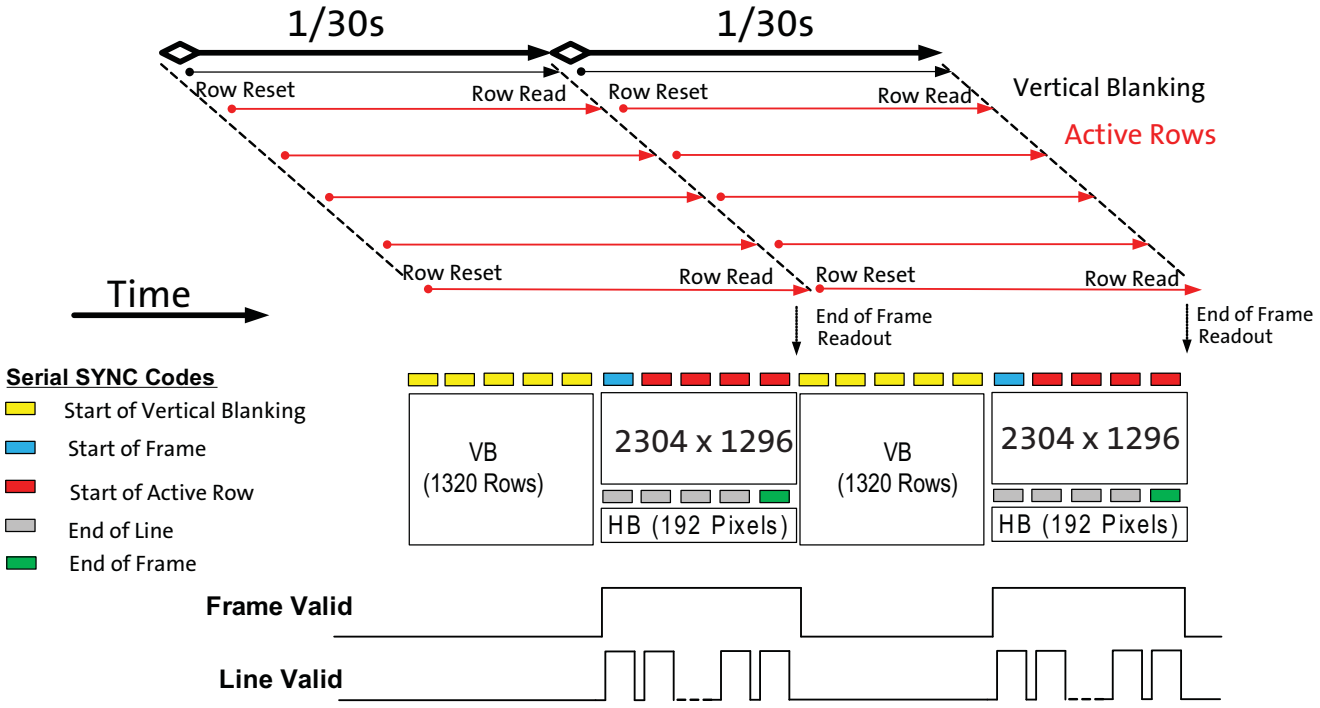
Interface/Protocol	Start of Vertical Blanking Row (SOV)	Start of Frame (SOF)	Start of Active Line (SOA)	End of Line (EOL)	End of Frame (EOF)
Parallel	Parallel interface uses FRAME VALID(FV) and LINE VALID (LV) outputs to denote start and end of line and frame.				
HiSPi Streaming S	Yes	Send SOV	Yes	No SYNC Code	No SYNC Code
HiSPi Streaming SP	Yes	Yes	Yes	Yes	Yes
HiSPi Packetized SP	No SYNC Code	Yes	Yes	Yes	Yes
MIPI	No SYNC Code	Yes	Yes	Yes	Yes

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 37 illustrates how the sensor active readout time can be minimized while reducing the frame rate. 1308 VB rows were added to the output frame to reduce the 2304 x1296 frame rate from 60 fps to 30 fps without increasing the delay between the readout of the first and last active row.

Figure 21: Example of the Sensor Output of a 2304 x1296 Frame at 30 fps

The frame valid and line valid signals mentioned in this diagram represent internal signals within the sensor. The SYNC codes represented in this diagram represent the HiSPi Streaming SP protocol.



Global Reset Release (GRR)

Global reset mode allows the integration time of the AR1820HS to be controlled by an external electromechanical shutter. Global reset mode is generally used in conjunction with ERS mode. The ERS mode is used to provide viewfinder information, the sensor is switched into global reset mode to capture a single frame, and the sensor is then returned to ERS mode to restore viewfinder operation.

Overview of Global Reset Sequence

The basic elements of the global reset sequence are:

1. By default, the sensor operates in ERS mode and the SHUTTER output signal is LOW. The electromechanical shutter must be open to allow light to fall on the pixel array. Integration time is controlled by the coarse_integration_time register.
2. A global reset sequence is triggered.
3. All of the rows of the pixel array are placed in reset.
4. All of the rows of the pixel array are taken out of reset simultaneously. All rows start to integrate incident light. The electromechanical shutter may be open or closed at this time.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

5. If the electromechanical shutter has been closed, it is opened.
6. After the desired integration time (controlled internally or externally to the AR1820HS), the electromechanical shutter is closed.
7. A single output frame is generated by the sensor with the usual LV, FV, PIXCLK, and DOUT timing. As soon as the output frame has completed (FV negates), the electromechanical shutter may be opened again.
8. The sensor automatically resumes operation in ERS mode.

This sequence is shown in Figure 38. The following sections expand to show how the timing of this sequence is controlled.

Figure 22: Overview of Global Reset Sequence

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Entering and Leaving the Global Reset Sequence

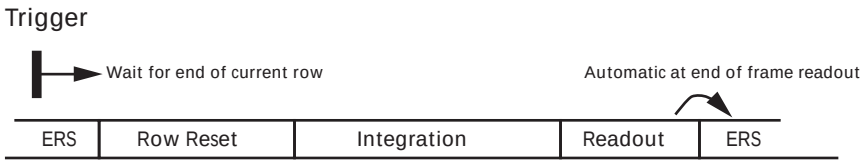
A global reset sequence can be triggered by a register write to R0x315E global_seq_trigger[0] (global trigger, to transition this bit from a 0 to a 1) or by a rising edge on a suitably-configured GPI input).

When a global reset sequence is triggered, the sensor waits for the end of the current row. When LV negates for that row, FV is negated 6 PIXCLK periods later, potentially truncating the frame that was in progress.

The global reset sequence completes with a frame readout. At the end of this readout phase, the sensor automatically resumes operation in ERS mode. The first frame integrated with ERS will be generated after a delay of approximately ((13 + coarse_integration_time) * line_length_pck). This sequence is shown in Figure 39.

While operating in ERS mode, double-buffered registers ("Double-Buffered Registers" on page 33) are updated at the start of each frame in the usual way. During the global reset sequence, double-buffered registers are updated just before the start of the readout phase.

Figure 23: Entering and Leaving a Global Reset Sequence



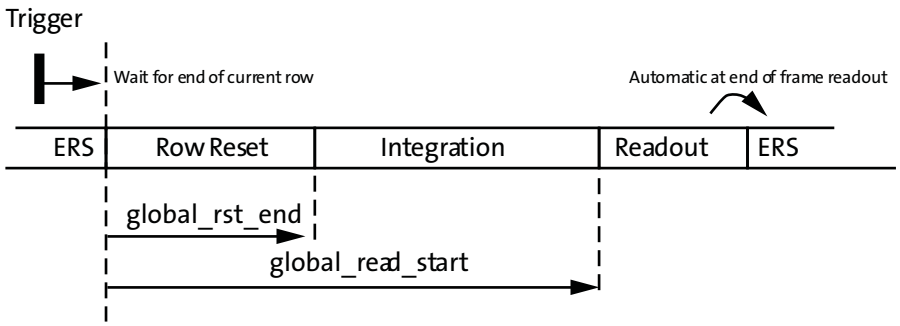
Programmable Settings

The registers global_rst_end and global_read_start allow the duration of the row reset phase and the integration phase to be controlled, as shown in Figure 40. The duration of the readout phase is determined by the active image size.

The recommended setting for global_rst_end is 0x3160 (for example, 512 µs total reset time) with default vt_pix_clk. This allows sufficient time for all rows of the pixel array to be set to the correct reset voltage level. The row reset phase takes a finite amount of time due to the capacitance of the pixel array and the capability of the internal voltage booster circuit that is used to generate the reset voltage level.

As soon as the global_rst_end count has expired, all rows in the pixel array are taken out of reset simultaneously and the pixel array begins to integrate incident light.

Figure 24: Controlling the Reset and Integration Phases of the Global Reset Sequence

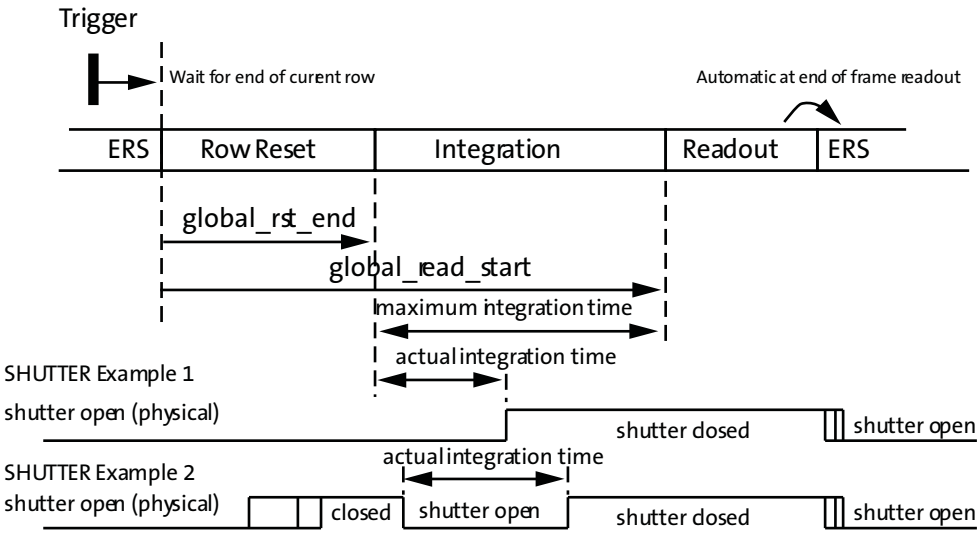


Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Control of the Electromechanical Shutter

Figure 41 on page 61 shows two different ways in which a shutter can be controlled during the global reset sequence. In both cases, the maximum integration time is set by the difference between global_read_start and global_rst_end. In shutter example 1, the shutter is open during the initial ERS sequence and during the row reset phase. The shutter closes during the integration phase. The pixel array is integrating incident light from the start of the integration phase to the point at which the shutter closes. Finally, the shutter opens again after the end of the readout phase. In shutter example 2, the shutter is open during the initial ERS sequence and closes sometime during the row reset phase. The shutter both opens and closes during the integration phase. The pixel array is integrating incident light for the part of the integration phase during which the shutter is open. As for the previous example, the shutter opens again after the end of the readout phase.

Figure 25: Control of the Electromechanical Shutter



It is essential that the shutter remains closed during the entire row readout phase (that is, until FV has negated for the frame readout); otherwise, some rows of data will be corrupted (over-integrated).

It is essential that the shutter closes before the end of the integration phase. If the row readout phase is allowed to start before the shutter closes, each row in turn will be integrated for one row-time longer than the previous row.

After FV negates to signal the completion of the readout phase, there is a time delay of approximately (10 * line_length_pck) before the sensor starts to integrate light-sensitive rows for the next ERS frame. It is essential that the shutter be opened at some point in this time window; otherwise, the first ERS frame will not be uniformly integrated.

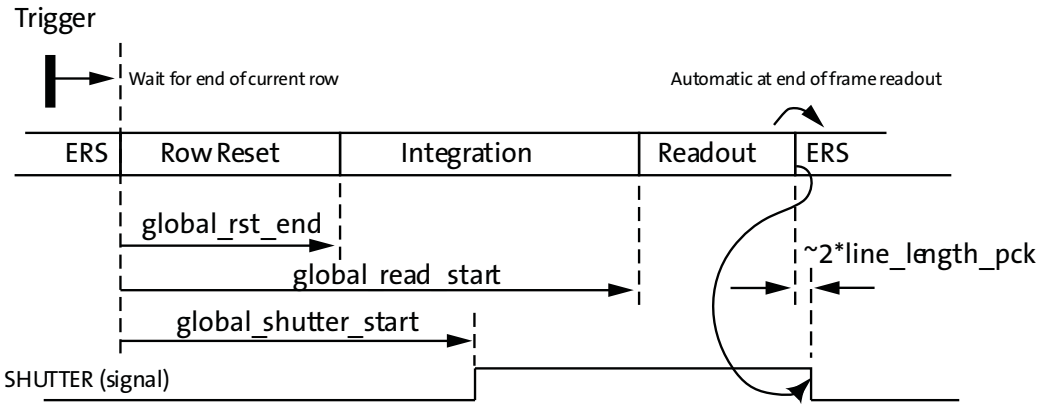
The AR1820HS provides a SHUTTER output signal to control (or help the host system control) the electromechanical shutter. The timing of the SHUTTER output is shown in Figure 42 on page 62. SHUTTER is negated by default. The point at which it asserts is controlled by the programming of global_shutter_start. At the end of the global reset readout phase, SHUTTER negates approximately (2 * line_length_pck) after the negation of FV.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

This programming restriction must be met for correct operation:

- global_read_start > global_shutter_start.

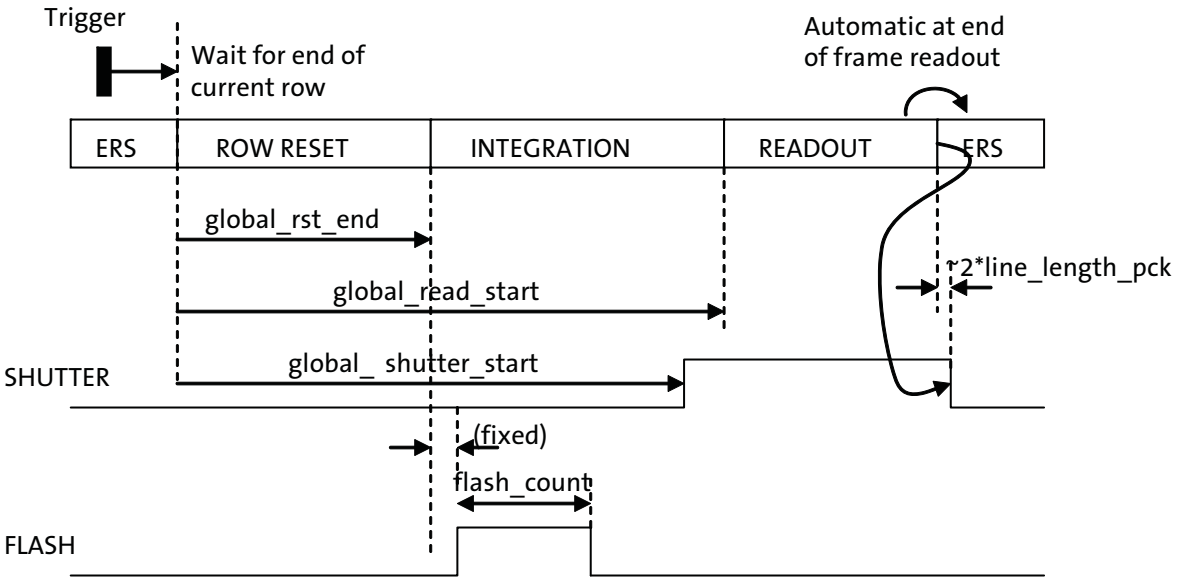
Figure 26: Controlling the SHUTTER Output



Using FLASH with Global Reset

If R0x315E global_seq_trigger[2] = 1 (global flash enabled) when a global reset sequence is triggered, the FLASH output signal will be pulsed during the integration phase of the global reset sequence. The FLASH output will assert a fixed number of cycles after the start of the integration phase and will remain asserted for a time that is controlled by the value of the flash_count register. When flash_count is programmed for value N, (where N is 0–0x3FE) the resulting flash duration is given by N * 512 * (1/vt_pix_clk_freq_mhz), as shown in Figure 43.

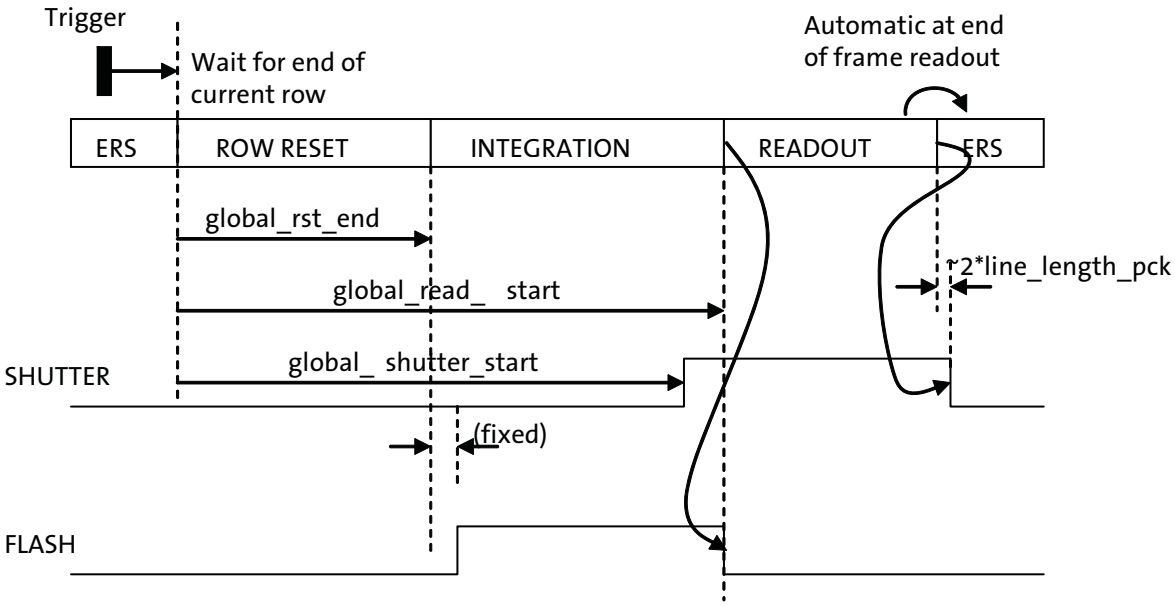
Figure 27: Using FLASH with Global Reset



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

When the flash_count = 0x3FF, the flash signal will be maximized and goes LOW when readout starts, as shown in Figure 44 on page 63. This would be preferred if the latency in closing the shutter is longer than the latency for turning off the flash. This guarantees that the flash stays on while the shutter is open.

Figure 28: Extending FLASH Duration in Global Reset (Reference Readout Start)



External Control of Integration Time

If global_seq_trigger[1] = 1 (global bulb enabled) when a global reset sequence is triggered, the end of the integration phase is controlled by the level of trigger (global_seq_trigger[0] or the associated GPI input). This allows the integration time to be controlled directly by an input to the sensor.

This operation corresponds to the shutter "B" setting on a traditional camera, where "B" originally stood for "Bulb" (the shutter setting used for synchronization with a magnesium foil flash bulb) and was later considered to stand for "Brief" (an exposure that was longer than the shutter could automatically accommodate).

When the trigger is de-asserted to end integration, the integration phase is extended by a further time given by *global_read_start – global_shutter_start*. Usually this means that global_read_start should be set to *global_shutter_start + 1*.

The operation of this mode is shown in Figure 45 on page 64. The figure shows the global reset sequence being triggered by the GPI2 input, but it could be triggered by any of the GPI inputs or by the setting and subsequence clearing of the global_seq_trigger[0] under software control.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

The integration time of the GRR sequence is defined as:

$$integration\_time = \frac{global\_scale \times [global\_read\_start - global\ shutter\_start - global\_rst\_end]}{(vt\_pix\_clk\_freq\_mhz \times 10^6) \times 4} \quad \text{(EQ 11)}$$

Where:

$$global\_read\_start = (2^{16} \times global\_read\_start2[7:0] + global\_read\_start1[15:0]) \quad \text{(EQ 12)}$$

$$global\_shutter\_start = (2^{16} \times global\_shutter\_start2[7:0] + global\_shutter\_start1[15:0]) \quad \text{(EQ 13)}$$

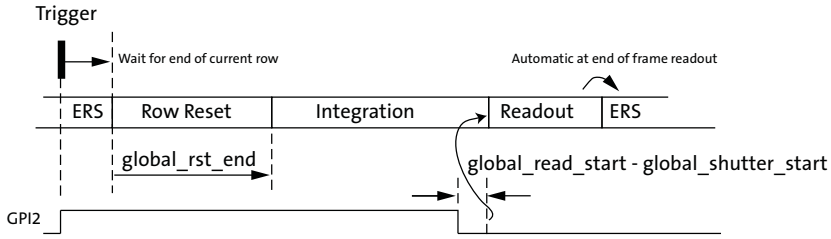
The integration equation allows for 24-bit precision when calculating both the shutter and readout of the image. The global_rst_end has only 16-bit as the array reset function and requires a short amount of time.

The integration time can also be scaled using global_scale. The variable can be set to 0–512, 1–2048, 2–128, and 3–32.

These programming restrictions must be met for correct operation of bulb exposures:

- global_read_start > global_shutter_start
- global_shutter_start > global_rst_end
- global_shutter_start must be smaller than the exposure time (that is, this counter must expire before the trigger is de-asserted)

Figure 29: Global Reset Bulb



Retriggering the Global Reset Sequence

The trigger for the global reset sequence is edge-sensitive; the global reset sequence cannot be retriggered until the global trigger bit (in the R0x315E global_seq_trigger register) has been returned to "0," and the GPI (if any) associated with the trigger function has been negated.

The earliest time that the global reset sequence can be retriggered is the point at which the SHUTTER output negates; this occurs approximately (2 * line_length_pck) after the negation of FV for the global reset readout phase.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Using Global Reset

When a global reset sequence is triggered, it usually results in the frame in progress being truncated (at the end of the current output line). The data path limiter function (see Figure 46 on page 65) attempts to extend (pad) all frames to the programmed value of y_output_size. If this padding is still in progress when the global reset readout phase starts, the data path will not detect the start of the frame correctly. Therefore, to use global reset with the serial data path, this timing scenario must be avoided. One possible way of doing this would be to synchronize (under software control) the assertion of trigger to an end-of-frame marker on the serial data stream.

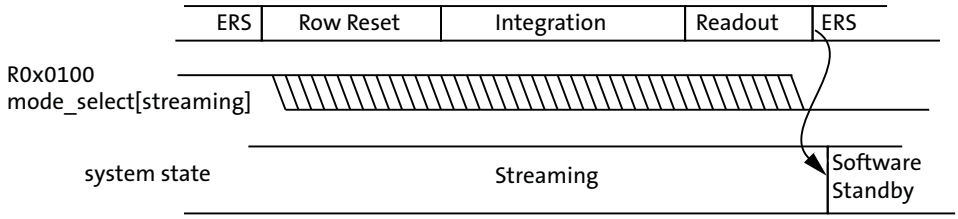
At the end of the readout phase of the global reset sequence, the sensor automatically resumes operation in ERS mode.

The frame that is read out of the sensor during the global reset readout phase has exactly the same format as any other frame out of the serial pixel data interface, including the addition of two lines of embedded data. The value of the coarse_integration_time register within the embedded data matches the programmed values of those registers and does not reflect the integration time used during the global reset sequence.

Global Reset and Soft Standby

If the R0x301A[2] mode_select[stream] bit is cleared while a global reset sequence is in progress, the AR1820HS will remain in streaming state until the global reset sequence (including frame readout) has completed, as shown in Figure 46 on page 65.

Figure 30: Entering Soft Standby During a Global Reset Sequence



Continuous GRR Mode

AR1820HS also features continuous GRR capturing.

- Unlike previous part (for example, A-14041), after GRR frame readout completed, sensor will automatically go back to ERS mode.
- AR1820HS has an option of keeping sensor staying at GRR mode operation.
- This feature is controlled by programming R0x3158[12]:
  - R0x3158[12] is frame sync controlled.
  - The sensor will remain at GRR mode if R0x3158[12] stays at high.
  - When R0x3158[12] being pulled down, sensor will go back to ERS mode after end of current GRR frame.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Slave Mode ERS-GRR-ERS

Slave mode is to ensure having an ERS-GRR-ERS transition without a broken ERS frame before GRR. It requests to trigger or end the GRR sequence through the pin, which is similar to the GRR Bulb mode. The major difference to our existing sensor is to start the GRR sequence after the end of the current frame instead of starting immediately in the following row.

The AR1820HS sensor supports Slave mode to sync the frame rate more precisely, and simply by the VD signal from external ASIC. The VD signal also allows for precise control of frame rate and register change updates.

The VD signal for slave GRR mode is synchronized to ERS frame time, so that sensor can complete the current frame readout in ERS mode before moving to GRR mode, and avoid ERS broken frame before moving into GRR mode. Control bit vd_trigger_new_-frame bit allows VD triggering every new frame.

A GPI pin on the sensor can be programmed to act as VD input pin signal whose rising edge can be used to start every new frame (see Figure 64 on page 99 for details).

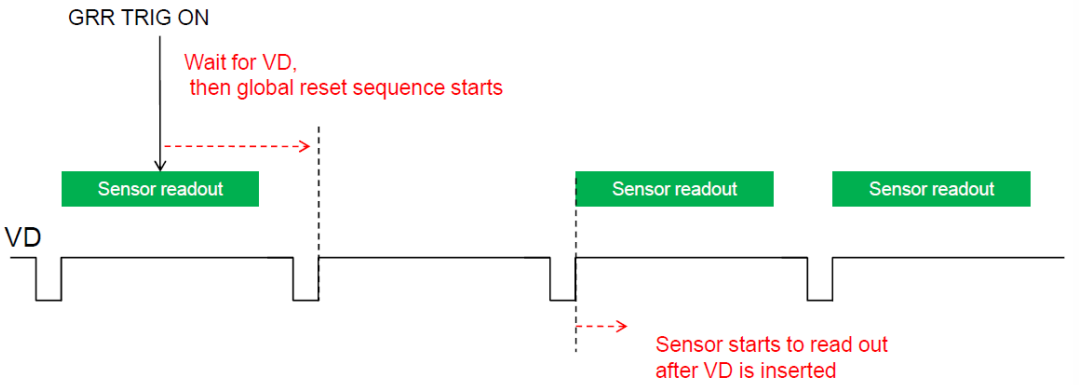
An optional functionality to limit the duration counters are halted is given by setting vd_timer bit to 1. When this bit is set the counters will not wait indefinitely for VD rising edge and resume normal counting after halting for a limited time. Otherwise when vd_timer is set to 0, internal row and column counters are halted until the arrival of VD's positive edge.

Slave Mode GRR

Global reset sequence is triggered by programming the global_seq_trigger bit. After this register bit is written the sensor will wait for rising edge of VD signal at the end of the current frame to go into GRR mode. The control bit needed to be set to enable this functionality is vd_trigger_grst. Once in the GRR integration phase, the sensor will wait for the next VD rising edge to begin the readout.

At the end of the readout phase, the sensor automatically resumes operation in ERS mode with readout of successive frames starting with rising edge of VD. Figure 48 and Figure 49 on page 67 are related timing diagrams:

Figure 31: Slave Mode ERS-GRR Transition



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Slave Mode GRR Timing

For example, to switch between ERS and GRR (and back to ERS), see Figure 48:

Figure 32: Slave Mode GRR Timing

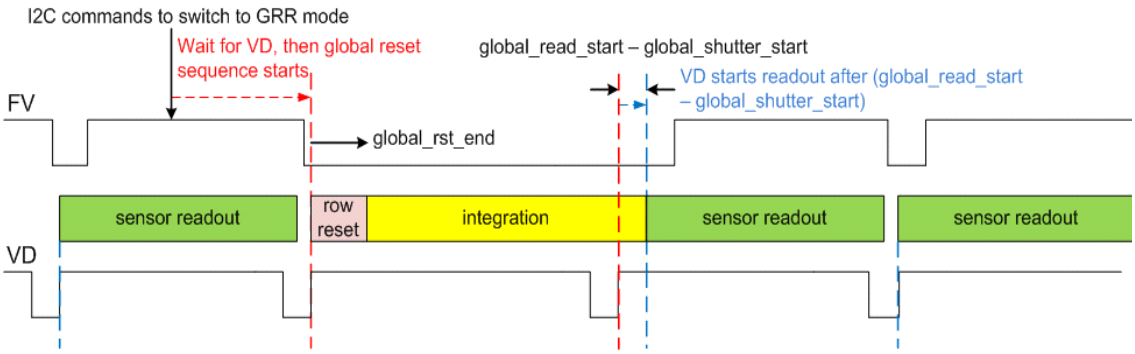
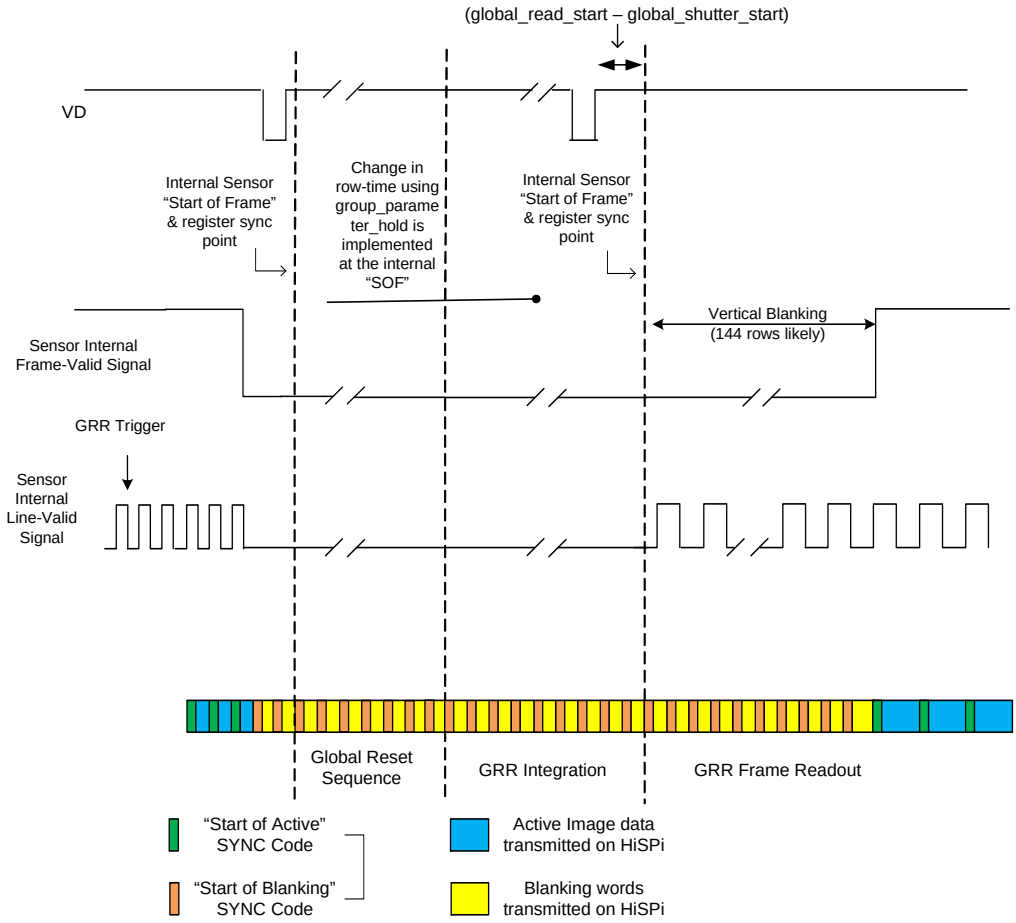


Figure 33: Slave Mode HiSPi Output (ERS to GRR Transition)



When GRR is triggered (by the rising edge of VD signal), the AR1820HS sensor starts GRR sequence and also send a start-of-blanking (SOB) SYNC code at the end of current ERS frame. It continues to send SOB sync codes during the entire GRR sequence.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Sensor Core Digital Data Path

Test Patterns

The AR1820HS supports a number of test patterns to facilitate system debug. Test patterns are enabled using test_pattern_mode (R0x0600–1). The test patterns are listed in Table 19.

Table 6: Test Patterns

test_pattern_mode	Description
0	Normal operation: no test pattern
1	Solid color
2	100% color bars
3	Fade-to-gray color bars
4	PN9 link integrity pattern (only on sensors with serial interface)
256	Walking 1s (12-bit value)
257	Walking 1s (10-bit value)
258	Walking 1s (8-bit value)

Test patterns 0–3 replace pixel data in the output image (the embedded data rows are still present). Test pattern 4 replaces all data in the output image (the embedded data rows are omitted and test pattern data replaces the pixel data).

HiSPi Test Patterns

Test patterns specific to the HiSPi are also generated. The test patterns are enabled by using test_enable (R0x31C6 - 7) and controlled by test_mode (R0x31C6[6:4]).

Table 7: HiSPi Test Patterns

test_mode	Description
0	Transmit a constant 0 on all enabled data lanes.
1	Transmit a constant 1 on all enabled data lanes.
2	Transmit a square wave at half the serial data rate on all enabled data lanes.
3	Transmit a square wave at the pixel rate on all enabled data lanes.
4	Transmit a continuous sequence of pseudo random data, with no SAV code, copied on all enabled data lanes.
5	Replace data from the sensor with a known sequence copied on all enabled data lanes.

For all of the test patterns, the AR1820HS registers must be set appropriately to control the frame rate and output timing. This includes:

- All clock divisors
- x_addr_start
- x_addr_end
- y_addr_start
- y_addr_end
- frame_length_lines
- line_length_pck
- x_output_size
- y_output_size

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Effect of Data Path Processing on Test Patterns

Test patterns are introduced early in the pixel data path. As a result, they can be affected by pixel processing that occurs within the data path. This includes:

- Noise cancellation
- Black pedestal adjustment
- Lens and color shading correction

These effects can be eliminated by the following register settings:

- R0x3044-5[10] = 0
- R0x30CA-B[0] = 1
- R0x30D4-5[15] = 0
- R0x31E0-1[0] = 0
- R0x3180-1[15] = 0
- R0x301A-B[3] = 0 (enable writes to data pedestal)
- R0x301E-F = 0x0000 (set data pedestal to 0)
- R0x3780[15] = 0 (turn off lens/color shading correction)

Solid Color Test Pattern

In this mode, all pixel data is replaced by fixed Bayer pattern test data. The intensity of each pixel is set by its associated test data register (test_data_red, test_data_greenR, test_data_blue, test_data_greenB).

100% Color Bars Test Pattern

In this test pattern, shown in Figure 41 on page 127, all pixel data is replaced by a Bayer version of an 8-color, color-bar chart (white, yellow, cyan, green, magenta, red, blue, black). Each bar is 1/8 of the width of the pixel array. The pattern repeats after eight bars.

Each color component of each bar is set to either 0 (fully off) or 0x3FF (fully on for 10-bit data). The pattern occupies the full height of the output image.

The image size is set by x_addr_start, x_addr_end, y_addr_start, y_addr_end and may be affected by the setting of x_output_size, y_output_size. The color-bar pattern is disconnected from the addressing of the pixel array, and will therefore always start on the first visible pixel, regardless of the value of x_addr_start. The number of colors that are visible in the output is dependent upon x_addr_end - x_addr_start and the setting of x_output_size: the width of each color bar is fixed.

The effect of setting horizontal_mirror in conjunction with this test pattern is that the order in which the colors are generated is reversed: the black bar appears at the left side of the output image. Any pattern repeat occurs at the right side of the output image regardless of the setting of horizontal_mirror. The state of vertical_flip has no effect on this test pattern.

The effect of subsampling, binning, and scaling of this test pattern is undefined.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 34: 100% Color Bars Test Pattern

Fade-to-gray Color Bars Test Pattern

In this test pattern, shown in Figure 42 on page 128, all pixel data is replaced by a Bayer version of an 8-color, color-bar chart (white, yellow, cyan, green, magenta, red, blue, black). Each bar is 1/8 of the width of the pixel array (2592/8 = 324 pixels). The test pattern repeats after 2592 pixels. Each color bar fades vertically from zero or full intensity at the top of the image to 50 percent intensity (mid-gray) on the last (968th) row of the pattern.

Each color bar is divided into a left and a right half, in which the left half fades smoothly and the right half fades in quantized steps. The speed at which each color fades is dependent on the sensor's data width and the height of the pixel array. We want half of the data range (from 100 or 0 to 50 percent) difference between the top and bottom of the pattern. Because of the Bayer pattern, each state must be held for two rows.

The rate-of-fade of the Bayer pattern is set so that there is at least one full pattern within a full-sized image for the sensor. Factors that affect this are the resolution of the ADC (10-bit or 12-bit) and the image height. For example, the MT9P013 fades the pixels by 2 LSB for each two rows. With 12-bit data, the pattern is 2048 pixels high and repeats after that, if the window is higher.

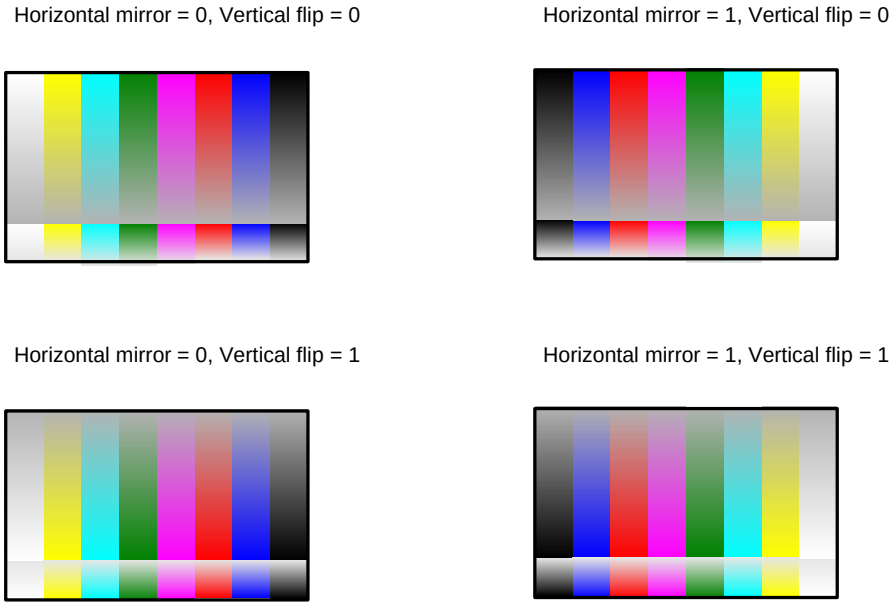
The image size is set by x_addr_start, x_addr_end, y_addr_start, y_addr_end and may be affected by the setting of x_output_size, y_output_size. The color-bar pattern starts at the first column in the image, regardless of the value of x_addr_start. The number of colors that are visible in the output is dependent upon x_addr_end - x_addr_start and the setting of x_output_size: the width of each color bar is fixed at 324 pixels.

The effect of setting horizontal_mirror or vertical_flip in conjunction with this test pattern is that the order in which the colors are generated is reversed: the black bar appears at the left side of the output image. Any pattern repeat occurs at the right side of the output image regardless of the setting of horizontal_mirror.

The effect of subsampling, binning, and scaling of this test pattern is undefined.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 35: Fade-to-Gray Color Bar Test Pattern



PN9 Link Integrity Pattern

The PN9 link integrity pattern is intended to allow testing of a serial pixel data interface. Unlike the other test patterns, the position of this test pattern at the end of the data path means that it is not affected by other data path corrections (row noise, pixel defect correction and so on).

This test pattern provides a 512-bit pseudo-random test sequence to test the integrity of the serial pixel data output stream. The polynomial x9 + x5 + 1 is used. The polynomial is initialized to 0x1FF at the start of each frame. When this test pattern is enabled:

- The embedded data rows are disabled and the value of frame_format_decriptor_1 changes from 0x1002 to 0x1000 to indicate that no rows of embedded data are present.
- The whole output frame, bounded by the limits programmed in x_output_size and y_output_size, is filled with data from the PN9 sequence.
- The output data format is (effectively) forced into RAW10 mode regardless of the state of the ccp_data_format register.

Before enabling this test pattern the clock divisors must be configured for RAW10 operation (op_pix_clk_div = 10).

This polynomial generates this sequence of 10-bit values: 0x1FF, 0x378, 0x1A1, 0x336, 0x385... On the parallel pixel data output, these values are presented 10-bits per PIXCLK.

On the serial pixel data output, these values are streamed out sequentially without performing the RAW10 packing to bytes that normally occurs on this interface.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Walking 1s

When selected, a walking 1s pattern will be sent through the digital pipeline. The first value in each row is 0. Each value will be valid for two pixels.

Figure 36: Walking 1s 12-Bit Pattern

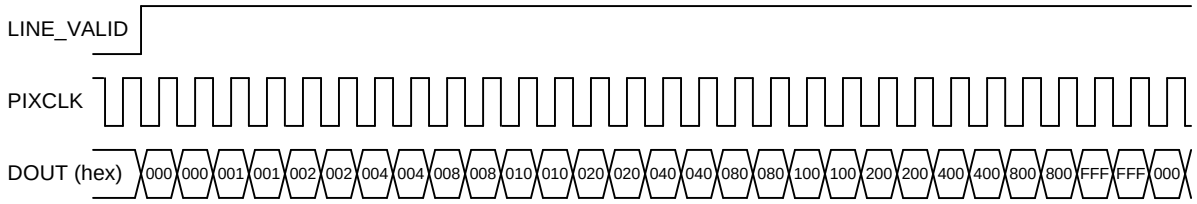
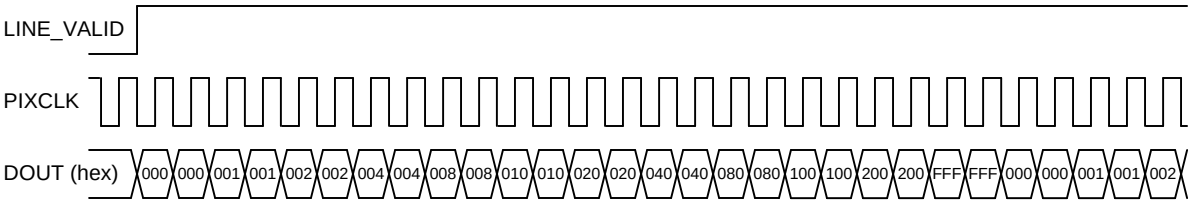


Figure 37: Walking 1s 10-Bit Pattern



The walking 1s pattern was implemented to facilitate assembly testing of modules with a parallel interface. The walking 1 test pattern is not active during the blanking periods; hence the output would reset to a value of 0x0. When the active period starts again, the pattern would restart from the beginning. The behavior of this test pattern is the same between full resolution and subsampling mode. RAW10 and RAW8 walking 1 modes are enabled by different test pattern codes.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Gain

AR1820HS supports both analog and digital gain.

Analog Gain

Analog gain is provided by colamp and ADC reference scaling (there is no ASC gain due to column parallel nature of column parallel architecture). Only global (not per-color) coarse gain can be set by analog gain. Global gain register (R0x305E) sets the analog gain. Bits [2:0] set the colamp gain while bits [6:3] are reserved for ADC gain. While the 3-bit colamp gain provides up to 8x analog gain, and it also need to be paired with writing match value at R0x3ED2.

Digital Gain

Digital gain provides both per-color and fine (sub 1x) gain. The analog and digital gains are multiplicative to give the total gain. Digital gain is set by setting bits R0x305E[15:7] to set global gain or by individually setting digital color gain R0x3056-C[15:7] where these 9 bits are designed in 2p5 format to support up to x16 with 1/64 step and the sub-1x gain provides the fine gain control for the sensor.

Total Gain

Maximum total gain required by design specification is 8x (analog) and 8x (digital) with min. step size of 1/64. The total gain equation can be formulated as:

$$\text{If R0x3ED2[15:12] = 14}\begin{cases} 0.64 \times 2^{\text{dec(R0x305E[2:0]-1)}} \times \dfrac{1}{1-(1/32)\times \text{dec(R0x305E[6:3])}} \times 2^{\text{dec(R0x3040[13]-1)+ dec(R0x3EE0[0]}} & \text{if dec(R0x305E[2:0] = 0. 1, 2, 3} \\ 0.64 \times 2^{\text{dec(R0x305E[2:0]-1}} \times 1 \times \dfrac{\text{dec(R0x305E[15:7]}}{64} \times 2^{\text{dec(R0x3040[13]) + dec(R0x3EE0[0])}} & \text{if dec(R0x305E[2:0] = 4} \\ 0.64 \times (1.5 \times \text{dec(R0x305E[2:0]} - 6) \times \dfrac{1}{1-(1/32)\text{dec(R0x305E[6:3]}} \times \dfrac{\text{dec(R0x305E[15:7]}}{64} \times 2^{\text{dec(R0x3040[13]) + dec(R0x3EE0[0])}} & \text{if dec(R0x305E[2:0] = 5, 6} \\ \text{DO NOT SUPPORT, if dec(R0x305E[2:0] = 7} & \end{cases} \quad \text{(EQ 14)}$$

$$\text{If R0x3ED2[15:12] = 4}\begin{cases} 1 \times 2^{\text{dec(R0x305E[2:0]-1)}} \times \dfrac{1}{1-(1/32)\times \text{dec(R0x305E[6:3])}} \times \dfrac{\text{dec(R0x305E[15:7]}}{64} \times 2^{\text{dec(R0x3040[13])+ dec(R0x3EE0[0]}} & \text{if dec(R0x305E[2:0] = 0. 1, 2, 3} \\ 1 \times 2^{\text{dec(R0x305E[2:0]-1}} \times 1 \times \dfrac{\text{dec(R0x305E[15:7]}}{64} \times 2^{\text{dec(R0x3040[13]) + dec(R0x3EE0[0])}} & \text{if dec(R0x305E[2:0] = 4} \\ 1 \times (1.5 \times \text{dec(R0x305E[2:0]} - 6) \times \dfrac{1}{1-(1/32)\text{dec(R0x305E[6:3]}} \times \dfrac{\text{dec(R0x305E[15:7]}}{64} \times 2^{\text{dec(R0x3040[13]) + dec(R0x3EE0[0])}} & \text{if dec(R0x305E[2:0] = 5, 6} \\ \text{DO NOT SUPPORT, if dec(R0x305E[2:0] = 7} & \end{cases} \quad \text{(EQ 15)}$$

Note: Aptina recommends using the registers mentioned above for gain settings. Avoid R0x3028 to R0x3038 unless their mapping to above registers is well understood and taken into account.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.

Table 8: Total Gain Setting Summary for Native Mode

Target Gain	R0x305E				R0x3ED2	R0x3040		R0x3EE0				R0x3EC8	R0x3EDC	R0x3ED8	R0x3ECC	R0x3F1A	R0x3F44
	Fine Gain		Digital Gain														
	[6:3]	Gain Value	[15:7]	Gain Value	[15:12]	[13]	[11]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	[15:0]
1	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
1.03	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
1.88	15	1.8823529	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
2	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
2.06	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
3.94	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
4	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
4.13	1	1.0322581	64	1	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
...	...	...	...	...	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
7.88	15	1.8823529	67	1.046875	4	0	0	0	0	0	1	7	1	0	3	0x0F04	0x0C0C
8	0	1	64	1	4	0	0	0	0	0	1	7	1	0	3	0x1E1E	0x0708
8.13	0	1	65	1.015625	4	0	0	0	0	0	1	7	1	0	3	0x1E1E	0x0708
...	0	1	...	...	4	0	0	0	0	0	1	7	1	0	3	0x1E1E	0x0708
15.5	0	1	124	1.9375	4	0	0	0	0	0	1	7	1	0	3	0x1E1E	0x0708
16	0	1	128	2	4	0	0	0	0	0	1	7	1	0	3	0x1919	0x0708

Note: R0x3040 will be changed during Mode switch.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.

Table 9: Total Gain Setting Summary for Subsampling

Target Gain	Hex	R305E						R0x3ED2	R0x3040		R0x3EE0				R0x 3EC8	R0x 3EDC	R0x 3ED8	R0x 3ECC	R0x 3F1A	R0x 3F44
		Coarse Gain		Fine Gain		Digital Gain														
		305E [2:0]	Gain Value	305E [6:3]	Gain Value	305E [15:7]	Gain Value	[15:12]	[13]	[14]	[0]	[1]	[15]	[6]	[7:4]	[0]	[4]	[11:8]	[15:0]	[15:0]
2	3089	1	0.64	1	1.0322581	97	1.515625	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
2.06	3091	1	0.64	2	1.0666667	97	1.515625	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
...	...	1	1	...	...	...	...	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
3.94	3279	1	0.64	15	1.8823529	100	1.5625	14	1	1	0	0	1	0	10	1	1	3	0x0404	0x0C0C
4	2002	2	2	0	1	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
4.13	200A	2	2	1	1.0322581	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
...	...	2	2	...	...	...	...	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
7.88	21FA	2	2	15	1.8823529	67	1.046875	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
8	2003	3	4	0	1	64	1	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x0C0C
8.13	2183	3	4	0	1	67	1.046875	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
...	...	3	4	...	...	...	...	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
15.5	3E03	3	4	0	1	124	1.9375	4	1	1	0	0	0	1	7	1	0	3	0x0404	0x1010
16	2004	4	8	0	1	64	1	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
16.75	2184	4	8	0	1	67	1.04687	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
...	...	4	8	0	1	...	...	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
31	3E04	4	8	0	1	124	1.9375	4	1	1	0	0	0	1	7	0	0	3	0x0504	0x0101
32	4004	4	8	0	1	128	2	4	1	1	0	0	0	1	7	0	0	3	0x0609	0x0101

Note: R0x3040 will be changed during Mode switch.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.

Table 10: Summary Native Gain

Gain Name for Native Mode	R0x305E	R0x3ED2	R0x3EE0	R 0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
1	2001	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.07	2011	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.14	2021	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.23	2031	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.33	2041	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.45	2051	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.6	2061	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.78	2071	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
1.88	2079	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2	2002	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.06	200A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.13	2012	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.21	201A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.29	2022	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.37	202A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.46	2032	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.56	203A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.67	2042	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.78	204A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
2.91	2052	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3	2152	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.1	20DA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.2	2062	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.37	206A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.56	2072	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.76	207A	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.82	20FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
3.94	21FA	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4	2003	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.13	200B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.27	2013	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.41	201B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.57	2023	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.74	202B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
4.92	2033	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
5.12	203B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
5.33	2043	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
5.57	204B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
5.82	2053	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
6.1	205B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
6.4	2063	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
6.6	2163	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
6.74	206B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
6.84	20EB	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 10: Summary Native Gain (continued)

Gain Name for Native Mode	R0x305E	R0x3ED2	R0x3EE0	R 0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
7.05	21EB	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.11	2073	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.22	20F3	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.33	2173	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.44	21F3	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.53	207B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.65	20FB	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.76	217B	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
7.88	21FB	449D	1558	1C9	0074	60A0	7386	0x0F04	0x0C0C
8	2004	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
8.38	2184	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
8.75	2304	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
9.13	2484	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
9.5	2604	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
9.88	2784	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
10.25	2904	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
10.63	2A84	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
11	2C04	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
11.38	2D84	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
11.75	2F04	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
12.13	3084	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
12.5	3204	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
12.88	3384	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
13.25	3504	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
13.63	3684	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
14	3804	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
14.38	3984	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
14.75	3B04	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
15.13	3C84	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
15.5	3E04	449D	1558	1C9	0074	60A0	7386	0x1E1E	0x0708
16	4004	449D	1558	1C9	0074	60A0	7386	0x1919	0x0101

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 11: Summary Subsampling Gain

Gain Name for Subsampling Mode	R0x305E	R0X3ED2	R 0x3EE0	R0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
2	3089	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.12	3019	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.28	3029	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
2.46	3039	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.02	31D9	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.27	30E9	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.41	3071	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
3.76	3279	E49D	9518	1C9	00A4	60B0	7386	0x0404	0x0101
4	2002	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.13	200A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.27	2012	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.41	201A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.57	2022	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
4.74	202A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5	20B2	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5.12	203A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5.33	2042	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5.57	204A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
5.82	2052	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
6	2152	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
6.19	20DA	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
6.4	2062	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
6.74	206A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
7.11	2072	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
7.53	207A	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
7.65	20FA	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
7.88	21FA	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
8	2003	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
8.26	200B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
8.53	2013	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
8.83	201B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
9.14	2023	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
9.48	202B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
9.85	2033	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
10.24	203B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
10.67	2043	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
11.13	204B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
11.64	2053	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
12.19	205B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
12.8	2063	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
13.2	2163	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
13.47	206B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
13.68	20EB	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
14.11	21EB	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 11: Summary Subsampling Gain (continued)

Gain Name for Subsampling Mode	R0x305E	R0X3ED2	R 0x3EE0	R0x3EDC	R 0x3EC8	R0X3ED8	R0X3ECC	R0x3F1A	R0x3F44
14.22	2073	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
14.44	20F3	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
14.67	2173	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
14.89	21F3	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
15.06	207B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
15.29	20FB	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
15.53	217B	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
15.76	21FB	449D	1558	1C9	0074	60A0	7786	0x0404	0x0101
16	2004	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
16.75	2184	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
17.5	2304	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
18.25	2484	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
19	2604	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
19.75	2784	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
20.5	2904	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
21.25	2A84	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
22	2C04	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
22.75	2D84	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
23.5	2F04	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
24.25	3084	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
25	3204	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
25.75	3384	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
26.5	3504	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
27.25	3684	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
28	3804	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
28.75	3984	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
29.5	3B04	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
30.25	3C84	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
31	3E04	449D	1558	1C8	0074	60A0	7786	0x0504	0x0101
32	4004	449D	1558	1C8	0074	60A0	7786	0x0609	0x0101

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Temperature Sensor

The AR1820HS has a built-in temperature sensor. The block is controlled independent of sensor timing and all communication happens through the two-wire serial interface.

Procedure

The AR1820HS On-chip Temperature Sensor readout procedure is shown below:

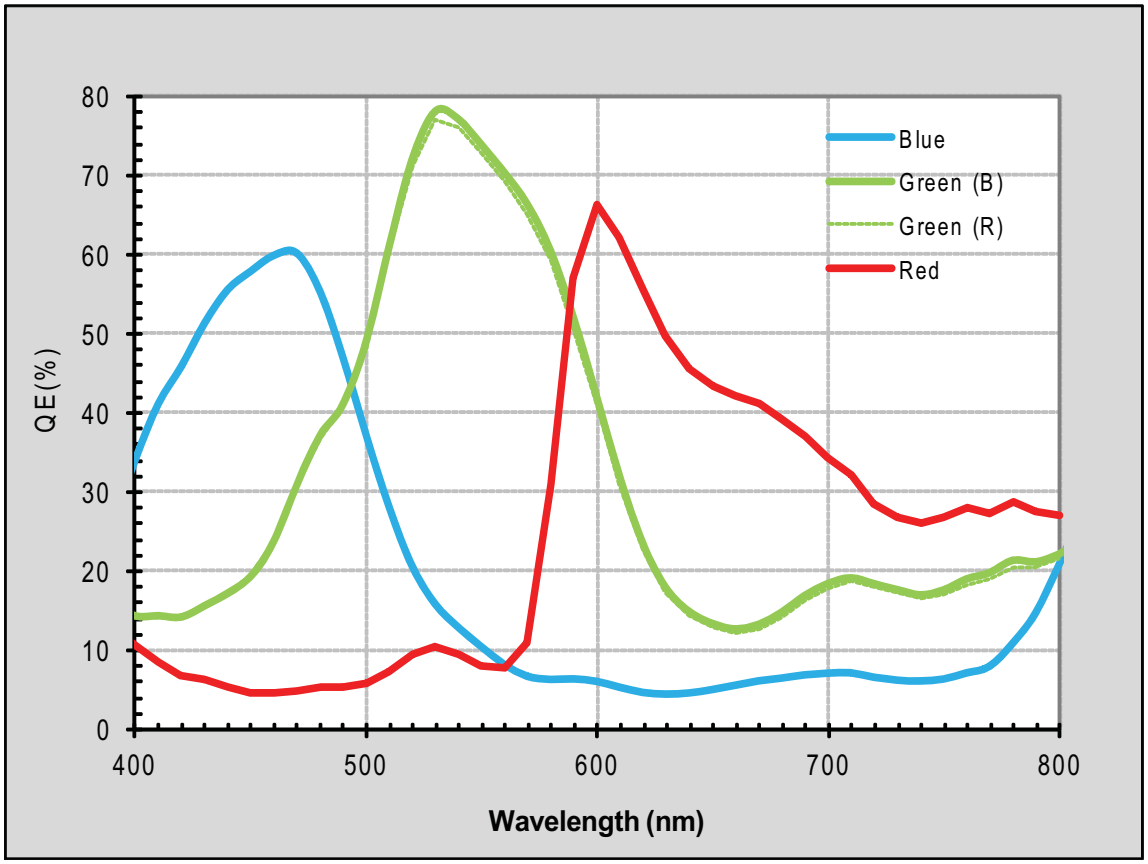
- Step1): Power up sensor.
- Step2): Power on the Temperature sensor by asserting (0x3EDE[14] =1 and set R0x30B4[0] = 1
- Step3): Enable Temperature start conversion, set R0x30B4[4] = 1
- Step4): Read Reg0x30B2 for code from temperature sensor.
- Step5): The temperature in degree Celsius = (dec(R0x30B2) - 331.92) / 1.2261

Example:

Following the procedure above, at Step 5 if R0x30B2 = 0x175(= 371 dec); then the readout temperature is (371-331.92)/1.2261 = 31.8 in degree Celsius.

Spectral Characteristics

Figure 38: Quantum Efficiency



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

AR1820HS CRA Characteristics

Table 12: 11.4 Degree CRA

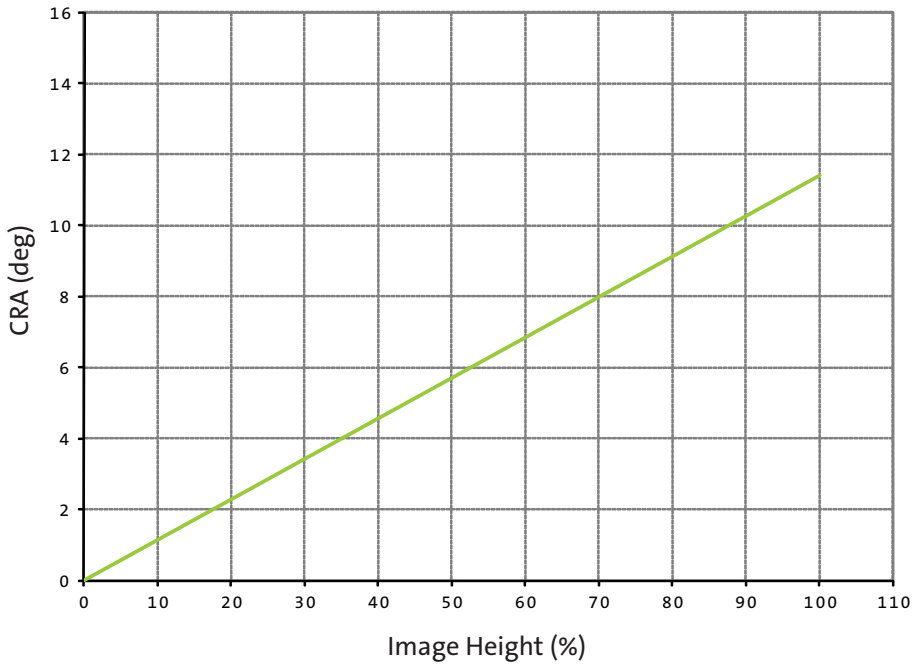


Image Height		CRA (deg)
(%)	(mm)	
0	0	0.00
5	0.192	0.57
10	0.384	1.14
15	0.576	1.71
20	0.768	2.28
25	0.959	2.85
30	1.151	3.42
35	1.343	3.99
40	1.535	4.56
45	1.727	5.13
50	1.919	5.70
55	2.111	6.27
60	2.303	6.84
65	2.494	7.41
70	2.686	7.98
75	2.878	8.55
80	3.070	9.12
85	3.262	9.69
90	3.454	10.26
95	3.646	10.83
100	3.838	11.40

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 13: 31 Degree CRA

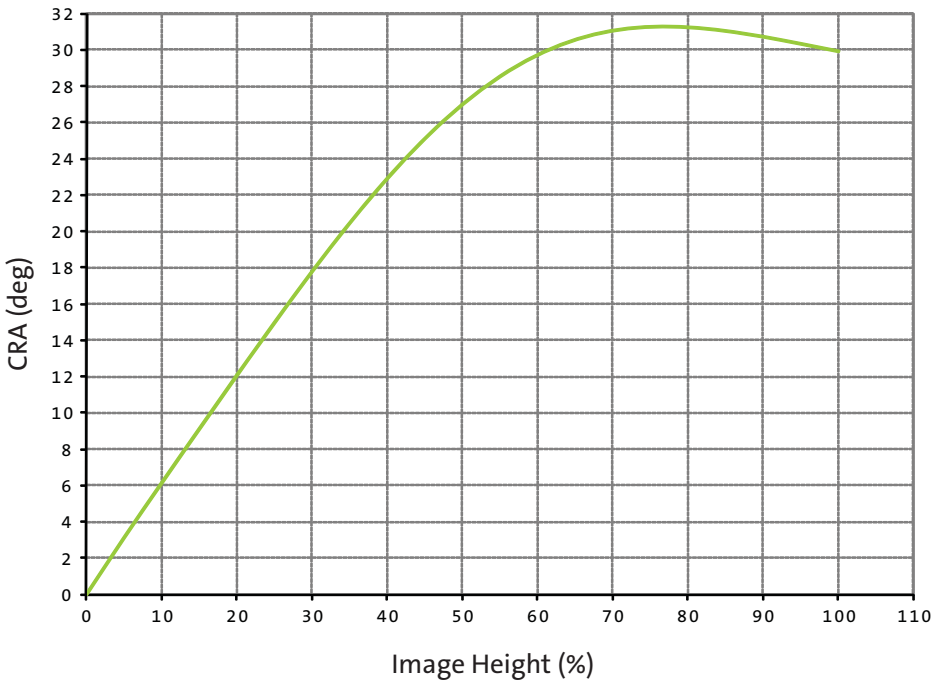
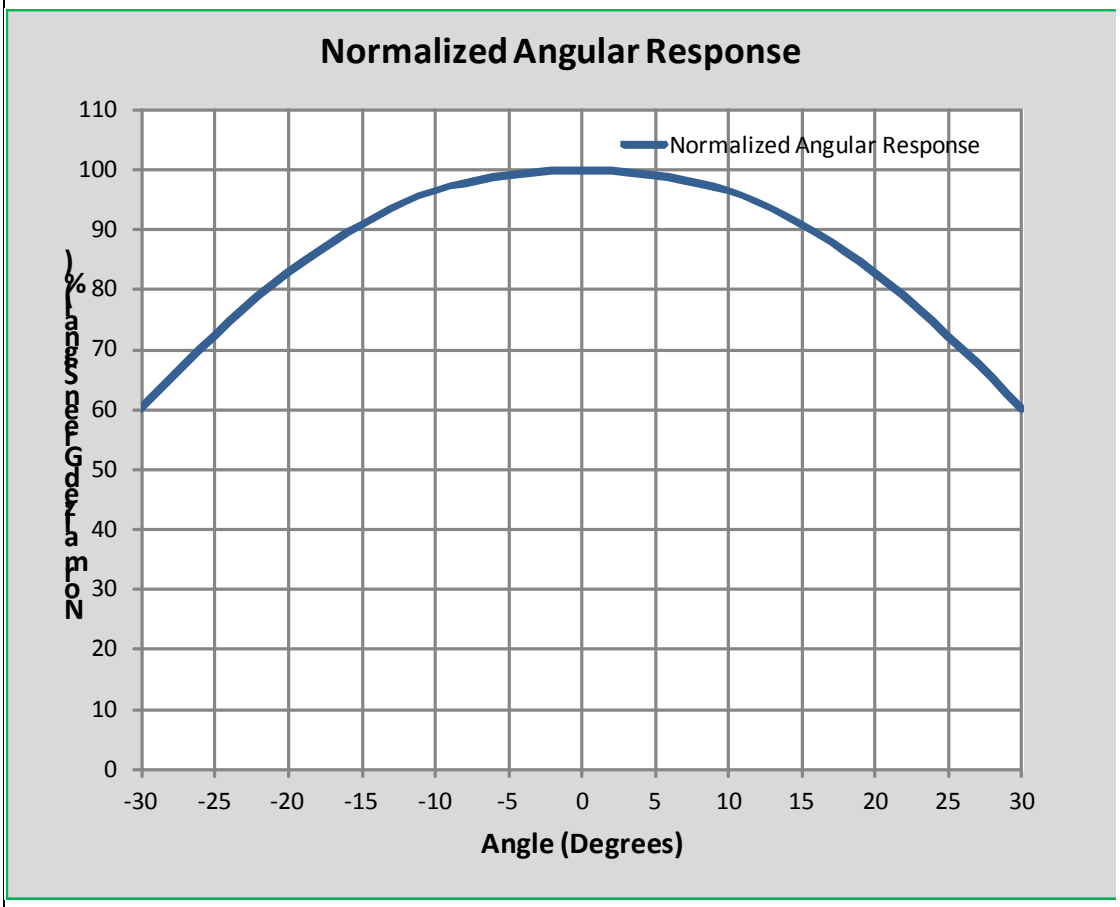


Image Height		CRA (deg)
(%)	(mm)	
0	0	0
5	0.192	3.13
10	0.384	6.14
15	0.576	9.12
20	0.768	12.07
25	0.959	14.97
30	1.151	17.78
35	1.343	20.45
40	1.535	22.91
45	1.727	25.11
50	1.919	26.99
55	2.111	28.53
60	2.303	29.72
65	2.494	30.55
70	2.686	31.05
75	2.878	31.26
80	3.070	31.24
85	3.262	31.03
90	3.454	30.71
95	3.646	30.33
100	3.838	29.92

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 14: Normalized Angular Response

Plot	Angle	Normalized Angular Response
	-30	60.17
	-29	62.63
	-28	65.13
	-27	67.56
	-26	69.97
	-25	72.27
	-24	74.55
	-23	76.75
	-22	78.84
	-21	80.82
	-20	82.71
	-19	84.54
	-18	86.21
	-17	87.87
	-16	89.41
	-15	90.81
	-14	92.16
	-13	93.38
	-12	94.51
	-11	95.50
	-10	96.39
	-9	97.11
	-8	97.75
	-7	98.32
	-6	98.77
	-5	99.16
	-4	99.45
	-3	99.69
	-2	99.86
	-1	99.92
	0	100.00
	1	99.92
	2	99.86
	3	99.69
	4	99.45
	5	99.16
	6	98.77
	7	98.32
	8	97.75
	9	97.11
	10	96.39
	11	95.50
	12	94.51
	13	93.38

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 14: Normalized Angular Response (continued)

Plot	Angle	Normalized Angular Response
	14	92.16
	15	90.81
	16	89.41
	17	87.87
	18	86.21
	19	84.54
	20	82.71
	21	80.82
	22	78.84
	23	76.75
	24	74.55
	25	72.27
	26	69.97
	27	67.56
	28	65.13
	29	62.63
	30	60.17

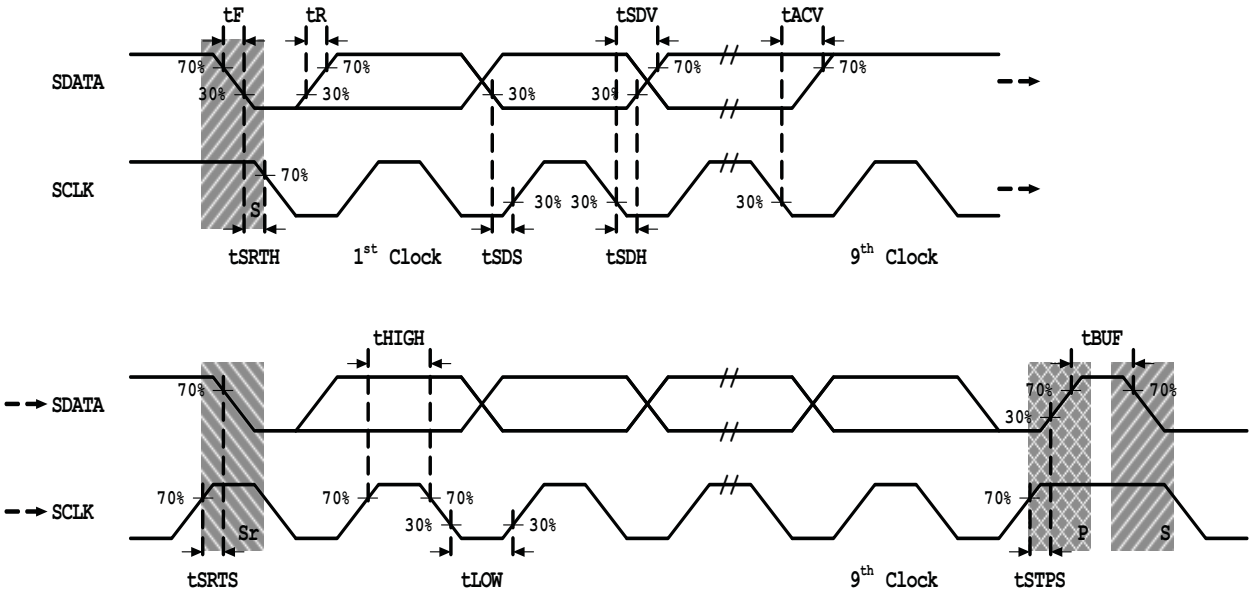
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Electrical Characteristics

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 55 and Table 28. Table 29 on page 86 shows the timing specification for the two-wire serial interface.

Figure 39: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 15: Two-Wire Serial Register Interface Electrical Characteristics

^{f}EXTCLK = 25 MHz; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_IO} = 1.8V; V_{DD} (digital core) = 1.2V; V_{DD_PLL} = 1.2V; V_{DD_TX} = 1.8V; Output load = 68.5pF; T_J = 55°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input LOW voltage		-0.5	–	0.3 x V_{DD_IO}	V
V_{IH}	Input HIGH voltage		0.7 x V_{DD_IO}	–	V_{DD_IO} + 0.5	V
I_{IN}	Input leakage current	No pull up resistor; V_{IN} = V_{DD_IO} or D_{GND}	10	–	14	µA
V_{OL}	Output LOW voltage	At specified 2mA	0.11	–	0.3	V
I_{OL}	Output LOW current	At specified V_{OL} 0.1V	–	–	6	mA
C_{IN}	Input pad capacitance		–	–	6	pF
C_{LOAD}	Load capacitance		–	–	N/A	pF

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 16: Two-Wire Serial Interface Timing Specifications
VDD = 1.7-1.9V; VAA = 2.4 -3.1V; Environment temperature = -30°C to 50°C

Symbol	Definition	Min	Max	Unit
f_{SCLK}	SCLK Frequency	0	400	KHz
t_{HIGH}	SCLK High Period	0.6	–	µs
t_{LOW}	SCLK Low Period	1.3	–	µs
t_{SRTS}	START Setup Time	0.6	–	µs
t_{SRTH}	START Hold Time	0.6	–	µs
t_{SDS}	Data Setup Time	100	–	ns
t_{SDH}	Data Hold Time	0	Note	µs
t_{SDV}	Data Valid Time	–	0.9	µs
t_{ACV}	Data Valid Acknowledge Time	–	0.9	µs
t_{STPS}	STOP Setup Time	0.6	–	µs
t_{BUF}	Bus Free Time between STOP and START	1.3	–	µs
tr	SCLK and SDATA Rise Time	–	300	ns
tf	SCLK and SDATA Fall Time	–	300	ns

EXTCLK

The electrical characteristics of the EXTCLK input are shown in Table 30. The EXTCLK input supports an AC-coupled sine-wave input clock or a DC-coupled square-wave input clock.

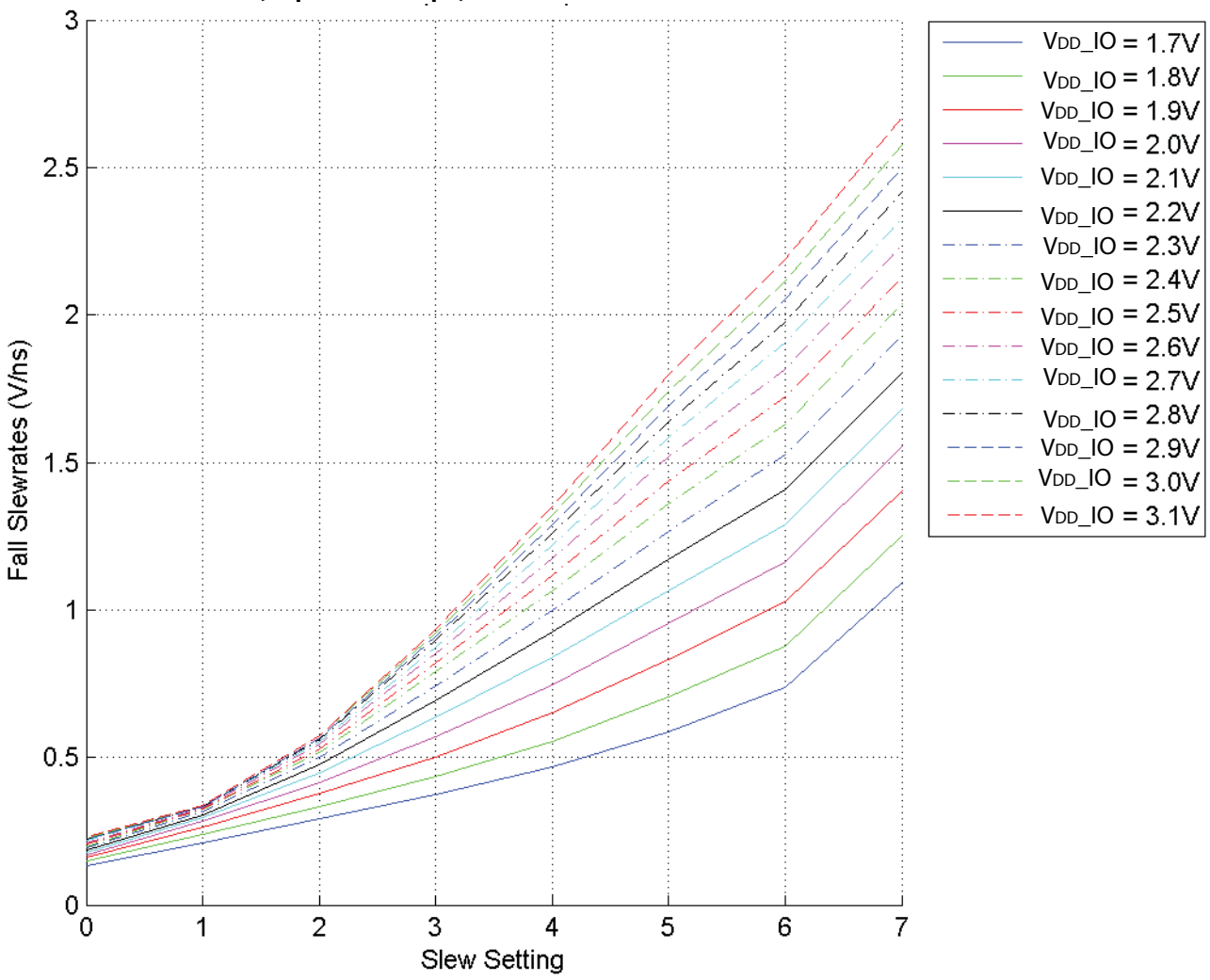
If EXTCLK is AC-coupled to the AR1820HS and the clock is stopped, the EXTCLK input to the AR1820HS must be driven to ground or to VDD_IO. Failure to do this will result in excessive current consumption within the EXTCLK input receiver.

Table 17: Electrical Characteristics (EXTCLK)
f_{EXTCLK} = 25 MHz; VAA = 2.8V; VAA_PIX = 2.8V; VDD_IO = 1.8V; DVDD_1V2 = 1.2V;
Output load = 68.5pF; TJ = 55°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL enabled	6	25	54	MHz
t_R	Input clock rise slew rate	CLOAD<20pF	–	2.883	–	ns
t_F	Input clock fall slew rate	CLOAD<20pF	–	2.687	–	ns
VIN_AC	Input clock minimum voltage swing (AC coupled)	–	0.5	–	–	V (p-p)
VIN_DC	Input clock maximum voltage swing (DC coupled)	–	–	–	VDD_IO + 0.5	V
$f_{CLKMAX(AC)}$	Input clock signaling frequency (low amplitude)	VIN = VIN_AC (MIN)	–	–	25	MHz
$f_{CLKMAX(DC)}$	Input clock signaling frequency (full amplitude)	VIN = VDD_IO	–	–	48	MHz
	Clock duty cycle	–	45	50	55	%
t_{JITTER}	Input clock jitter	cycle-to-cycle	–	545	600	ps
t_{LOCK}	PLL VCO lock time	–	–	0.2	2	ms
CIN	Input pad capacitance	–	–	6	–	pF
IIH	Input HIGH leakage current	–	0	–	10	µA
VIH	Input HIGH voltage	–	0.3 x VDD_IO	–	VDD_IO + 0.5	V
VIL	Input LOW voltage	–	-0.5	–	0.3 x VDD_IO	V

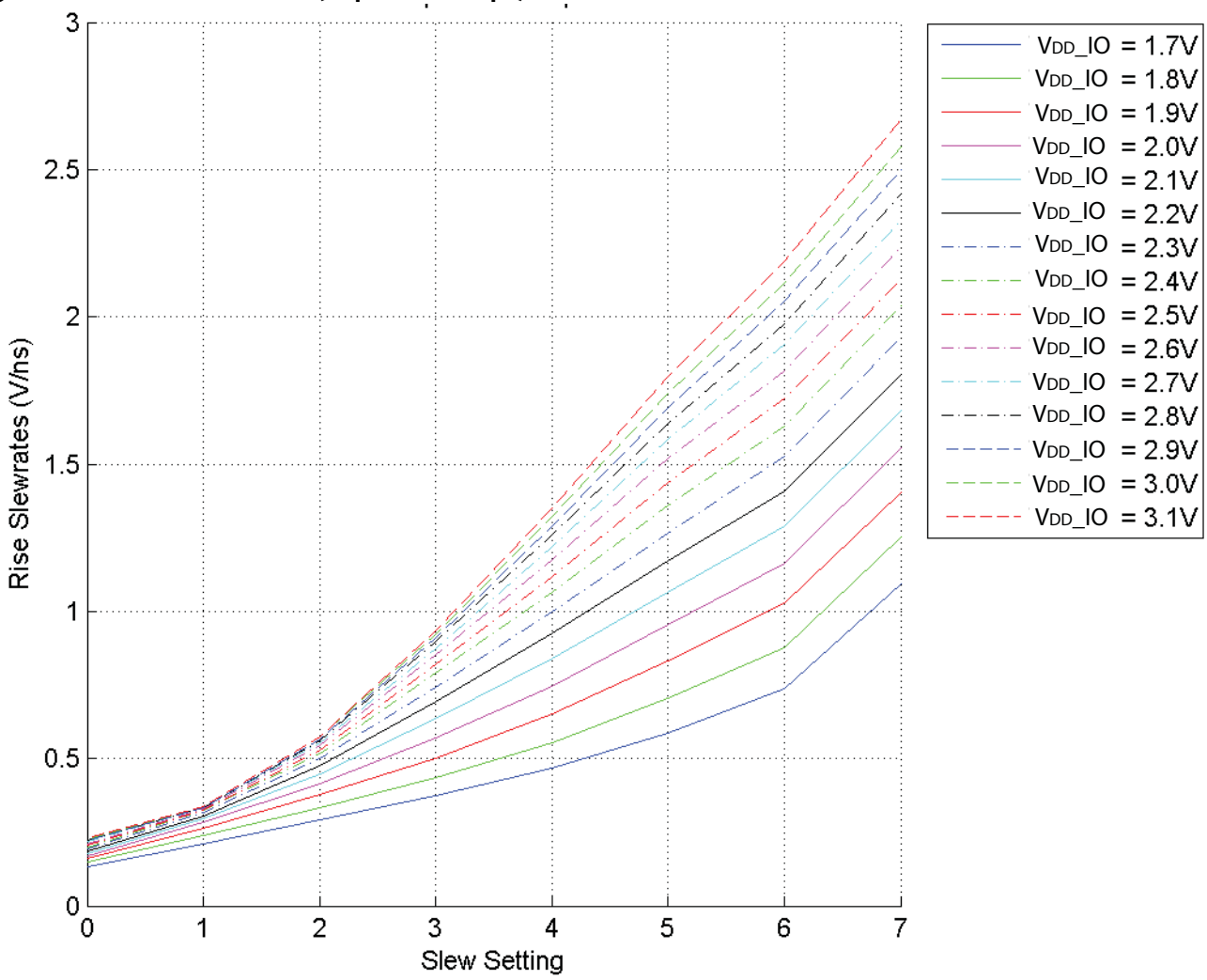
Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 40: Fall Slew Rates (Cap Load = 25pF)



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 41: Rise Slew Rates (Cap Load = 25pF)



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Serial Pixel Data Interface

HiSPi Serial Pixel Data Interface

The electrical characteristics of the HiSPi serial pixel data interface (CLK_P, CLK_N, DATA[4:1]_P, and DATA[4:1]_N) are shown in Table 31.

Table 18: Electrical Characteristics (Serial HiSPi Pixel Data Interface)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	High speed transmit differential voltage	140		270	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential-1 or Differential-0		<10		mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch		<14		%
^tR	Rise time (20–80%)	150		321	ps
^tF	Fall time (20–80%)	150		321	ps
V_{OL}	LP Output LOW level		<50		mV
V_{OH}	LP Output HIGH level	1.14		1.3	V
Z_{OLP}	Output impedance of low power parameter	110			Ω
T_{RLP}	15–85% rise time			25	ns
T_{FLP}	15–85% fall time			25	ns
Δv/Δdtsr	Slew rate (C_{LOAD} = 20–70pF)	30			mV/ns
CLKskew	PHY1-Clock to PHY2-Clock skew		<600		ps

MIPI Serial Pixel Data Interface

The electrical characteristics of the MIPI serial pixel data interface are shown in Table 32.

Table 19: Electrical Characteristics (Serial MIPI Pixel Data Interface)

Symbol	Parameter	Min	Typ	Max	Unit
MIPI High Speed (HS)					
VOD	|VOD| HS transmit differential voltage	188.5		217.35	mV
VCMTX	VCMTX HS transmit static common mode voltage	192.89		236.65	mV
ΔVOD	|ΔVOD| HS VOD mismatch	≤9.2			mV
ΔVCMTX	|ΔVCMTX(1,0)| VCMTX mismatch	≤3.55			mV
ZOS	ZOS Single ended output impedance	47.5		59.6	Ω
ΔZOS	ΔZOS Single ended output impedance mismatch			< 4.31	%
t_R and t_F	t_R and t_F 20%-80% rise time and fall time (@400Mbps)	0.16		0.224	UI
	t_R and t_F 20%-80% rise time and fall time (@533Mbps)	0.206		0.279	UI
	t_R and t_F 20%-80% rise time and fall time (@800Mbps)	0.284		0.341	UI
Skew	Data to Clock Skew	-0.075		0.155	UI
MIPI Low Power (LP)					
V_{OL}	V_{OL} output low level	0.347		4.64	mV
V_{OH}	V_{OH} output high level	1.0716		1.284	V
Z_{OLP}	Z_{OLP} Output impedance of LP	142.7		168.84	ohms
t_{RLP}/t_{FLP}	t_{RLP}/t_{FLP} 15%-85% rise time and fall	2.549		11.622	ns
Slew rate	Max Slew rate, (CLOAD = 70pF)	31.67		112.14	mV/ns
	Min Fall Slew Rate	31.67		99.65	mV/ns

Note: Measured with package part on Aptina Standard Serial I/O test Board.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Control Interface

The electrical characteristics of the control interface (RESET_BAR, TEST, GPIO0, GPIO1, GPI2, and GPI3) are shown in Table 33.

Table 20: DC Electrical Characteristics (Control Interface)
f_{EXTCLK} = 25 MHz; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_IO} = 1.8V; DV_{DD_1V2} = 1.2V;
Output load = 68.5pF; T_J = 55°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage	Preliminary	0.7 x V_{DD_IO}	–	V_{DD_IO} + 0.5	V
V_{IL}	Input LOW voltage	Preliminary	–0.5	–	V_{DD_IO} x 0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	–	–	10	µA
C_{IN}	Input pad capacitance	Preliminary	–	6	–	pF

Operating Voltages

V_{AA} and V_{AA_PIX} must be at the same potential for correct operation of the AR1820HS.

Table 21: DC Electrical Definitions and Characteristics
f_{EXTCLK} = 25 MHz; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_IO} = 1.8V; V_{DD_1V2} = 1.2V;
Output load = 68.5pF; T_J = 60°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{AA}	Analog voltage		2.7	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.7	2.8	3.1	V
V_{DD}	Digital, HiSPi core, and PLL voltage		1.14	1.2	1.3	V
V_{DD_1V8}	OTPMY digital voltage		1.7	1.8	1.9	V
V_{DD_IO}	I/O digital voltage		1.7	1.8	1.9	V
			2.7	2.8	3.1	V
V_{DD_TX}	MIPI transmitter supply voltage	Internal regulator disabled	1.14	1.2	1.3	V
	HiSPi transmitter supply voltage	Internal regulator enabled	1.14	1.2	1.3	V
	HiSPi transmitter supply voltage	Internal regulator disabled	0.35	0.4	0.45	V
H/W Standby Current Consumption			–	–	30	µA
Output Driving Strength			10	–	–	mA
Slew Rate			–	0.7	–	µV/sec
V_{AA}	Analog core current			65	–	mA
V_{DD}	Digital core current			194	–	mA
V_{DD_1V8}	OTPM core current			1.15	–	mA
V_{DD_TX}	HiSPi transmitter current			29	–	mA
V_{DD_IO}	IO and HiSPi IO current			1.9	–	mA
V_{AA_PIX}	Pixel supply current			6	–	mA

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Operating Current

Table 22: Typical Operating Current Consumption (MIPI)
f_{EXTCLK} = 25 MHz; VAA = 2.8V; VAA_PIX = 2.8V; VDD_IO = 1.8V; VDD_1V2 = 1.2V; Ta = 25°C

Symbol	Standard Voltage	Parameter	Condition	Typical Mean	Max. Peak	Unit
I_{AA} +I_{AA_PIX}	2.8V	Analog and Pixel supply	Full Resolution 18Mpix	87.83	169	mA
			1080p60 + 20%EIS 3.5Mpix	87.88	130	mA
			QuadHD 30 8Mpix	84.16	122	mA
			Ultra-Fast HD 1080p120	97.61	154	mA
I_{DD}	1.2V	Digital, PHY Core, and PLL supply current	Full Resolution 18Mp	152.72	268	mA
			1080p60 + 20%EIS 3.5Mpix	148.78	236	mA
			8M QuadHD	153.43	224	mA
			Ultra-Fast HD 1080p120	156.06	227	mA
I_{TX}	1.2V	Serial Transmitter supply current	Full Resolution 18Mp	11.34	17	mA
			1080p60 + 20%EIS 3.5Mpix	10.78	21	mA
			8M QuadHD	11.41	14	mA
			Ultra-Fast HD 1080p120	8.63	26	mA
I_{DD_IO}+I_{DD_IV8}	1.8V	IO Digital and OTPM digital	Full Resolution 18Mp	0.726	2	mA
			1080p60 + 20%EIS 3.5Mpix	0.726	2	mA
			8M QuadHD	0.726	2	mA
			Ultra-Fast HD 1080p120	0.726	2	mA

Notes:
1. AR1820 utilizes a dynamic power-saving technique to reduce the power consumption. Some circuits are dynamically turned off when they are not used during vertical blanking time.
2. The maximum peak value indicates the peak current which is measured at active time in the worst case scenario (fewest number of die and highest power consumption). The customer ‘s power supply needs to be able to support this scenario.
3. The typical mean indicates the mean current which measured as an average of active and blanking time,

Absolute Maximum Ratings

Caution **Stresses greater than those listed in Table 36 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Table 23: Absolute Max Voltages

Symbol	Parameter	Condition	Min	Max	Unit
V_{DD}	Digital, PHY core, and PLL voltage		-0.3	1.5	V
V_{DD_1V8}	OTPM		-0.3	2.1	V
V_{DD_IO}	IO/PHY IO voltage		-0.3	3.5	V
V_{AA}	Analog voltage		-0.3	3.5	V
V_{AA_PIX}	Pixel supply voltage		-0.3	3.5	V
V_{DD_TX}	Serial interface supply		-0.3	1.5	V

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Data Compression

The compression block supports A-law compression. A-law compression is used with HiSPi only. In the AR1820HS, the following configurations are supported:

- 10/8/10, 12/10/12, 12/8/12 A-law compression with HiSPi.

Table 24: 12-10-12 A-law Binary Encoding Table
(X – don't care)

Input Range	Input Values												Compressed Code Word									
	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
0 to 127	0	0	0	0	0	a	b	c	d	e	f	g	0	0	0	a	b	c	d	e	f	g
128 to 255	0	0	0	0	1	a	b	c	d	e	f	g	0	0	1	a	b	c	d	e	f	g
256 to 511	0	0	0	1	a	b	c	d	e	f	g	X	0	1	0	a	b	c	d	e	f	g
512 to 1023	0	0	1	a	b	c	d	e	f	g	X	X	0	1	1	a	b	c	d	e	f	g
1024 to 2047	0	1	a	b	c	d	e	f	g	h	X	X	1	0	a	b	c	d	e	f	g	h
2048 to 4095	1	a	b	c	d	e	f	g	h	X	X	X	1	1	a	b	c	d	e	f	g	h

Table 25: 12-10-12 A-law Binary Decoding Table
(X – don't care)

Code Word										Decoded Values												Max. Error
9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	a	b	c	d	e	f	g	0	0	0	0	0	a	b	c	d	e	f	g	0
0	0	1	a	b	c	d	e	f	g	0	0	0	0	1	a	b	c	d	e	f	g	0
0	1	0	a	b	c	d	e	f	g	0	0	0	1	a	b	c	d	e	f	g	1	1
0	1	1	a	b	c	d	e	f	g	0	0	1	a	b	c	d	e	f	g	1	0	2
1	0	a	b	c	d	e	f	g	h	0	1	a	b	c	d	e	f	g	h	1	0	3
1	1	a	b	c	d	e	f	g	h	1	a	b	c	d	e	f	g	h	1	0	0	4

Table 26: 12-8-12 A-law Binary Encoding Table

Input Range	Input Values												Compressed Code Word							
	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0 to 31	0	0	0	0	0	0	0	a	b	c	d	e	0	0	0	a	b	c	d	e
32 to63	0	0	0	0	0	0	1	a	b	c	d	e	0	0	1	a	b	c	d	e
64 to 127	0	0	0	0	0	1	a	b	c	d	e	X	0	1	0	a	b	c	d	e
128 to 255	0	0	0	0	1	b	b	c	d	e	X	X	0	1	1	a	b	c	d	e
256 to 511	0	0	0	1	a	c	c	d	e	X	X	X	1	0	0	a	b	c	d	e
512 to 1023	0	0	1	a	b	d	d	e	X	X	X	X	1	0	1	a	b	c	d	e
1024 to 2047	0	1	a	b	c	d	e	X	X	X	X	X	1	1	0	a	b	c	d	e
2048 to 4095	1	a	b	c	d	e	X	X	X	X	X	X	1	1	1	a	b	c	d	e

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Table 27: 12-8-12 A-law Binary Decoding Table

Code Word								Decoded Values												Max. Error
7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	a	b	c	d	e	0	0	0	0	0	0	0	a	b	c	d	e	0
0	0	1	a	b	c	d	e	0	0	0	0	0	0	1	a	b	c	d	e	0
0	1	0	a	b	c	d	e	0	0	0	0	0	1	a	b	c	d	e	1	1
0	1	1	a	b	c	d	e	0	0	0	0	1	a	b	c	d	e	1	0	2
1	0	0	a	b	c	d	e	0	0	0	1	a	b	c	d	e	1	0	0	4
1	01	c	a	b	c	d	e	0	0	1	a	b	c	d	e	1	0	0	0	8
1	1	0	a	b	c	d	e	0	1	a	b	c	d	e	1	0	0	0	0	16
1	1	1	a	b	c	d	e	1	a	b	c	d	e	1	0	0	0	0	0	32

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Registers

The following registers are related to compression:

Address (Base+)	Mnemonic	Register	
0x0112	ccp_data_format	RW	[3:0]: The bit-width of the compressed pixel data [11:8]: The bit-width of the uncompressed data
0x31AE	serial format	RW	[9:8]: serial interface type 2: MIPI 3: HiSPi [2:0]: serial data lanes

The compression block gets the following control signals ccp_data_format and serial_-format registers

- MIPI: indicates MIPI interface
- HiSPi: indicates HiSPi interface

The output type by compression control signals is shown in Table 41.

Table 28: Output Type by Compression Control Signals

Mode	Comp_10_8	Comp_10_6	Output
MIPI=0 HiSPi=0	X	X	Bypass
MIPI=1, HiSPi=1	X	X	Invalid
MIPI=1, HiSPi=0	0	0	Bypass
	0	1	10_6 dpcm
	1	0	10_8 dpcm
	1	1	Invalid
HiSPi=1, MIPI=0	0	0	Bypass
	0	1	Bypass
	1	0	10_8 a-law
	1	1	10_8 a-law

Example

A-law 10to8

Set 0x0112=0x0a08; // 10 to 8 compression

Set 0x31AE=0x030X; // HiSPi; [2:0] is serial data lanes.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Output Data Format

Pixel Data Interface

The AR1820HS reads data out of the pixel array in a progressive scan over a High Speed serial data interface, or parallel data interface. RAW8, RAW10, and RAW12 image data formats are supported.

Figure 42: Data Formats

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RAW12
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	RAW10
D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	RAW8

High Speed Serial Pixel Data Interface

The High Speed Serial Pixel (HiSPi)^{TM} interface outputs serialized pixel data using eight data lanes and two clock lanes, each lane consisting of a pair of differential signals.

The HiSPi interface supports the following protocols: Streaming-S, Streaming-SP, and Packetized-SP. The streaming protocol conforms to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The packetized protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

HiSPi Streaming Mode Protocol Layer

The protocol layer is positioned between the output data path of the sensor and the physical layer. The main functions of the protocol layer are generating sync codes, formatting pixel data, inserting horizontal/vertical blanking codes, and distributing pixel data over defined data lanes.

The HiSPi interface can only be configured when the sensor is in standby. This includes configuring the interface to transmit across four or eight data lanes.

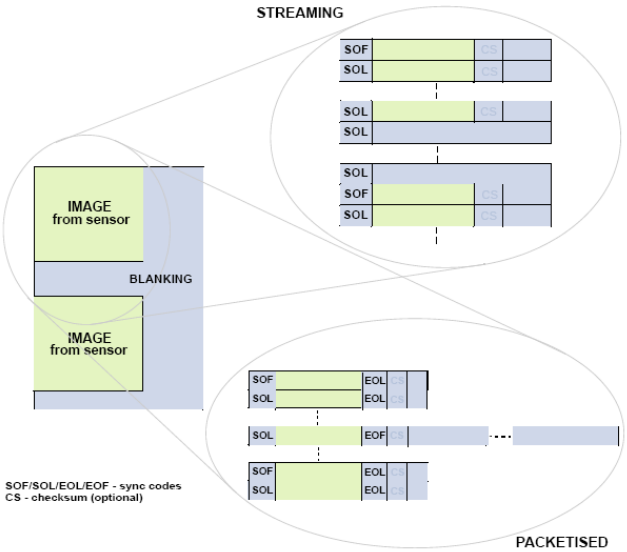
Protocol Fundamentals

Referring to Figure 59, it can be seen that a SYNC code is inserted in the serial data stream prior to each line of image data. The Streaming-S and Streaming-SP protocols will insert a SYNC code to transmit each active data line and vertical blanking lines.

The Packetized-SP protocol will transmit a SYNC code to note the start and end of each row. The packetized protocol uses sync a “Start of Frame” (SOF) sync code at the start of a frame and a “Start of Line” (SOL) sync code at the start of a line within the frame. The protocol will also transmit an “End of Frame” (EOF) at the end of a frame and an “End of Line” (EOL) sync code at the end of a row within the frame

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 43: Steaming-S/SP vs. Packetized-SP Transmission



Note: See the High-Speed Serial Pixel (HiSPi)™ Protocol Specification V1.50.00 for HiSPi details.

HiSPi Physical Layer

The HiSPi physical layer is partitioned into two blocks of four data lanes and an associated clock lane. Any reference to a PHY in the remainder of this document is referring to this minimum building block. For full details, see HiSPi Physical Layer Specification V3.00.00.

The HiSPi PHY uses a low voltage serial differential output. The HiSPi PHY drivers use a simple current steering driver scheme with two outputs that are complementary to each other (V_{OA} and V_{OB}). It is intended that these drivers be attached to short-length 100Ω differential interconnect to a receiver with a 100Ω termination. CL represents the total parasitic excess capacitance loading of the receiver and the interconnect.

The AR1820HS supports two electrical signaling modes:

- Scalable Low Voltage Serial (SLVS) which has low amplitude and common-mode voltage (VCM) but scalable using an external supply.
- Sub-SLVS, which has a smaller non-scalable amplitude and a higher common-mode voltage.

Comparison of SLVS and Sub-LVDS

Here is a high-level comparison of the differences between SLVS and Sub-SLVS.

Table 29: SLVS and Sub-LVDS Comparison

Parameter	Sub-LVDS	SLVS
Typical Differential Amplitude[1]	150mV	200mV
Typical Common Mode[1]	0.9V	200mV
Typical Power Consumption[2]	TBD	4mW

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

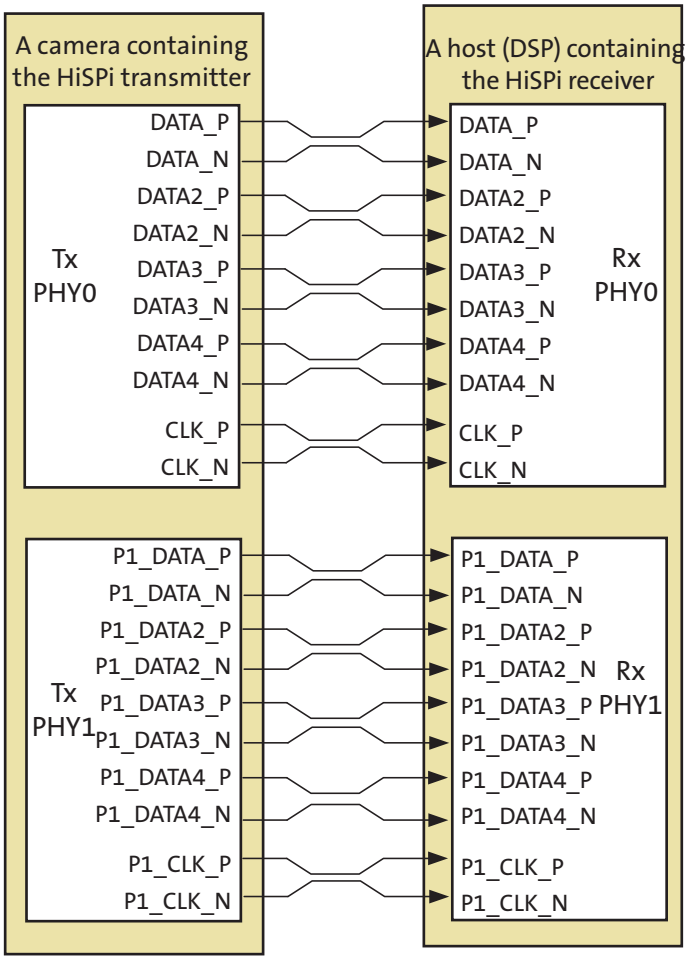
Table 29: SLVS and Sub-LVDS Comparison

Parameter	Sub-LVDS	SLVS
Compatibility with industry-standard receivers	SMIA CCP2	MIPI D-PHY

Notes:
1. These are nominal values
2. Power from load driving stage, digital/serializer logic (VDD_HiSPi) not included.

Each HiSPi PHY is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. The four Data lanes are 90 degrees out of phase with the Clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 60 shows the configuration between the HiSPi transmitter and the receiver.

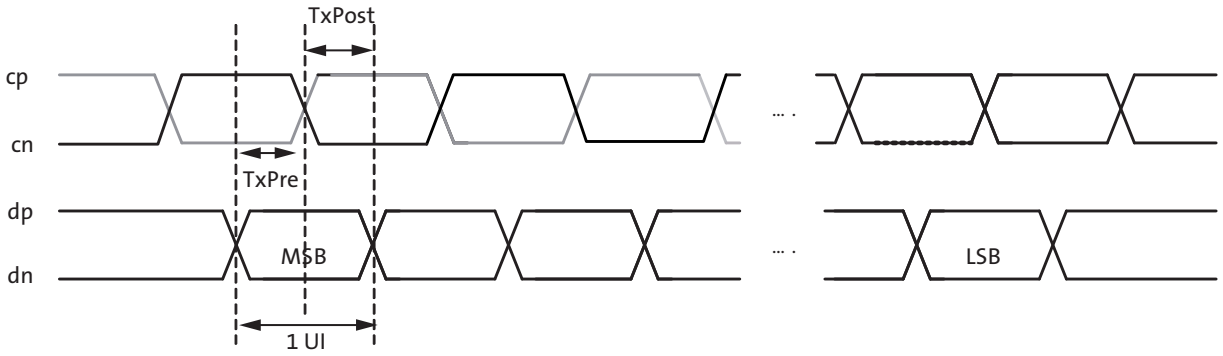
Figure 44: HiSPi Transmitter and Receiver Interface Block Diagram



The PHY will serialize an 8-, 10-, or 12-bit data word and transmit each bit of data centered on a rising edge of the clock, the second on the falling edge of clock. Figure 61 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 45: Timing Diagram

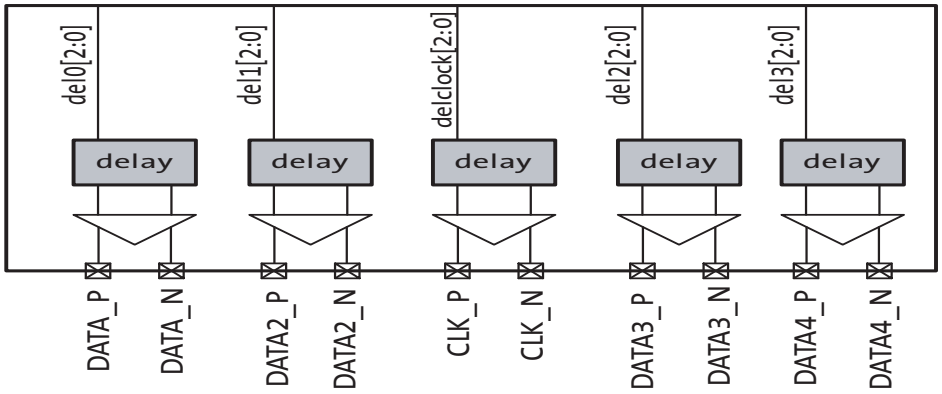


DLL Timing Adjustment

The HiSPi specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

Figure 46: Block Diagram of DLL Timing Adjustment



Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 47: Delaying the clock_lane with Respect to data_lane

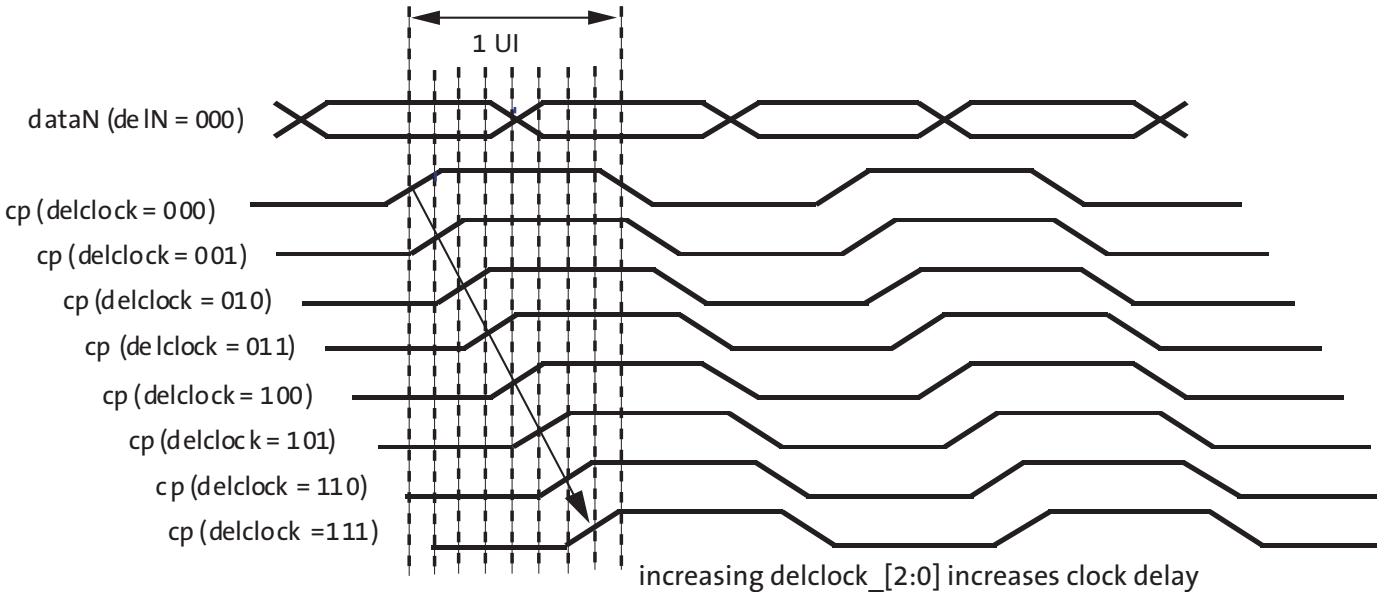
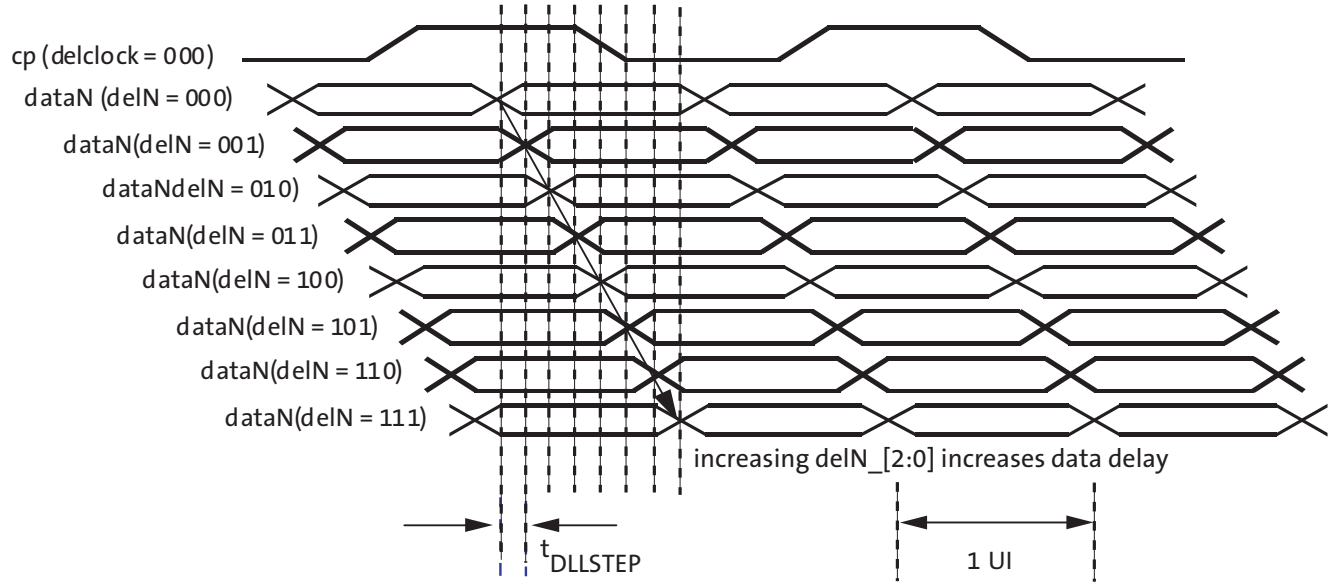


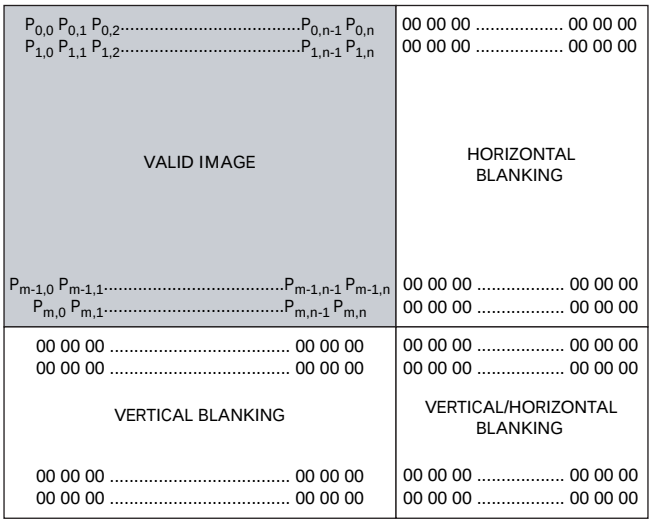
Figure 48: Delaying data_lane with Respect to the clock_lane



Note: See the High-Speed Serial Pixel (HiSPi)™ Physical Layer Specification V3.00.00 for details.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 49: Spatial Illustration of Image Readout



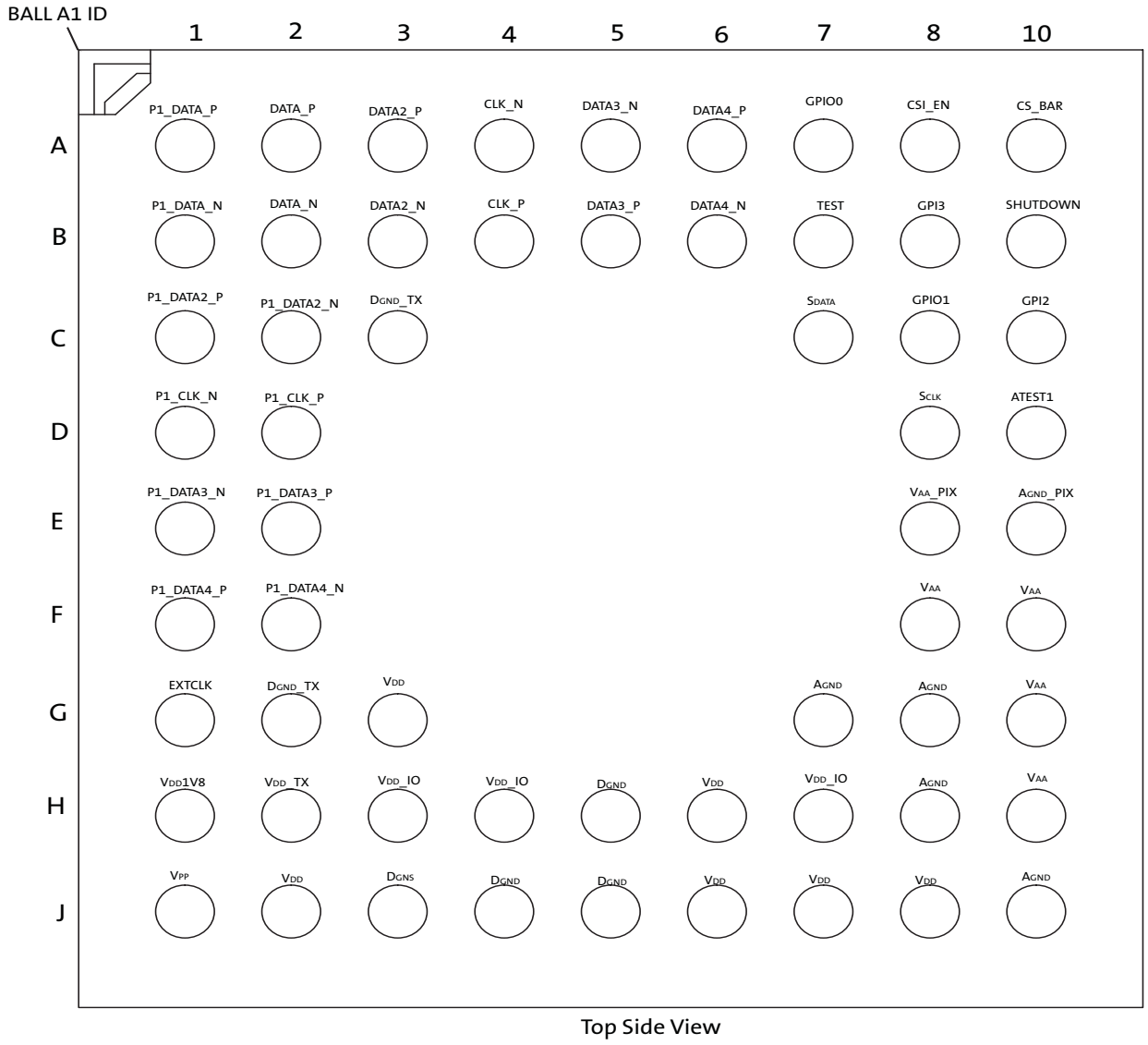
References

- High-Speed Serial Pixel (HiSPi) Interface Physical Layer Reference: HiSPi Physical Layer V 3.00.00_release pending
- High-Speed Serial Pixel (HiSPi) Interface Protocol: HiSPi Protocol V 1.50.00_B
- MIPI Alliance Standard for CSI-2 version 1.0
- MIPI Alliance Standard for D-PHY version 1.0

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Package Dimensions

Figure 50: iBGA Package Pinout



Top Side View

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

Figure 51: Package Diagram

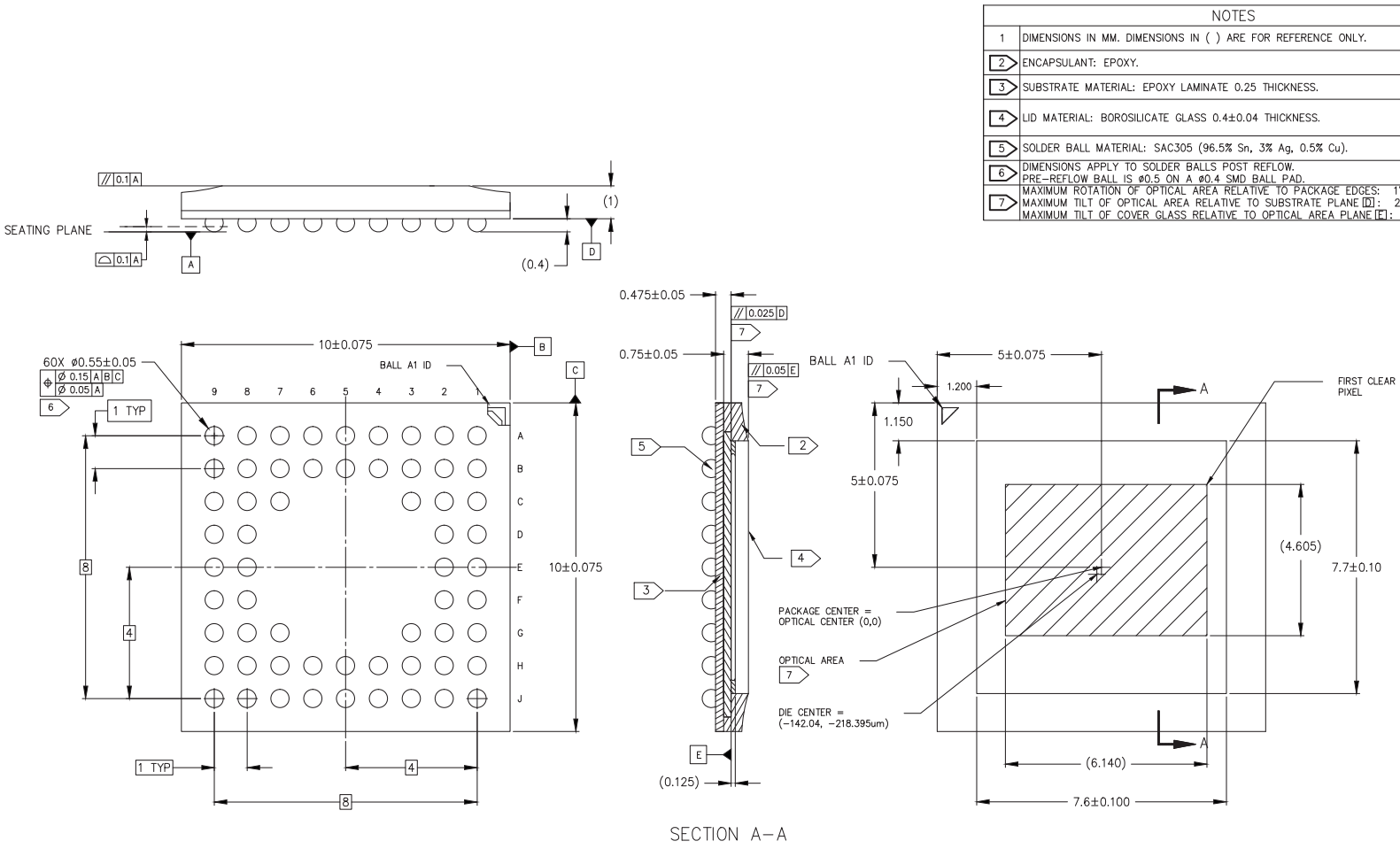


Table 30: iBGA Thermal Specifications (Simulation)

Package Type	Symbol	θ Value (°C/W)
iBGA	θ_{JB}	12.71
	$\theta_{JC\ bottom}$	8.06

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.

Revision History

Rev. D 10/21/13

- Updated Table 1, “Key Performance Parameters,” on page 1
- Updated Table 3, “HiSPi Modes of Operation and Power Consumption,” on page 2
- Updated Table 4, “MIPI Modes of Operation and Power Consumption,” on page 3
- Updated Table 7, “Usage Case for Power Rail and Internal Regulator,” on page 19
- Updated “One-Time Programmable Memory (OTPM)” on page 37
- Updated Table 21, “Total Gain Setting Summary for Native Mode,” on page 74
- Updated Table 22, “Total Gain Setting Summary for Subsampling,” on page 75
- Updated Table 23, “Summary Native Gain,” on page 78
- Updated Table 24, “Summary Subsampling Gain,” on page 78
- Updated Table 31, “Electrical Characteristics (Serial HiSPi Pixel Data Interface),” on page 89
- Updated Table 34, “DC Electrical Definitions and Characteristics,” on page 90
- Updated Table 35, “Typical Operating Current Consumption (MIPI),” on page 91

Rev. C 7/31/13

- Updated Table 1, “Key Performance Parameters,” on page 1
- Updated Table 6, “Independent Power and Ground Domains,” on page 18
- Added Table 7, “Usage Case for Power Rail and Internal Regulator,” on page 10
- Updated Table 21, “Total Gain Setting Summary for Native Mode,” on page 74
- Updated Table 23, “Summary Native Gain,” on page 78
- Updated Table 32, “Electrical Characteristics (Serial MIPI Pixel Data Interface),” on page 89

Rev. B 7/30/13

- Updated to Preliminary
- Updated “Features” on page 1
- Updated “Applications” on page 1
- Updated Table 1, “Key Performance Parameters,” on page 1
- Updated Table 2, “Available Part Numbers,” on page 2
- Replaced Table 3, “Modes of Operation and Power Consumption” with:
  - Table 3, “HiSPi Modes of Operation and Power Consumption,” on page 2
  - Table 4, “MIPI Modes of Operation and Power Consumption,” on page 3
- Updated “Functional Overview” on page 10
- Updated Figure 3: “Typical Application Circuit—HiSPi Connection,” on page 13
- Added Figure 4: “Typical Application Circuit—MIPI Connection,” on page 15
- Updated “Signal Descriptions” on page 17
- Updated Table 6, “Independent Power and Ground Domains,” on page 18
- Updated “Power On Sequence” on page 22
- Updated “Power Down Sequence” on page 23
- Updated “Power Down Sequence” on page 23
- Updated “Slave Address/Data Direction Byte” on page 27
- Updated Equation 11 on page 64
- Updated “Analog Gain” on page 73
- Updated Equation 14 on page 73
- Updated “Total Gain” on page 73
- Added Table 21, “Total Gain Setting Summary for Native Mode,” on page 74

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation. All rights reserved.

- Added Table 22, “Total Gain Setting Summary for Subsampling,” on page 75
- Added Table 23, “Summary Native Gain,” on page 78
- Added Table 24, “Summary Subsampling Gain,” on page 80
- Updated “Temperature Sensor” on page 80
- Added Table 25: “11.4 Degree CRA,” on page 81
- Added Table 26: “31 Degree CRA,” on page 82
- Updated “Serial Pixel Data Interface” on page 89
- Updated “Operating Voltages” on page 90
- Updated Table 34, “DC Electrical Definitions and Characteristics,” on page 90
- Updated Table 36, “Absolute Max Voltages,” on page 91
- Updated “References” on page 100

Rev. A, Advance 10/9/12

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com
Aptina, Aptina Imaging, A-PixHS, HiSPi, and the Aptina logo are the property of Aptina Imaging Corporation
All other trademarks are the property of their respective owners.
Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

Aptina reserves the right to change products or specifications without notice.
©2012 Aptina Imaging Corporation All rights reserved.