1/6-Inch 1080P High-Definition (HD) System-On-A-Chip (SOC) Digital Image Sensor Die

AS0260 Die Data Sheet

For the product data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Superior low-light performance
- Ultra-low-power
- 1080p Full HD video at 30 fps
- Internal master clock generated by on-chip phase-locked loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, JPEG, MJPEG, 565RGB, 555RGB, 444RGB, processed Bayer, BT656, RAW8-, RAW8+2-bit, and M420
- Parallel and 1- or 2-lane MIPI data output
- Independently configurable gamma correction
- Lens shading correction
- UVC interface support
- Perspective correction
- Multi-camera synchronization

General Physical Specifications

- Die thickness: 200 µm ±12 µm
  (Consult factory for other die thickness)
- Back side die surface of polished bare silicon
- Typical metal 1 thickness: 1.8 kÅ
- Typical metal 2 thickness: 1.8 kÅ
- Typical metal 3 thickness: 1.8 kÅ
- Typical metal 4 thickness: 6.2 kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.1 kÅ nitride over 5.5 kÅ of undoped oxide
- Passivation openings (MIN): 75 µm x 90 µm

Die Database

- Die outline, see Figure 2 on page 9
- Singulated die size (nominal dimension):
  6024 µm ±25 µm x 4184 µm ±25 µm
- "Bond Pad Location and Identification Tables", see page 6–8

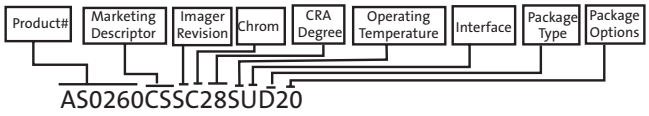
Order Information

Part Number	Description
AS0260CSSC28SUD20	Standard product
AS0260HQSC28SUD20	With Face Detect feature

Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

Options

- Form
  – Die D
- Testing
  – Standard (level 1) probe C1



Key Performance Parameters

- Optical format: 1/6-inch (16:9)
- Active imager size: 2.69 mm(H) x 1.51 mm(V), 3.08 mm diagonal
- Active pixels: 1920 H x 1080 V (2.0Mp)
- Pixel size:1.4 µm x 1.4 µm
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Maximum data rate/master clock: 48 MPS/96 MHz
- Maximum MIPI data rate: 768 Mb/s
- Frame rate: 1080p (1920H x 1080V) 30fps
- ADC resolution: 10-bit, on die
- Responsivity: 0.64 V/lux-sec (550 nm)
- Pixel dynamic range: 65 dB
- SNR MAX: 33 dB
- Supply voltage:
  – I/O digital: 1.8 V or 2.8 V
  – Digital: 1.8 V
  – Analog: 2.8 V
  – MIPI voltage:1.8V
- Typical power consumption: 296 mW
- Operating temperature: –30°C to +70°C
- Chief ray angle (CRA): 28°

General Description

Aptina's AS0260 is a 1/6-inch 2.0Mp CMOS digital image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), MIPI and parallel output ports (only one output port can be used). The microcontroller manages all functions of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1920 x 1080 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and a 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has superior low-light performance that is particularly suitable for PC camera applications. The AS0260 features Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The Aptina® AS0260 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p image size at 30 frames per second (fps). It outputs JPEG compressed 8-bit data, using the parallel output port.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test. Wafer probe is performed at an elevated temperature to test product functionality in Aptina's standard package. Because the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die A/D converter, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The AS0260 imager die has 58 bond pads. Refer to Table 1 on page 5 and Table 2 on page 7or a complete list of bond pads and coordinates.

The AS0260 imager die does not require the user to determine bond option features.

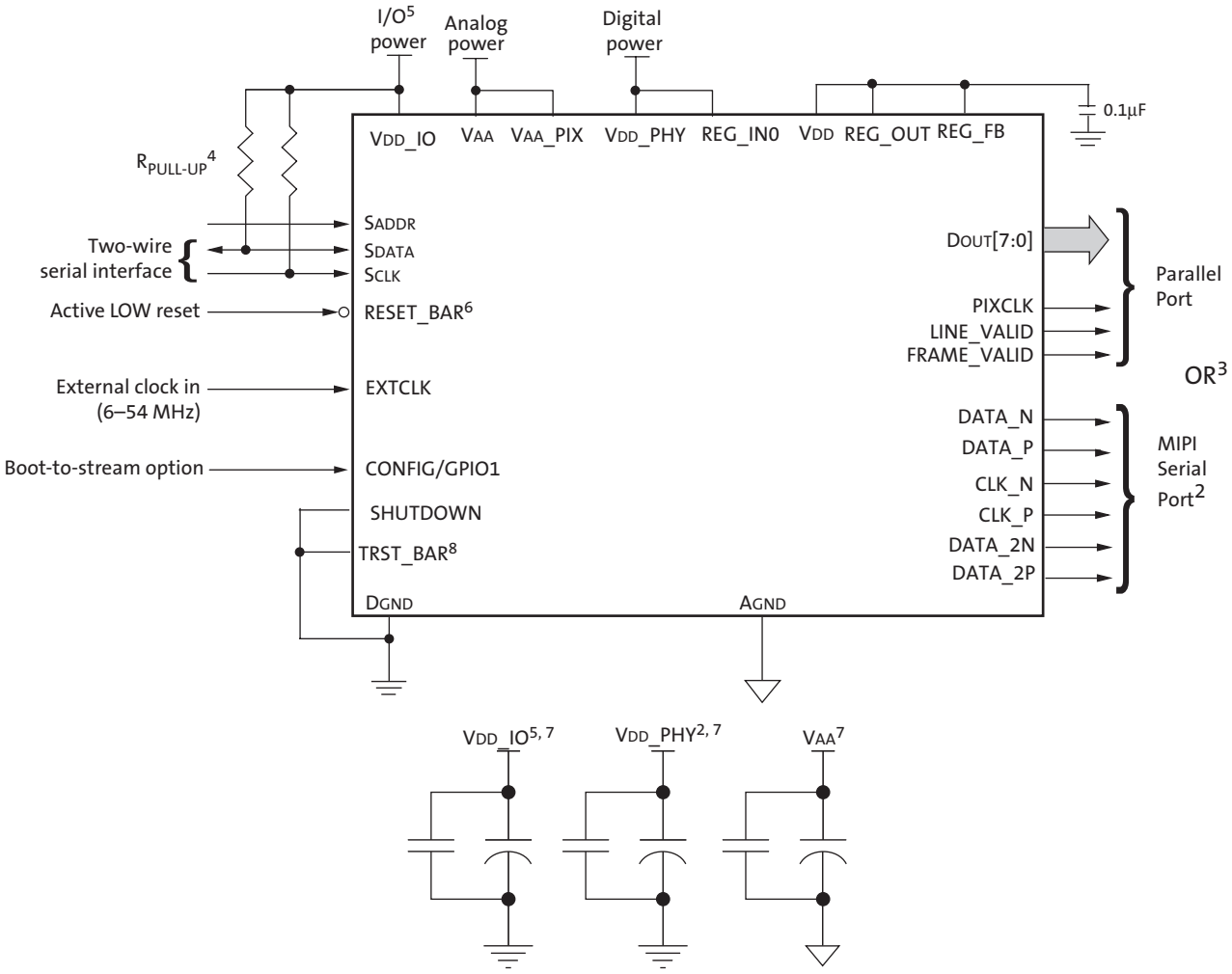
The AS0260 imager die also has several pads defined as “reserved.” These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows the AS0260 typical die connections. For low-noise operation, the AS0260 die requires separate supplies for analog and digital power.

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Figure 1: Typical Configuration



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI Interface is not required, the MIPI serial port must be left floating. The VDD_PHY power signal must always be connected to the 1.8V supply.
3. Only one of the output modes (serial or parallel) can be used at any time.
4. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
5. All inputs must be configured with VDD_IO.
6. RESET_BAR has an internal pull-up resistor and can be left floating.
7. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and numbers may vary depending on layout and design considerations.
8. TRST_BAR connects to GND for normal operation.
9. Connections shown are for Revision 2 and later versions. Revision 1 of AS0260 requires VDD, REG_OUT, and REG_FB to be connected to REG_IN0.

Decoupling Capacitor Recommendations

It is important to provide clean, well-regulated power to each power supply. The customer is ultimately responsible for ensuring that clean power is provided for their own designs because hardware design is influenced by many factors, such as layout, operating conditions, and component selection.

The recommendations for capacitor placement and values listed below are based on our internal demo camera design and verified in hardware.

In order of preference, Aptina recommends:

1. Mount 0.1µF and 1µF decoupling capacitors for each power supply as close as possible to the pad and place a 10 µF capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design, use a 0.1µF and 1µF capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 µF capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, use a 1µF capacitor (preferred) or a 0.1 µF capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 µF capacitor for each supply off-module but close to each supply.
4. Give priority to the V_{AA} supply for additional decoupling capacitors.

Inductive filtering components are not recommended.

Follow best practices when performing physical layout. Refer to technical note TN-09-131.

Bond Pad Location and Identification Tables

Table 1: Bond Pad Location and Identification From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND2	0	0	0	0
2	VDD2	150.12	0	0.005910236	0
3	CLK_N	329.76	0	0.012982677	0
4	CLK_P	649.08	0	0.025554331	0
5	DATA_2N	1011.96	0	0.039840945	0
6	DATA_2P	1331.28	0	0.052412598	0
7	DATA_N	1580.4	0	0.062220472	0
8	DATA_P	1899.72	0	0.074792126	0
9	DGND6	2079.36	0	0.081864567	0
10	VDD_PHY	2229.48	0	0.087774803	0
11	VPP	2394	0	0.094251969	0
12	AGND2	2554.92	0	0.100587402	0
13	Reserved	2665.08	0	0.104924409	0
14	VAA_PIX0	2775.24	0	0.109261417	0
15	VAA_PIX1	2925.36	0	0.115171654	0
16	Reserved	3035.52	0	0.119508661	0
17	VAA0	3145.68	0	0.123845669	0
18	VAA1	3295.79	0	0.129755512	0
19	AGND0	3445.91	0	0.135665748	0
20	AGND1	3596.03	0	0.141575984	0
21	RESET_BAR	2989.79	-5851.2	0.117708268	-0.230362205
22	TRST_BAR	2839.67	-5851.2	0.111798031	-0.230362205
23	Reserved	2689.55	-5851.2	0.105887795	-0.230362205
24	SCLK	2539.44	-5851.2	0.099977953	-0.230362205
25	SDATA	2389.32	-5851.2	0.094067717	-0.230362205
26	SADDR	2239.2	-5851.2	0.08815748	-0.230362205
27	EXTCLK	2089.08	-5851.2	0.082247244	-0.230362205
28	VDD_IO0	1938.96	-5851.2	0.076337008	-0.230362205
29	PIXCLK	1786.92	-5851.2	0.070351181	-0.230362205
30	DGND3	1636.8	-5851.2	0.064440945	-0.230362205
31	GPIO2	1486.69	-5851.2	0.058531102	-0.230362205
32	VDD0	1336.57	-5851.2	0.052620866	-0.230362205
33	DGND0	1186.46	-5851.2	0.046711024	-0.230362205
34	DOUT7	-325.05	-5446.72	-0.012797244	-0.214437795
35	DOUT6	-325.05	-5272.96	-0.012797244	-0.20759685
36	DGND4	-325.05	-5122.84	-0.012797244	-0.201686614
37	DOUT5	-325.05	-4972.72	-0.012797244	-0.195776378
38	VDD_IO1	-325.05	-4822.6	-0.012797244	-0.189866142
39	DOUT4	-325.05	-4672.48	-0.012797244	-0.183955906
40	DOUT3	-325.05	-4489.84	-0.012797244	-0.176765354
41	DGND5	-325.05	-4339.72	-0.012797244	-0.170855118
42	DOUT2	-325.05	-4189.6	-0.012797244	-0.164944882
43	VDD_IO2	-325.05	-4039.48	-0.012797244	-0.159034646

Table 1: Bond Pad Location and Identification From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	DOUT1	-325.05	-3889.36	-0.012797244	-0.153124409
45	DOUT0	-325.05	-3706.72	-0.012797244	-0.145933858
46	DGND6	-325.05	-3556.6	-0.012797244	-0.140023622
47	CHAIN/GPIO0	-325.05	-3406.48	-0.012797244	-0.134113386
48	VDD_IO3	-325.05	-3256.37	-0.012797244	-0.128203543
49	CONFIG/GPIO1	-325.05	-3106.25	-0.012797244	-0.122293307
50	FRAME_VALID	-325.05	-2923.61	-0.012797244	-0.115102756
51	DGND1	-325.05	-2773.49	-0.012797244	-0.10919252
52	LINE_VALID	-325.05	-2623.37	-0.012797244	-0.103282283
53	SHUTDOWN	-325.05	-2463.05	-0.012797244	-0.096970472
54	VDD1	-325.05	-2252.09	-0.012797244	-0.088664961
55	REG_IN0	-325.05	-2101.97	-0.012797244	-0.082754724
56	REG_OUT	-325.05	-1857.11	-0.012797244	-0.073114567
57	REG_FB	-325.05	-1707.11	-0.012797244	-0.067209055
58	DGND7	-325.05	-1454.215	-0.012797244	-0.057252559

Notes: 1. Reference to center of each bond pad from center of bond pad 1.
2. Reserved = do not use. See "Bonding Instructions" on page 3

Table 2: Bond Pad Location and Identification From Center of Die (0,0)

Pad Number	Pad Name	"X" Microns	"Y" Microns	"X" Inches	"Y" Inches
1	DGND2	-1677.05	2925.6	-0.066025591	0.115181102
2	VDD2	-1526.93	2925.6	-0.060115354	0.115181102
3	CLK_N	-1347.29	2925.6	-0.053042913	0.115181102
4	CLK_P	-1027.97	2925.6	-0.04047126	0.115181102
5	DATA_2N	-665.09	2925.6	-0.026184646	0.115181102
6	DATA_2P	-345.77	2925.6	-0.013612992	0.115181102
7	DATA_N	-96.65	2925.6	-0.003805118	0.115181102
8	DATA_P	222.67	2925.6	0.008766535	0.115181102
9	DGND6	402.31	2925.6	0.015838976	0.115181102
10	VDD_PHY	552.43	2925.6	0.021749213	0.115181102
11	VPP	716.95	2925.6	0.028226378	0.115181102
12	AGND2	877.87	2925.6	0.034561811	0.115181102
13	Reserved	988.03	2925.6	0.038898819	0.115181102
14	VAA_PIX0	1098.19	2925.6	0.043235827	0.115181102
15	VAA_PIX1	1248.31	2925.6	0.049146063	0.115181102
16	Reserved	1358.47	2925.6	0.053483071	0.115181102
17	VAA0	1468.63	2925.6	0.057820079	0.115181102
18	VAA1	1618.74	2925.6	0.063729921	0.115181102
19	AGND0	1768.86	2925.6	0.069640157	0.115181102
20	AGND1	1918.98	2925.6	0.075550394	0.115181102
21	RESET_BAR	1312.74	-2925.6	0.051682677	-0.115181102
22	TRST_BAR	1162.62	-2925.6	0.045772441	-0.115181102
23	Reserved	1012.5	-2925.6	0.039862205	-0.115181102

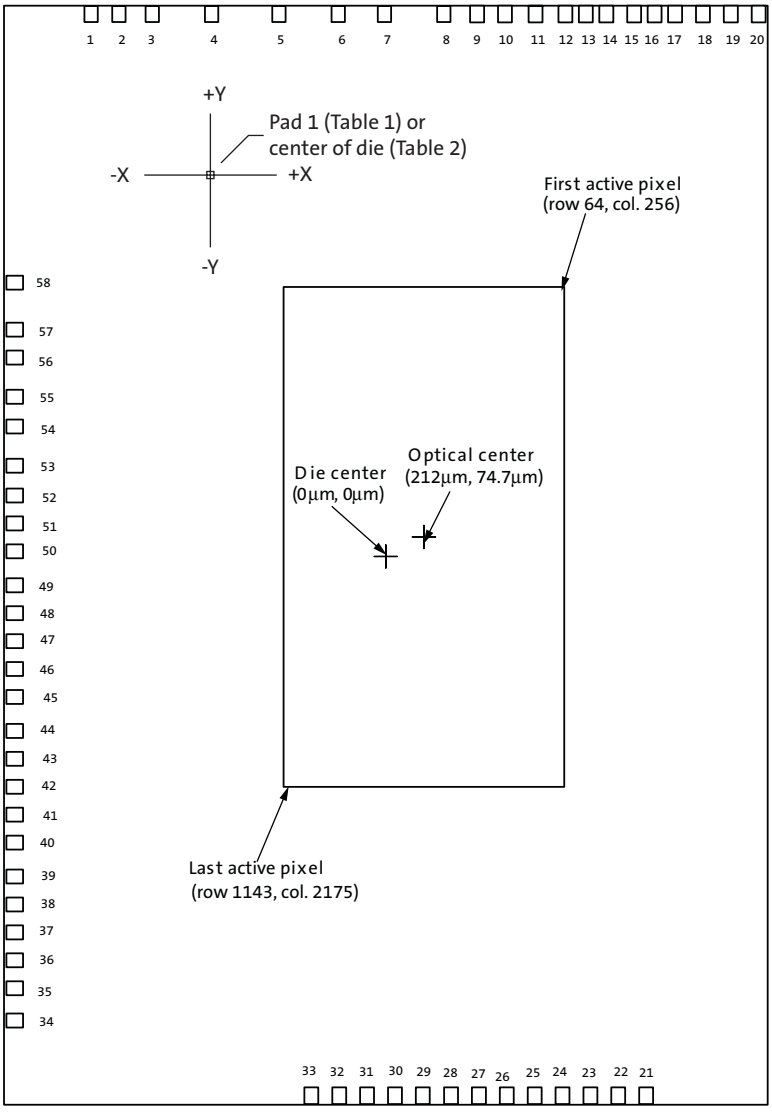
Table 2: Bond Pad Location and Identification From Center of Die (0,0)

Pad Number	Pad Name	"X" Microns	"Y" Microns	"X" Inches	"Y" Inches
24	SCLK	862.39	-2925.6	0.033952362	-0.115181102
25	SDATA	712.27	-2925.6	0.028042126	-0.115181102
26	SADDR	562.15	-2925.6	0.02213189	-0.115181102
27	EXTCLK	412.03	-2925.6	0.016221654	-0.115181102
28	VDD_IO0	261.91	-2925.6	0.010311417	-0.115181102
29	PIXCLK	109.87	-2925.6	0.004325591	-0.115181102
30	DGND3	-40.25	-2925.6	-0.001584646	-0.115181102
31	GPIO2	-190.36	-2925.6	-0.007494488	-0.115181102
32	VDD0	-340.48	-2925.6	-0.013404724	-0.115181102
33	DGND0	-490.59	-2925.6	-0.019314567	-0.115181102
34	DOUT7	-2002.1	-2521.12	-0.078822835	-0.099256693
35	DOUT6	-2002.1	-2347.36	-0.078822835	-0.092415748
36	DGND4	-2002.1	-2197.24	-0.078822835	-0.086505512
37	DOUT5	-2002.1	-2047.12	-0.078822835	-0.080595276
38	VDD_IO1	-2002.1	-1897	-0.078822835	-0.074685039
39	DOUT4	-2002.1	-1746.88	-0.078822835	-0.068774803
40	DOUT3	-2002.1	-1564.24	-0.078822835	-0.061584252
41	DGND5	-2002.1	-1414.12	-0.078822835	-0.055674016
42	DOUT2	-2002.1	-1264	-0.078822835	-0.04976378
43	VDD_IO2	-2002.1	-1113.88	-0.078822835	-0.043853543
44	DOUT1	-2002.1	-963.76	-0.078822835	-0.037943307
45	DOUT0	-2002.1	-781.12	-0.078822835	-0.030752756
46	DGND6	-2002.1	-631	-0.078822835	-0.02484252
47	CHAIN/GPIO0	-2002.1	-480.88	-0.078822835	-0.018932283
48	VDD_IO3	-2002.1	-330.77	-0.078822835	-0.013022441
49	CONFIG/GPIO1	-2002.1	-180.65	-0.078822835	-0.007112205
50	FRAME_VALID	-2002.1	1.99	-0.078822835	7.83465E-05
51	DGND1	-2002.1	152.11	-0.078822835	0.005988583
52	LINE_VALID	-2002.1	302.23	-0.078822835	0.011898819
53	SHUTDOWN	-2002.1	462.55	-0.078822835	0.01821063
54	VDD1	-2002.1	673.51	-0.078822835	0.026516142
55	REG_IN0	-2002.1	823.63	-0.078822835	0.032426378
56	REG_OUT	-2002.1	1068.49	-0.078822835	0.042066535
57	REG_FB	-2002.1	1218.49	-0.078822835	0.047972047
58	DGND7	-2002.1	1471.385	-0.078822835	0.057928543

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. Reserved = do not use." See "Bonding Instructions" on page 3.

Die Features

Figure 2: Die Outline (Top View)



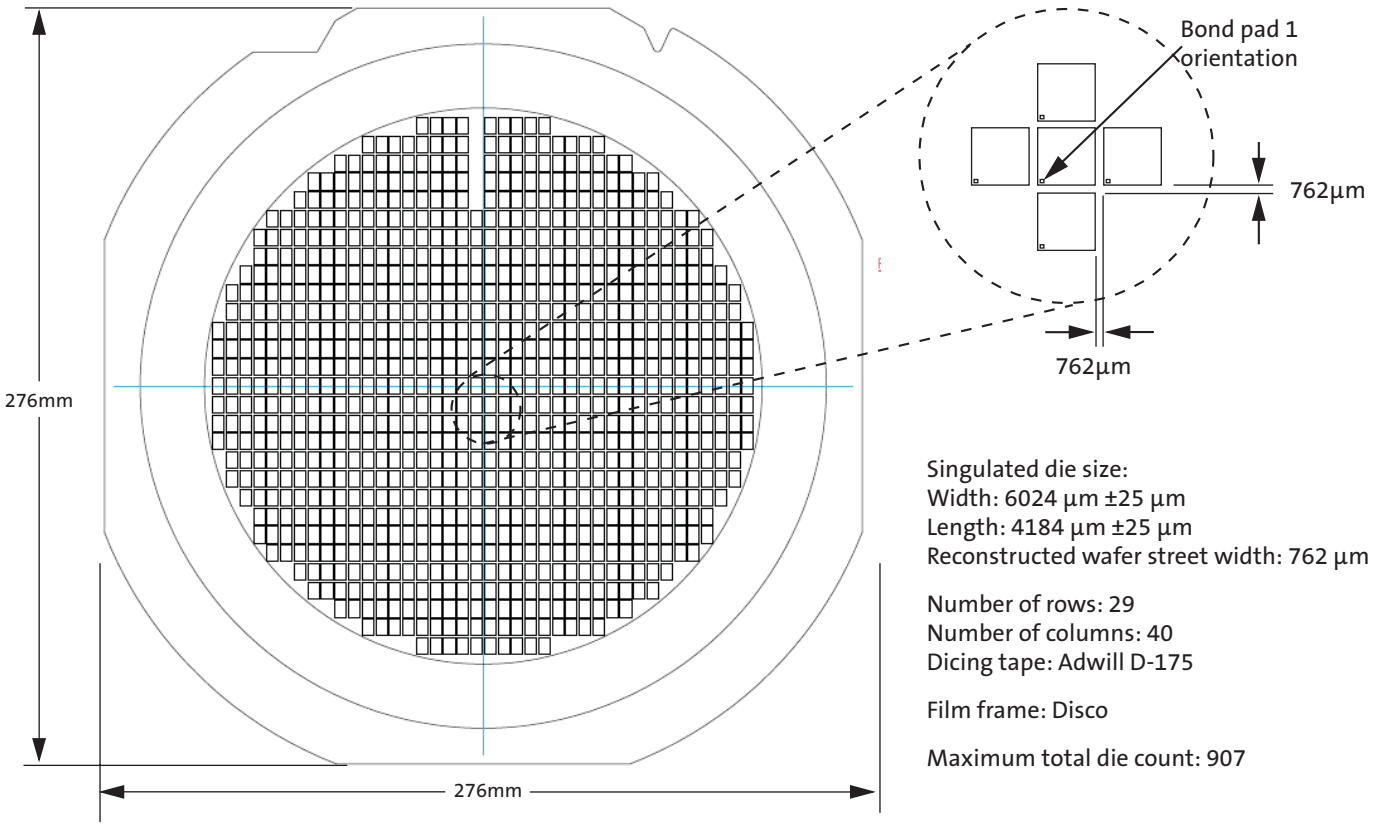
Note: This figure is not drawn to scale.

Physical Specifications

Table 3: Die Dimensions

Features	Dimensions
Die thickness	200µm ±12µm
Singulated die size Width: Length:	 6024 µm ±25 µm 4184 µm ±25 µm
Bond pad size (MIN)	85 µm x 100 µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75 µm x 90 µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	110.4 µm (4.34203 mil)
Optical array Optical center from die center:	 X = 212 µm, Y = 74.7 µm
First active pixel (row 64, col. 256) From die center:	 X = 967.7µm, Y = 1418.7 µm
Last active pixel (row 1143, col. 2175) From die center:	 X =–544.3 µm, Y = –1269.3 µm

Figure 3: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 6024 µm ±25 µm
Length: 4184 µm ±25 µm
Reconstructed wafer street width: 762 µm

Number of rows: 29
Number of columns: 40
Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 907

Revision History

Rev. E 6/7/12

- Updated to Production
- Updated "Features" on page 1
- Updated "Key Performance Parameters" on page 1
- Updated Figure 1: "Typical Configuration," on page 4
- Updated Figure 3: "Die Orientation in Reconstructed Wafer," on page 10

Rev. D 1/24/12

- Updated "Order Information" on page 1
- Updated Figure 2: " Die Outline (Top View)," on page 9
- Updated Table 3, "Die Dimensions," on page 10

Rev. C 10/18/11

- Updated singulated die size in "Die Database" on page 1, Table 3, "Die Dimensions," on page 10, and Figure 3: "Die Orientation in Reconstructed Wafer," on page 10
- Updated Figure 1: "Typical Configuration," on page 4
- Added Table 2, "Bond Pad Location and Identification From Center of Die (0,0)," on page 7
- Updated Figure 3: "Die Orientation in Reconstructed Wafer," on page 10

Rev. B 10/17/11

- Removed Table 2, "Bond Pad Location and Identification From Center of Die (0,0)"

Rev. A 7/15/11

- Initial release

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