1/3-Inch Wide-VGA CMOS Digital Image Sensor Die

MT9V022

For the packaged product data sheet, refer to Micron's Web site: www.micron.com

Features

- Micron® DigitalClarity® CMOS imaging technology
- Global shutter photodiode pixels; simultaneous integration and readout
- Monochrome or color: Near-IR enhanced performance for use with non-visible NIR illumination
- Readout modes: Progressive or interlaced
- Simple two-wire serial interface
- Register lock capability
- Window size: User programmable to any smaller format (QVGA, CIF, QCIF, etc.). Data rate can be maintained independent of window size
- Binning: 2 x 2 and 4 x 4 of the full resolution
- ADC: On-die, 10-bit column-parallel (option to operate in 12-bit to 10-bit companding mode)
- Automatic controls: Auto exposure control (AEC) and auto gain control (AGC); variable regional and variable weight AEC/AGC
- Support for four unique serial control register IDs to control multiple imagers on the same bus
- Data output formats
  - Single sensor mode: 10-bit parallel/standalone 8-bit or 10-bit serial LVDS
  - Stereo sensor mode: Interspersed 8-bit serial LVDS

General Physical Specifications

- Die thickness: 200µm ±12µm
  (Consult factory for die thickness other than 200µm)
- Backside wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

MT9V022D00ATMC13BC1 (Monochrome)

MT9V022D00ATCC13BC1 (Color)

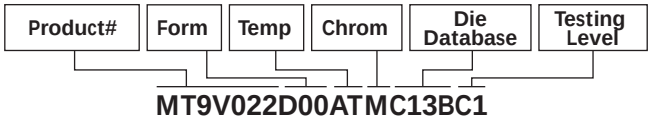
Die Database C13B

- Die outline, see Figure 2 on page 9
- Singulated die size: 6,398µm ±25µm x 5,794µm ±25µm
- Bond Pad Location and Identification Tables, see pages 5–8

Options

- Form
  - Die — D
- Testing
  - Standard (level 1) probe — C1

Note: Please consult die distributor or factory before ordering to verify long-term availability of these die products.



Key Performance Parameters

- Optical format: 1/3-inch
- Active imager size: 4.51mm x 2.88mm, 5.35mm diagonal
- Active pixels: 752H x 480V
- Pixel size: 6.0µm x 6.0µm
- Color filter array: Monochrome or color RGB Bayer pattern
- Shutter type: Global shutter - TrueSNAP™
- Maximum data rate/master clock: 26.6 MPS/26.6 MHz
- Full resolution: 752H x 480V
- Frame rate: 60 fps at full resolution
- ADC resolution: 10-bit column-parallel
- Responsivity: 4.8 V/lux-sec (550nm)
- Dynamic range: >55dB linear; >80dB–100dB in HiDy mode
- Supply voltage: 3.3V ±0.3V (all supplies)
- Power consumption: <320mW at maximum data rate; <100µW in standby mode
- Operating temperature: –40°C to +85°C

General Description

Micron Imaging MT9V022 die is a 1/3-inch wide-VGA format CMOS active-pixel digital image sensor with a global shutter and high dynamic range operation. The sensor has specifically been designed to support the demanding interior and exterior automotive imaging needs, which makes this part ideal for a wide variety of imaging applications in real-world environments

This wide-VGA CMOS image sensor features DigitalClarity—Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on-die—such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions—as well as windowing, column and row mirroring. It is programmable through a simple two-wire serial interface.

The MT9V022 can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide-VGA-size image at 60 frames per second (fps).

An on-die analog-to-digital converter (ADC) provides 10 bits per pixel. The user can alternatively enable 12-bit resolution companded to 10-bits for small signals, enabling more accurate digitization for darker areas in the image.

In addition to a traditional, parallel low-voltage, logic output, the MT9V022 also features a serial low-voltage differential signaling (LVDS) output. The sensor can be operated in a stereo-camera, and the sensor, designated as a stereo-master, is able to merge the data from itself and the stereo-slave sensor into one serial LVDS stream.

The sensor is designed to operate within a wide temperature range (–40°C to +85°C).

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided here are for reference only. For functional and parametric specifications, refer to the packaged product data sheets found on Micron's Web site.

Bonding Instructions

The MT9V022 imager die has 65 bond pads. Refer to Tables 1 and 2 on pages 5–8 for a complete list of bond pads and coordinates.

The MT9V022 Imager die does not require the user to determine bond option features.

Figure 1 on page 4 shows the MT9V022 typical die connections for parallel output mode operation. For low-noise operation the MT9V022 die requires separate supplies for analog and digital power. Both power supply rails should be decoupled to ground using ceramic capacitors. Use of inductance filters is not recommended.

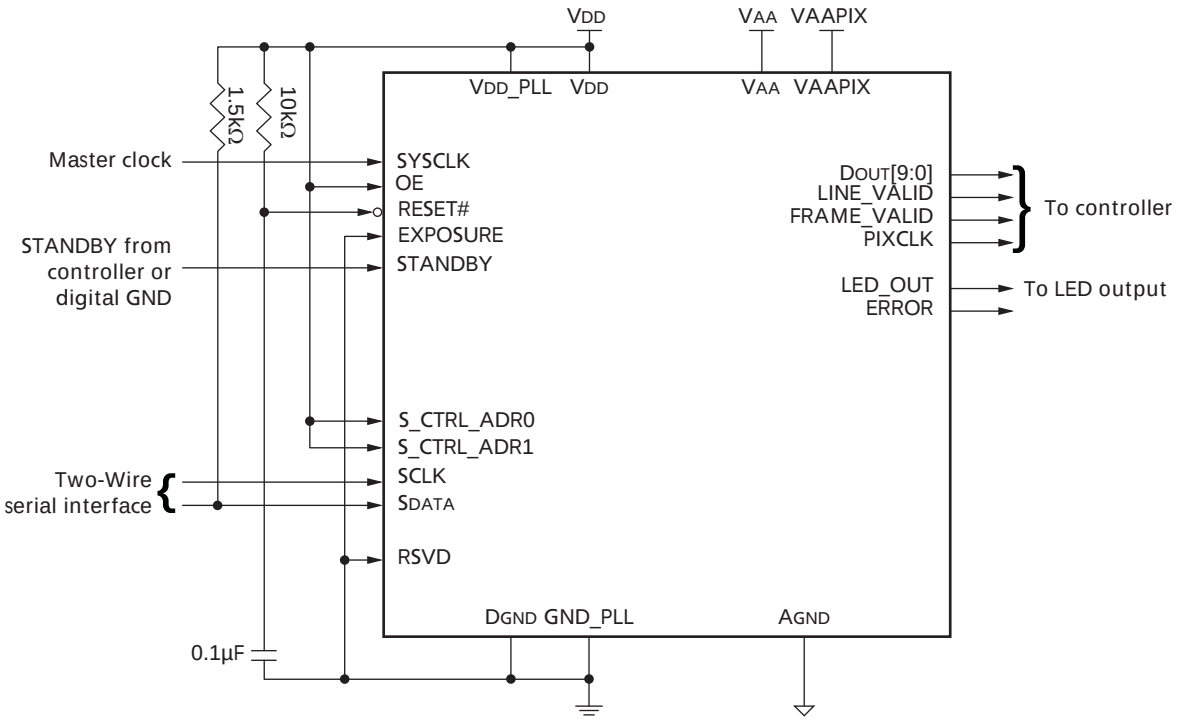
Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Figure 1: Typical Configuration (Connection) Parallel Output Mode



Notes: 1. LVDS signals are to be left floating.

Bond Pad Location and Identification Tables

Table 1: MT9V022 Bond Pad Location From Center of Pad 1

Pad	MT9V022	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_PLL1	0.00	0.00	0.0000000	0.0000000
2	SER_DATAOUT_P	140.85	0.00	0.0055453	0.0000000
3	SER_DATAOUT_N	423.63	0.00	0.0166783	0.0000000
4	SHFT_CLKOUT_P	790.84	0.00	0.0311354	0.0000000
5	SHFT_CLKOUT_N	1073.66	0.00	0.0422685	0.0000000
6	VDD_PLL2	1203.67	0.00	0.0473886	0.0000000
7	VDD3	1770.47	0.00	0.0697035	0.0000000
8	VDD2	2003.75	0.00	0.0788878	0.0000000
9	VDD1	2237.03	0.00	0.0880720	0.0000000
10	DGND3	2581.19	0.00	0.1016217	0.0000000
11	DGND2	2814.47	0.00	0.1108059	0.0000000
12	DGND1	3047.75	0.00	0.1199902	0.0000000
13	SYSCLK	3514.31	0.00	0.1383587	0.0000000
14	PIXCLK	3858.47	0.00	0.1519083	0.0000000
15	DOUT0	4202.63	0.00	0.1654579	0.0000000
16	DOUT1	4669.19	0.00	0.1838264	0.0000000
17	DOUT2	5135.75	0.00	0.2021949	0.0000000
18	DOUT3	5558.99	–288.07	0.2188579	–0.0113411
19	DOUT4	5558.99	–521.35	0.2188579	–0.0205254
20	VAAPIX0	5558.99	–902.17	0.2188579	–0.0355183
21	VAAPIX1	5558.99	–1135.45	0.2188579	–0.0447026
22	VAA4	5558.99	–1368.73	0.2188579	–0.0538868
23	VAA3	5558.99	–1602.01	0.2188579	–0.0630711
24	AGND4	5558.99	–1856.57	0.2188579	–0.0730931
25	AGND3	5558.99	–2089.85	0.2188579	–0.0822774
26	DNU[2]	5558.99	–2646.01	0.2188579	–0.1041734
27	DNU	5558.99	–2924.23	0.2188579	–0.1151270
28	DNU	5558.99	–3157.51	0.2188579	–0.1243112
29	DNU	5558.99	–3390.79	0.2188579	–0.1334955
30	VAA2	5558.99	–3857.35	0.2188579	–0.1518640
31	VAA1	5558.99	–4090.63	0.2188579	–0.1610482
32	AGND2	5558.99	–4323.91	0.2188579	–0.1702325
33	AGND1	5558.99	–4557.19	0.2188579	–0.1794167
34	STANDBY	5558.99	–4963.79	0.2188579	–0.1954246
35	RESET#	5558.99	–5197.07	0.2188579	–0.2046089
36	S_CTRL_ADR1	4978.36	–5485.13	0.1959982	–0.2159500
37	S_CTRL_ADR0	4511.80	–5485.13	0.1776297	–0.2159500
38	RSVD[3]	4167.64	–5485.13	0.1640801	–0.2159500

Table 1: MT9V022 Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9V022	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
39	OE	3701.08	–5485.13	0.1457116	–0.2159500
40	LED_OUT	3234.52	–5485.13	0.1273431	–0.2159500
41	ERROR	2890.36	–5485.13	0.1137935	–0.2159500
42	STFRM_OUT	2423.80	–5485.13	0.0954250	–0.2159500
43	SCLK	2079.64	–5485.13	0.0818754	–0.2159500
44	SDATA	1613.08	–5485.13	0.0635069	–0.2159500
45	EXPOSURE	1146.52	–5485.13	0.0451384	–0.2159500
46	STLN_OUT	802.36	–5485.13	0.0315888	–0.2159500
47	FRAME_VALID	335.80	–5485.13	0.0132203	–0.2159500
48	LINE_VALID	–130.77	–5485.13	–0.0051482	–0.2159500
49	DOUT9	–529.71	–5169.87	–0.0208547	–0.2035380
50	DOUT8	–529.71	–4878.99	–0.0208547	–0.1920860
51	DOUT7	–529.71	–4645.71	–0.0208547	–0.1829018
52	DOUT6	–529.71	–4179.15	–0.0208547	–0.1645333
53	DOUT5	–529.71	–3945.87	–0.0208547	–0.1553490
54	VDD6	–529.71	–3601.71	–0.0208547	–0.1417994
55	VDD5	–529.71	–3368.43	–0.0208547	–0.1326152
56	VDD4	–529.71	–3135.15	–0.0208547	–0.1234309
57	DGND6	–529.71	–2901.87	–0.0208547	–0.1142467
58	DGND5	–529.71	–2668.59	–0.0208547	–0.1050624
59	DGND4	–529.71	–2435.31	–0.0208547	–0.0958781
60	GND_PLL1	–529.71	–1735.63	–0.0208547	–0.0683317
61	SER_DATAIN_P	–529.71	–1529.71	–0.0208547	–0.0602246
62	SER_DATAIN_N	–529.71	–1398.67	–0.0208547	–0.0550656
63	BYPASS_CLKIN_P	–529.71	–793.09	–0.0208547	–0.0312240
64	BYPASS_CLKIN_N	–529.71	–662.05	–0.0208547	–0.0260650
65	GND_PLL2	–529.71	–456.13	–0.0208547	–0.0179579

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = "do not use."
3. RSVD must be tied to DGND for normal operation.

Table 2: MT9V022 Bond Pad Location From Center of Die (0, 0)

Pad	MT9V022	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_PLL1	–2514.65	2742.61	–0.0990018	0.1079766
2	SER_DATAOUT_P	–2373.80	2742.61	–0.0934565	0.1079766
3	SER_DATAOUT_N	–2091.02	2742.61	–0.0823234	0.1079766
4	SHFT_CLKOUT_P	–1723.81	2742.61	–0.0678663	0.1079766
5	SHFT_CLKOUT_N	–1441.03	2742.61	–0.0567333	0.1079766
6	VDD_PLL2	–1310.98	2742.61	–0.0516132	0.1079766
7	VDD3	–744.18	2742.61	–0.0292982	0.1079766
8	VDD2	–510.90	2742.61	–0.0201140	0.1079766
9	VDD1	–277.62	2742.61	–0.0109297	0.1079766
10	DGND3	66.55	2742.61	0.0026199	0.1079766
11	DGND2	299.83	2742.61	0.0118041	0.1079766
12	DGND1	533.11	2742.61	0.0209884	0.1079766
13	SYSCLK	999.67	2742.61	0.0393569	0.1079766
14	PIXCLK	1343.83	2742.61	0.0529065	0.1079766
15	DOUT0	1687.99	2742.61	0.0664561	0.1079766
16	DOUT1	2154.55	2742.61	0.0848246	0.1079766
17	DOUT2	2621.11	2742.61	0.1031931	0.1079766
18	DOUT3	3044.35	2454.54	0.1198561	0.0966354
19	DOUT4	3044.35	2221.26	0.1198561	0.0874512
20	VAAPIX0	3044.35	1840.44	0.1198561	0.0724583
21	VAAPIX1	3044.35	1607.16	0.1198561	0.0632740
22	VAA4	3044.35	1373.88	0.1198561	0.0540898
23	VAA3	3044.35	1140.60	0.1198561	0.0449055
24	AGND4	3044.35	886.04	0.1198561	0.0348835
25	AGND3	3044.35	652.76	0.1198561	0.0256992
26	DNU[2]	3044.35	96.60	0.1198561	0.0038031
27	DNU	3044.35	–181.62	0.1198561	–0.0071504
28	DNU	3044.35	–414.90	0.1198561	–0.0163346
29	DNU	3044.35	–648.18	0.1198561	–0.0255189
30	VAA2	3044.35	–1114.74	0.1198561	–0.0438874
31	VAA1	3044.35	–1348.02	0.1198561	–0.0530717
32	AGND2	3044.35	–1581.30	0.1198561	–0.0622559
33	AGND1	3044.35	–1814.58	0.1198561	–0.0714402
34	STANDBY	3044.35	–2221.18	0.1198561	–0.0874480
35	RESET#	3044.35	–2454.46	0.1198561	–0.0966323
36	S_CTRL_ADR1	2463.71	–2742.53	0.0969965	–0.1079734
37	S_CTRL_ADR0	1997.15	–2742.53	0.0786280	–0.1079734
38	RSVD[3]	1652.99	–2742.53	0.0650783	–0.1079734

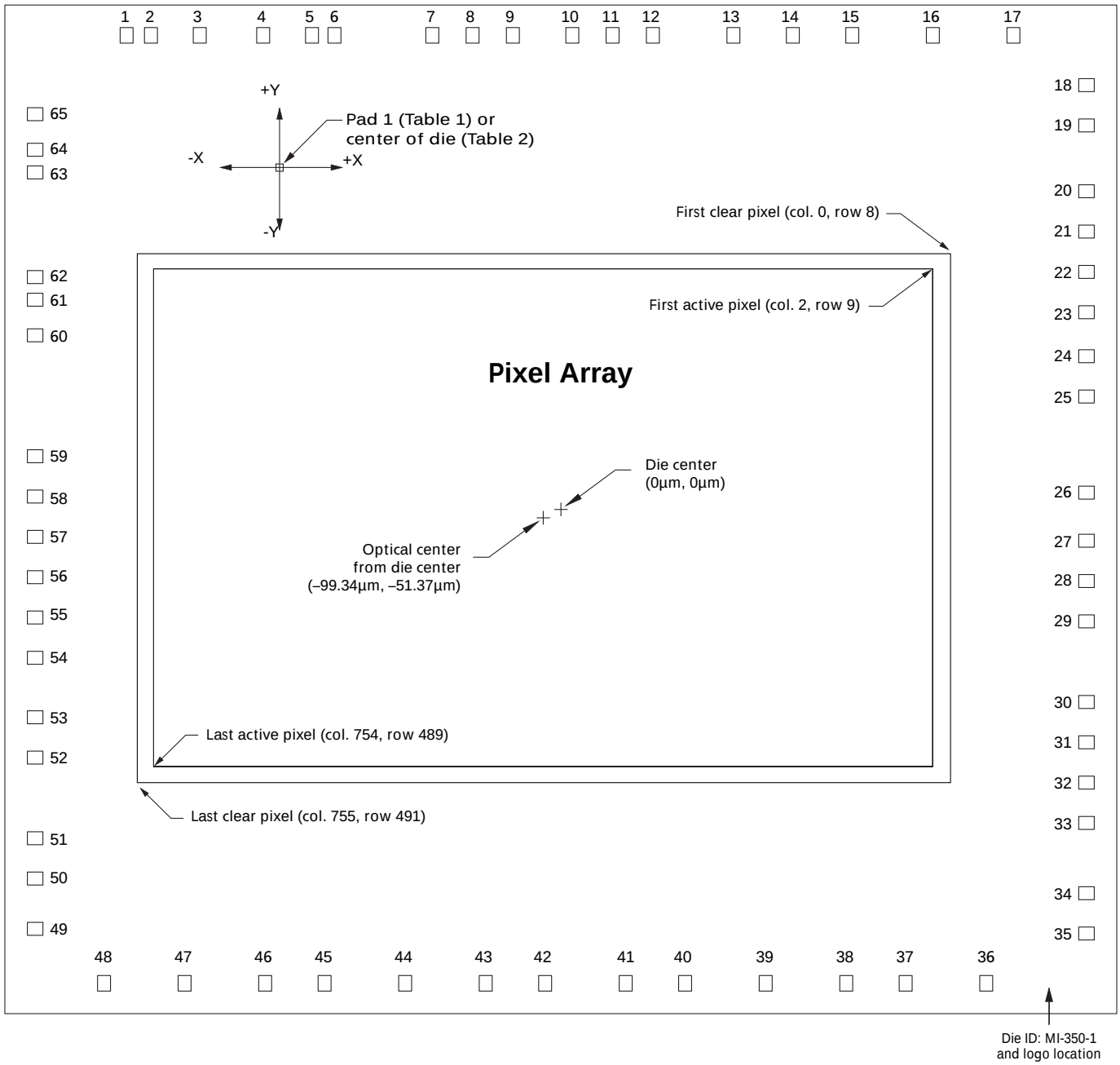
Table 2: MT9V022 Bond Pad Location From Center of Die (0, 0) (continued)

Pad	MT9V022	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
39	OE	1186.43	–2742.53	0.0467098	–0.1079734
40	LED_OUT	719.87	–2742.53	0.0283413	–0.1079734
41	ERROR	375.71	–2742.53	0.0147917	–0.1079734
42	STFRM_OUT	–90.85	–2742.53	–0.0035768	–0.1079734
43	SCLK	–435.01	–2742.53	–0.0171264	–0.1079734
44	SDATA	–901.57	–2742.53	–0.0354949	–0.1079734
45	EXPOSURE	–1368.13	–2742.53	–0.0538634	–0.1079734
46	STLN_OUT	–1712.29	–2742.53	–0.0674130	–0.1079734
47	FRAME_VALID	–2178.85	–2742.53	–0.0857815	–0.1079734
48	LINE_VALID	–2645.41	–2742.53	–0.1041500	–0.1079734
49	DOUT9	–3044.36	–2427.26	–0.1198565	–0.0955614
50	DOUT8	–3044.36	–2136.38	–0.1198565	–0.0841094
51	DOUT7	–3044.36	–1903.10	–0.1198565	–0.0749252
52	DOUT6	–3044.36	–1436.54	–0.1198565	–0.0565567
53	DOUT5	–3044.36	–1203.26	–0.1198565	–0.0473724
54	VDD6	–3044.36	–859.10	–0.1198565	–0.0338228
55	VDD5	–3044.36	–625.82	–0.1198565	–0.0246386
56	VDD4	–3044.36	–392.54	–0.1198565	–0.0154543
57	DGND6	–3044.36	–159.26	–0.1198565	–0.0062701
58	DGND5	–3044.36	74.02	–0.1198565	0.0029142
59	DGND4	–3044.36	307.30	–0.1198565	0.0120984
60	GND_PLL1	–3044.36	1006.98	–0.1198565	0.0396449
61	SER_DATAIN_P	–3044.36	1212.90	–0.1198565	0.0477520
62	SER_DATAIN_N	–3044.36	1343.94	–0.1198565	0.0529110
63	BYPASS_CLKIN_P	–3044.36	1949.52	–0.1198565	0.0767526
64	BYPASS_CLKIN_N	–3044.36	2080.56	–0.1198565	0.0819116
65	GND_PLL2	–3044.36	2286.48	–0.1198565	0.0900187

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = "do not use."
3. RSVD must be tied to DGND for normal operation.

Die Features

Figure 2: Die Outline (Top View)

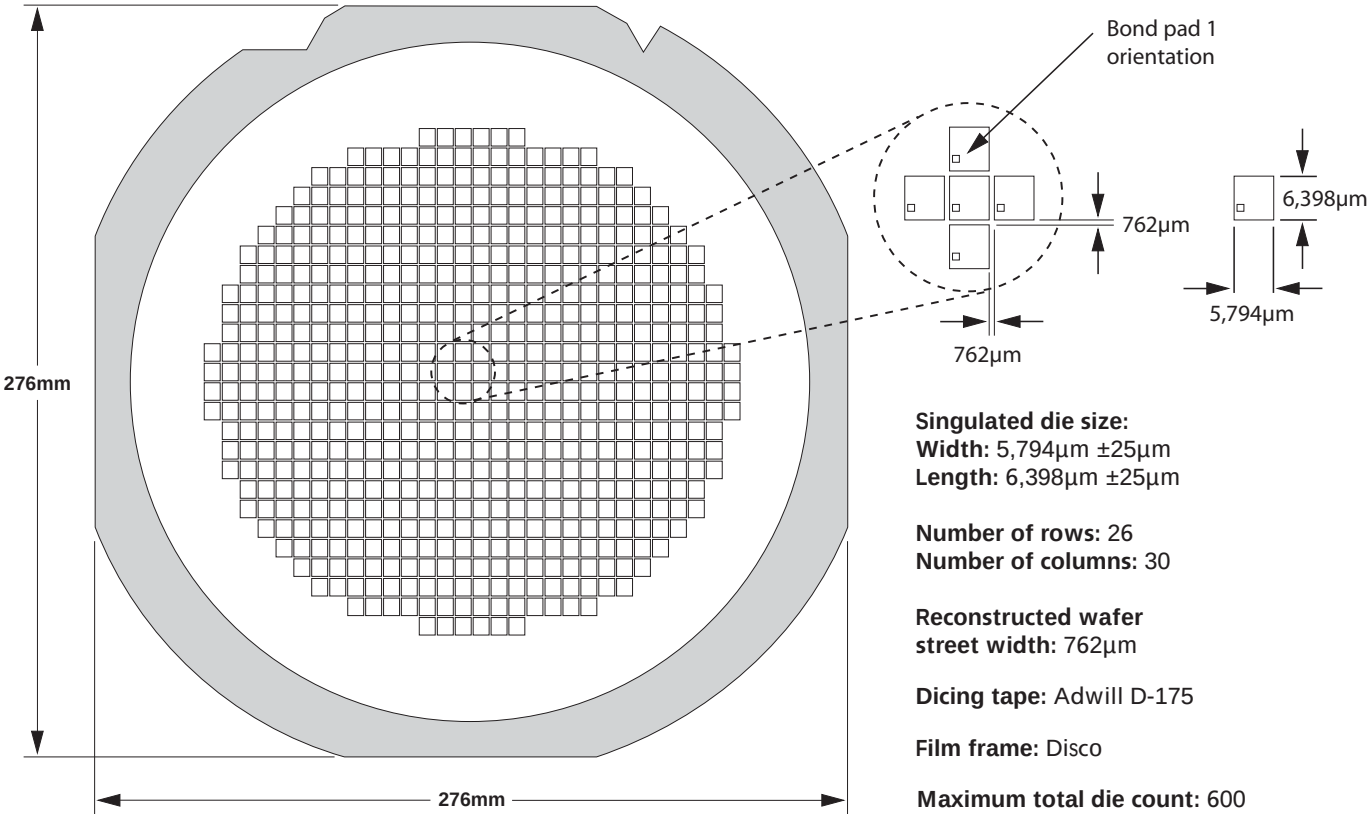


Physical Specifications

Table 3: Die Dimensions

Features	Dimensions
Die thickness	200µm ±12µm
Singulated die size *Width:* *Length:*	 6,398µm ±25µm 5,794µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	131.04µm (5.159 mil)
Optical array *Optical center from die center:* *Optical center from center of pad 1:*	 X = –99.34µm, Y = –51.37µm X = 2,415.31µm, Y = –2,793.98µm
First clear pixel (col. 0, row 8) *From die center:* *From center of pad 1:*	 X = 2,165.67µm, Y = 1,397.64µm X = 4,680.32µm, Y = –1,344.97µm
Last clear pixel (col. 755, row 491) *From die center:* *From center of pad 1:*	 X = –2,364.34µm, Y = –1,500.37µm X = 150.31µm, Y = –4,242.98µm
First active pixel (col 2, row 9) *From die center:* *From center of pad 1:*	 X = 2,153.67µm, Y = 1,391.64µm X = 4,668.32µm, Y = –1,350.97µm
Last active pixel (col 754, row 489) *From die center:* *From center of pad 1:*	 X = –2,358.34µm, Y = –1,488.37µm X = 156.31µm, Y = –4,230.98µm

Figure 3: MT9V022 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 5,794µm ±25µm
Length: 6,398µm ±25µm

Number of rows: 26
Number of columns: 30

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 600

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Revision History

Rev. G, Production 8/07

- Corrected X coordinates in Table 1 from 1071.66 (microns)/0.000.0421911 (inches) to 1073.66 (microns)/0.000.0422685 (inches).

Rev. F, Production 4/07

- Updated template.
- Updated Figure 3 on page 11.

Rev. E, Production 12/06

- Updated Figure 2 on page 9 to show both active and clear pixel positions on die.
- Updated Table 3 on page 10 with both active and clear pixel dimensions.
- Changed document designation to Production.
- Changed voltage designations from VDDLVDS to VDD_PLL and LVDSGND to GND_PLL.

Rev. D, Preliminary 7/06

- Changed die thickness to 200µm ± 12µm (7.9 mil ± 0.5 mil)
- Updated “Key Performance Parameters” on page 1 and “Typical Configuration (Connection) Parallel Output Mode” on page 4.
- Updated wording about parallel low voltage and thermal diode in“General Description” on page 2.
- Updated template.

Rev. C, Preliminary 1/06

- Updated template.

Rev. B, Preliminary 3/05

- Changed pads 26 and 28 from RSVD to DNU.
- Removed wafer option information

Rev. A, Preliminary 2/05

- Initial release.