1/11-Inch VGA CMOS Digital Image Sensor Die

MT9V013

For the product data sheet, refer to Micron's Web site: www.micron.com

Features

- Micron® DigitalClarity® CMOS imaging technology
- Low dark current
- Simple two-wire serial interface
- Auto black calibration
- Support for external LED or xenon flash
- Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, panning, and skip 2X
- SMIA-compatible
- Data interface: CCP2-compliant sub-low-voltage differential signalling (sub-LVDS)
- On-die phase-lock loop (PLL) oscillator
- Superior low-light performance

Applications

- Cellular phones
- PC cameras
- PDAs

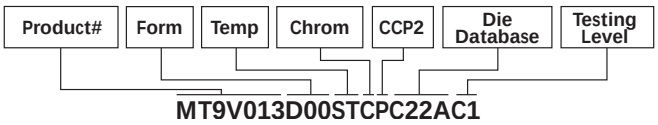
General Physical Specifications

- Die thickness
  - 200µm ±12µm

  (Consult factory for other die thickness)
- Backside wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.2kÅ
- Typical metal 3 thickness: 3.2kÅ
- Typical metal 4 thickness: 4.0kÅ
- Metallization composition
  - 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation
  - 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

MT9V013D00STCP C22AC1



Die Database C22A

- Die outline, see Figure 2 on page 7
- Singulated die size (nominal dimension): 2,461µm ±25µm x 2,731µm ±25µm
- Bond Pad Location and Identification Tables, see pages 5–6

Options

- Form
  - Die — D
- Testing
  - Standard (level 1) probe — C1

1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Key Performance Parameters

- Optical format: 1/11-inch VGA (4:3)
- Active imager size
  - 1.43mm(H) x 1.07mm(V), 1.78mm diagonal
- Active pixels: 648H x 488V
- Pixel size: 2.2µm x 2.2µm
- Color filter array: RGB Bayer pattern
- Shutter type: Electronic rolling shutter (ERS)
- Maximum data rate/master clock
  - 14 Mp/s at 14 MHz system clock
- Frame rate
  - VGA (640H x 480V) programmable up to 30 fps
- ADC resolution: 10 bit, on-die
- Responsivity: 1.1 V/lux-sec
- Dynamic range: 64dB
- SNR MAX: >36.5dB
- Supply voltage: Analog 2.5–3.1V (2.8V nominal)
  - Digital, digital PHY 1.7–1.9V (1.8V nominal)
  - Digital I/O 1.7–1.9V (1.8V nominal)
- Power consumption: 80mW at 30 fps
- Operating temperature: –30°C to +70°C

General Description

Micron's Imaging MT9V013 die is a 1/11-inch VGA-format CMOS active-pixel digital image sensor with a pixel array of 640H x 480V (648H x 488V including border pixels). It incorporates sophisticated on-die camera functions, such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9V013 digital image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Because the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die analog-to-digital converter (ADC), logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9V013 imager die has 24 bond pads. Refer to Tables 1 and 2 on pages 5–6 for a complete list of bond pads and coordinates.

The MT9V013 imager die does not require the user to determine bond option features.

The MT9V013 imager die also has two pads defined as "do not use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows typical die connections. For low-noise operation, the MT9V013 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

Bond pad 21 (TEST_EN) must be grounded for proper device functionality.

Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

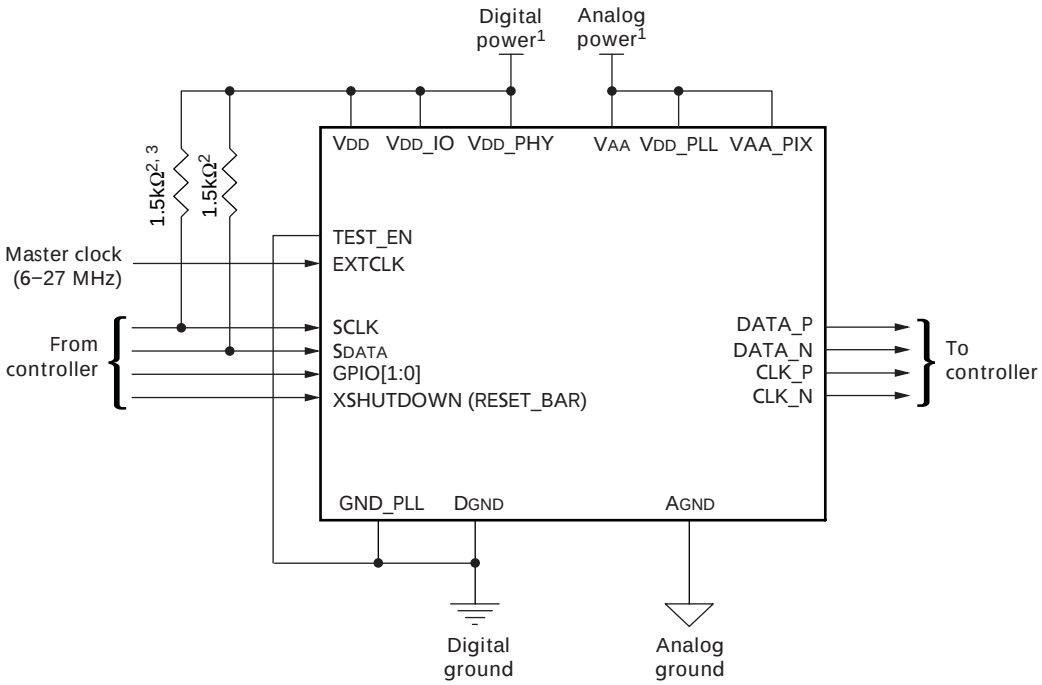
Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Operating Mode

By default, the MT9V013 powers up as an SMIA-compatible sensor with the serial pixel data interface enabled. A typical configuration in this mode is shown in Figure 1.

Figure 1: Typical Configuration (Connection)



Notes:
1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.

Bond Pad Location and Identification Tables

Table 1: MT9V013 Bond Pad Location and Identification from Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	SCLK	0.00	0.00	0.0000000	0.0000000
2	VAA	2180.80	–2401.20	0.0858583	–0.0945354
3	AGND	2070.60	–2401.20	0.0815197	–0.0945354
4	DNU[2]	1960.40	–2401.20	0.0771811	–0.0945354
5	DNU	1850.20	–2401.20	0.0728425	–0.0945354
6	VAA_PIX	1740.00	–2401.20	0.0685039	–0.0945354
7	DATA_N	1466.79	–2401.20	0.0577474	–0.0945354
8	DATA_P	1236.79	–2401.20	0.0486923	–0.0945354
9	CLK_N	1006.78	–2401.20	0.0396370	–0.0945354
10	CLK_P	776.78	–2401.20	0.0305819	–0.0945354
11	VDD_PHY	548.68	–2401.20	0.0216016	–0.0945354
12	GND_PLL	438.48	–2401.20	0.0172630	–0.0945354
13	VDD_PLL	328.28	–2401.20	0.0129244	–0.0945354
14	EXTCLK	0.00	–1816.56	0.0000000	–0.0715181
15	FLASH	0.00	–1638.50	0.0000000	–0.0645079
16	SDATA	0.00	–1439.56	0.0000000	–0.0566756
17	VDD_IO	0.00	–1288.76	0.0000000	–0.0507386
18	DGND2	0.00	–1178.56	0.0000000	–0.0464000
19	GPI0	0.00	–1048.64	0.0000000	–0.0412850
20	GPI1	0.00	–899.00	0.0000000	–0.0353937
21	TEST_EN[3]	0.00	–546.36	0.0000000	–0.0215102
22	RESET_BAR	0.00	–396.72	0.0000000	–0.0156189
23	VDD	0.00	–240.12	0.0000000	–0.0094535
24	DGND1	0.00	–129.92	0.0000000	–0.0051150

Notes:
1. Reference to center of each bond pad from center of bond pad number 1.
2. DNU = do not use. See "Bonding Instructions" on page 2.
3. TEST_EN must be connected to DGND for proper device functionality.

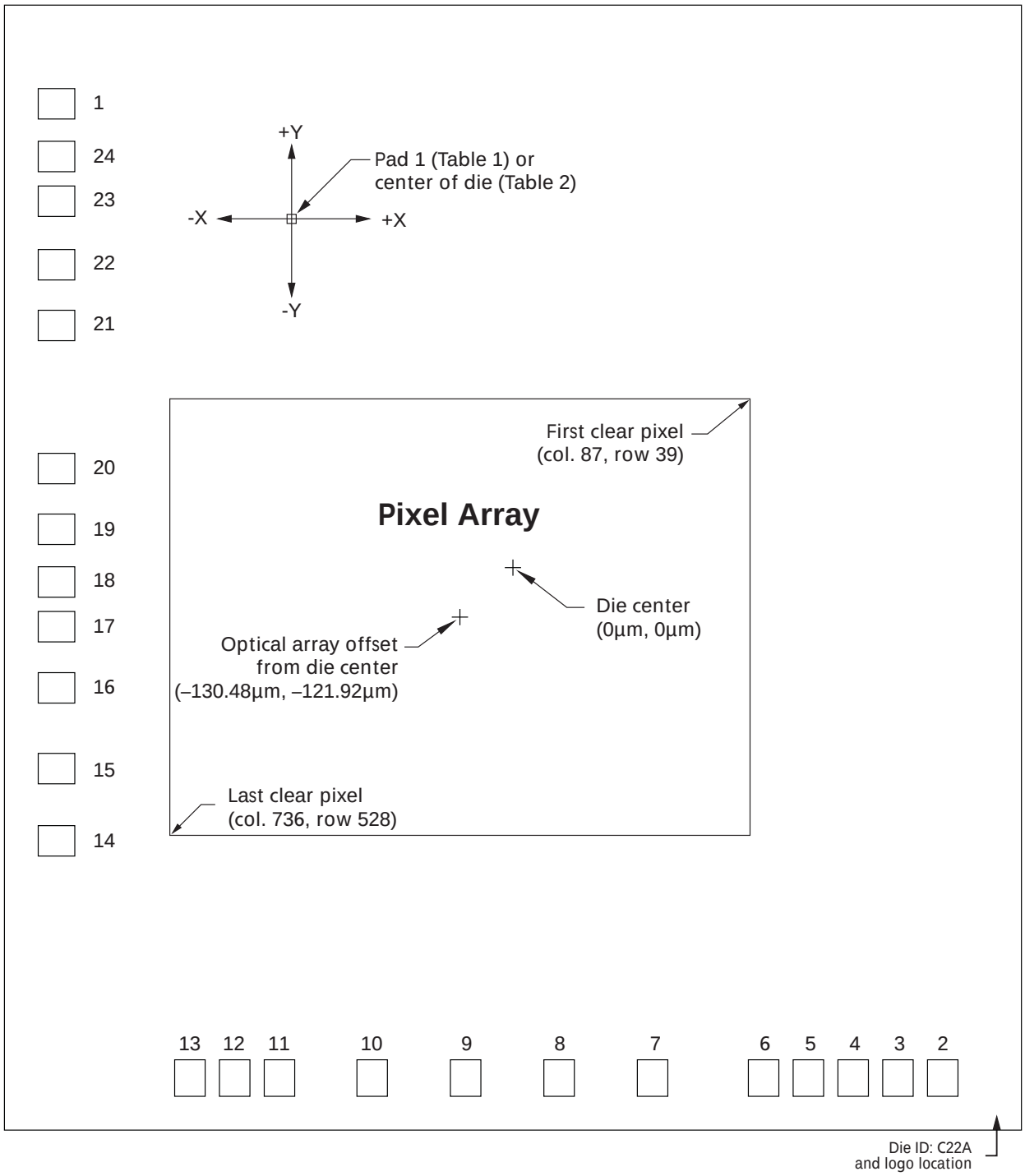
Table 2: MT9V013 Bond Pad Location and Identification from Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	SCLK	–1123.17	1143.18	–0.0442193	0.0450071
2	VAA	1057.63	–1258.02	0.0416390	–0.0495283
3	AGND	947.43	–1258.02	0.0373004	–0.0495283
4	DNU[2]	837.23	–1258.02	0.0329618	–0.0495283
5	DNU	727.03	–1258.02	0.0286232	–0.0495283
6	VAA_PIX	616.83	–1258.02	0.0242846	–0.0495283
7	DATA_N	343.62	–1258.02	0.0135281	–0.0495283
8	DATA_P	113.62	–1258.02	0.0044730	–0.0495283
9	CLK_N	–116.39	–1258.02	–0.0045823	–0.0495283
10	CLK_P	–346.39	–1258.02	–0.0136374	–0.0495283
11	VDD_PHY	–574.49	–1258.02	–0.0226177	–0.0495283
12	GND_PLL	–684.69	–1258.02	–0.0269563	–0.0495283
13	VDD_PLL	–794.89	–1258.02	–0.0312949	–0.0495283
14	EXTCLK	–1123.17	–673.38	–0.0442193	–0.0265110
15	FLASH	–1123.17	–495.32	–0.0442193	–0.0195008
16	SDATA	–1123.17	–296.38	–0.0442193	–0.0116685
17	VDD_IO	–1123.17	–145.58	–0.0442193	–0.0057315
18	DGND2	–1123.17	–35.38	–0.0442193	–0.0013929
19	GPI0	–1123.17	94.54	–0.0442193	0.0037220
20	GPI1	–1123.17	244.18	–0.0442193	0.0096134
21	TEST_EN[3]	–1123.17	596.82	–0.0442193	0.0234969
22	RESET_BAR	–1123.17	746.46	–0.0442193	0.0293882
23	VDD	–1123.17	903.06	–0.0442193	0.0355535
24	DGND1	–1123.17	1013.26	–0.0442193	0.0398921

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 2.
3. TEST_EN must be connected to DGND for proper device functionality.

Die Features

Figure 2: Die Outline (Top View)

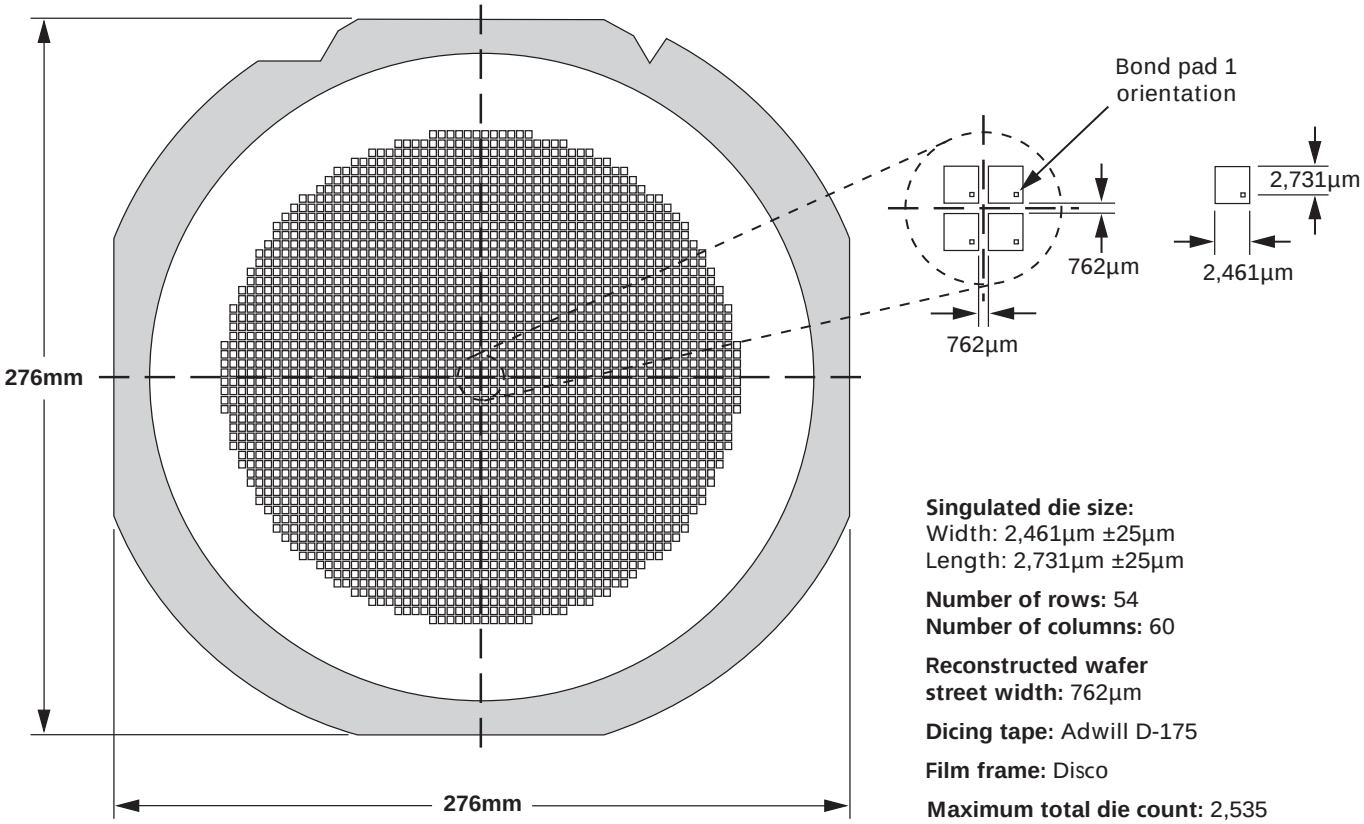


Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Singulated die size *Width:* *Length:*	 2,461µm ±25µm 2,731µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	110.2µm (4.339 mil)
Optical array *Optical array offset from die center:* *Optical array offset from center of pad 1:*	 X = –130.48µm, Y = –121.92µm X = 992.69µm, Y = –1,265.10µm
First clear pixel (col. 87, row 39) *From die center:* *From center of pad 1:*	 X = 583.48µm, Y = 415.94µm X = 1,706.65µm, Y = –727.24µm
Last clear pixel (col. 736, row 528) *From die center:* *From center of pad 1:*	 X = –844.32µm, Y = –659.85µm X = 278.85µm, Y = –1,803.03µm

Figure 3: MT9V013 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 2,461µm ±25µm
Length: 2,731µm ±25µm

Number of rows: 54
Number of columns: 60

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 2,535

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

Rev. D, Production 12/07

- Updated document to production status
- Updated metal thicknesses on page 1
- Updated “Key Performance Parameters” on page 1

Rev. C, Advance 4/07

- Updated Figure 3 on page 9
- Updated template

Rev. B, Advance 1/07

- Added Figure 3, MT9V013 Die Orientation in Reconstructed Wafer, on page 9
- Changed Maximum data rate/master clock bullet to 14 Mp/S at 14 MHz system clock

Rev. A, Advance 11/06

- Initial release