1/2.3-Inch, 9-Megapixel CMOS Active-Pixel Digital Image Sensor Die

MT9N001

For the product data sheet, refer to Micron's Web site: www.micron.com

Features

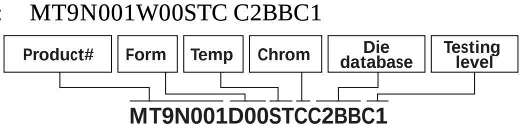
- Micron® DigitalClarity® CMOS imaging technology
- Low dark current
- Simple two-wire serial interface
- Auto black-level calibration
- Support for external mechanical shutter
- Support for external LED or xenon flash
- High frame rate preview mode with arbitrary downsize scaling from maximum resolution
- Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning
- Data interfaces: parallel or serial
  - CCP2-compliant, sub-low-voltage, differential signaling (sub-LVDS)
  - One- or two-lane mobile industry processor interface (MIPI)
- On-die phase-locked loop (PLL) oscillator
- Bayer pattern down-size scaler
- One-time programmable (OTP) memory for storing module information
- Superior low-light performance
- Integrated position-based color and lens shading correction

General Physical Specifications

- Die thickness: 200µm ±12µm
- Wafer thickness: 750µm ±25µm
  (Consult factory for other thickness)
- Backside wafer surface of bare silicon
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 3.1kÅ
- Typical metal 4 thickness: 4.15kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

Die: MT9N001D00STC C2BBC1
Wafer: MT9N001W00STC C2BBC1



Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database C2BB

- Die outline, see Figure 5 on page 14
- Die size (stepping interval): 8,713.85µm x 8,410.55µm
- Singulated die size: 8,672µm ±25µm x 8,369µm ±25µm
- Bond Pad Identification Tables, see pages 8–13

Options

Options	Designator
• Form	
– Die	D
– Wafer	W
• Testing	
– Standard (level 1) probe	C1

Key Performance Parameters

- Optical format: 1/2.3-inch (4:3)
- Active imager size: 6.104mm(H) x 4.578mm(V), 7.630mm diagonal
- Active pixels: 3488H x 2616V
- Pixel size: 1.75µm x 1.75µm
- Chief ray angle: TBD
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS) with global reset release (GRR)
- Input clock frequency: 6–48 MHZ
- Maximum data rate
  - Parallel: 96 Mp/s at 96 MHz PIXCLK
  - CCP2: 640 Mb/s
  - MIPI (two-lane): 1.536 Gb/s
- Frame rate
  - Full resolution: programmable up to 13.2 fps serial, 9.7 fps parallel
  - VGA: 640H x 480V with 2X skip and 2X bin: 74 fps (full power), 50 fps (low power)
- ADC resolution: 12-bit, on-die
- Responsivity: 0.44 V/lux-sec (at 550nm)
- Dynamic range: 62.7dB (preliminary)
- SNR MAX: 37.4dB (preliminary)
- Supply voltage
  - I/O digital: 1.7–1.9V (1.8V nominal) or 2.4–3.1V (2.8V nominal)
  - Digital: 1.7–1.9V (1.8V nominal)
  - Analog: 2.4–3.1V (2.8V nominal)
- Power consumption
  - Full resolution: 485mW
  - Preview: 150mW low power VGA
  - Standby: 50µW (typical, EXTCLK disabled)
- Operating temperature: –30°C to +70°C (at junction)

General Description

The Micron Imaging MT9N001 is a 1/2.3-inch CMOS active-pixel digital image sensor die with an active pixel array of 3488H x 2,616V including border pixels. It incorporates sophisticated on-die camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9N001 digital image sensor die features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

When operated in its default mode, the sensor generates a full resolution image at 13.2 frames per second (fps). An on-die analog-to-digital converter (ADC) generates a 12-bit value for each pixel.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Micron's standard package. Because the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

Specifications provided here are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9N001 imager die has 97 bond pads. Refer to Table 1 and Table 2 on pages 8–13 for a complete list of bond pads and coordinates.

The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figures 1 through 4 on pages 4 through 7 show the typical die connections. For low-noise operation, the MT9N001 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9N001 also supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGND) power domains that can be at different voltages. The PLL requires a clean power source (VDD_PLL).

Storage Requirements

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Micron recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Wafer Saw

The die size (stepping interval) provided is measured from the center of the die street on one side of the die to the center of the die street on the other side of the die. A singulated die is approximately 42µm smaller in length and width. The dimensional tolerance of a singulated die is ±25µm. For example, if the die width (stepping interval) is 5,080µm and the die length (stepping interval) is 7,620µm, the dimensions of the singulated die will be 5,038µm ±25µm by 7,578µm ±25µm.

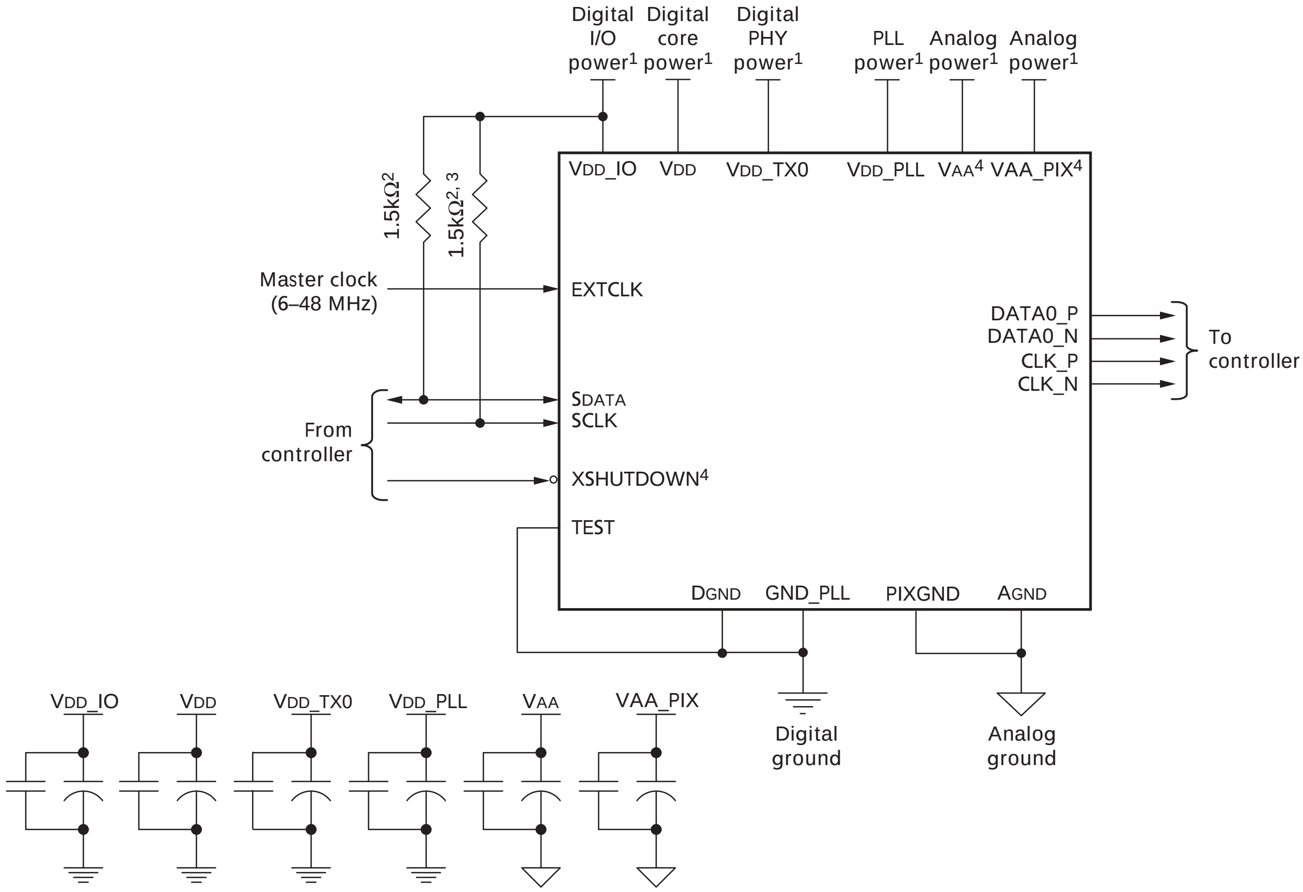
Wafer-Level Processing

Customers should choose the wafer form when post-processing of die is required. This includes adding extra passivation or metal layers or bumping of the bond pads. For these customers, the street widths are provided in the die outline. Also, a reference from the center of bond pad 1 to the center of the intersection of two streets is provided for easy alignment.

Typical Connections

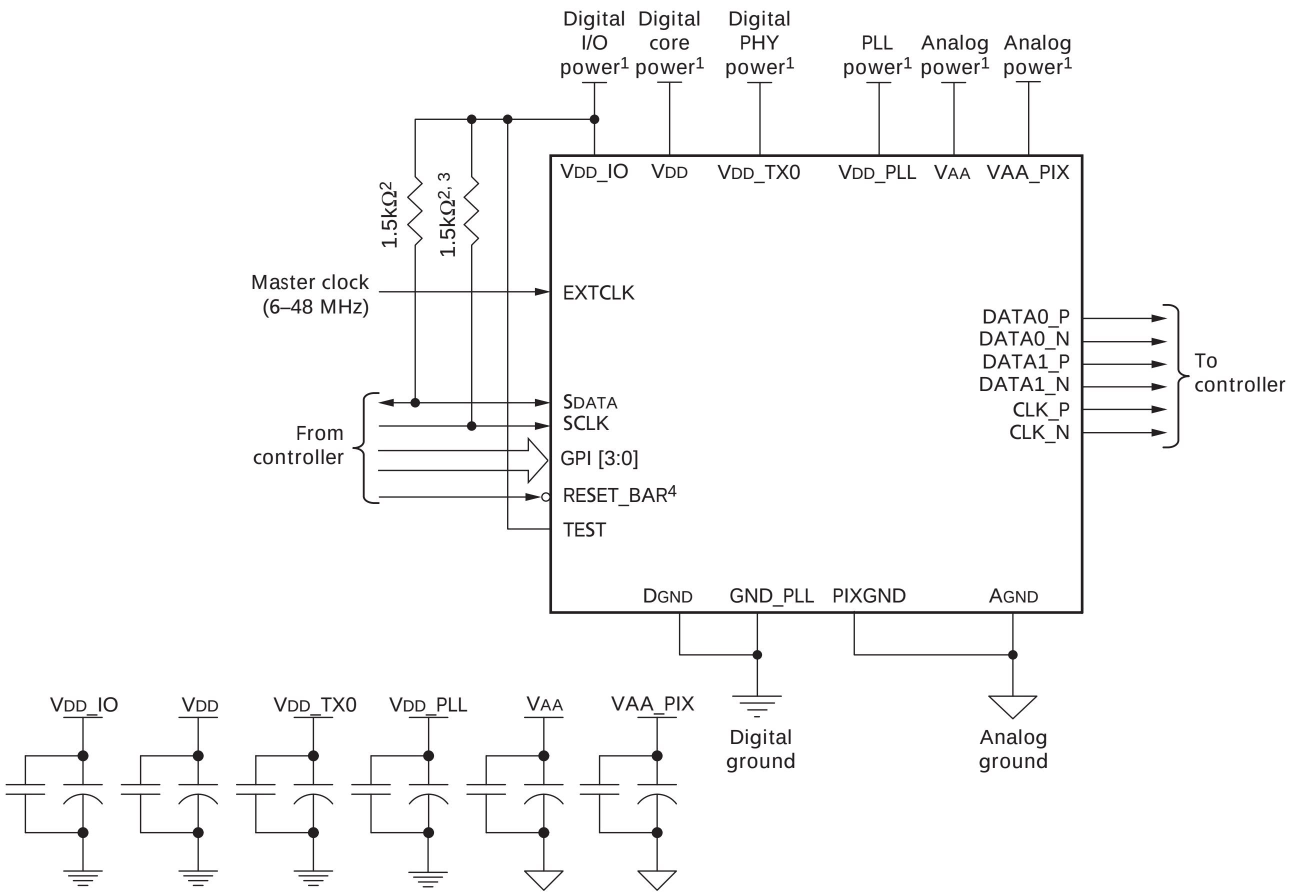
Figures 1 through 4 on pages 4 through 7 show typical configuration schematics for the MT9N001 operating in serial and parallel modes.

Figure 1: Typical Configuration: Serial CCP2 Pixel Data Interface



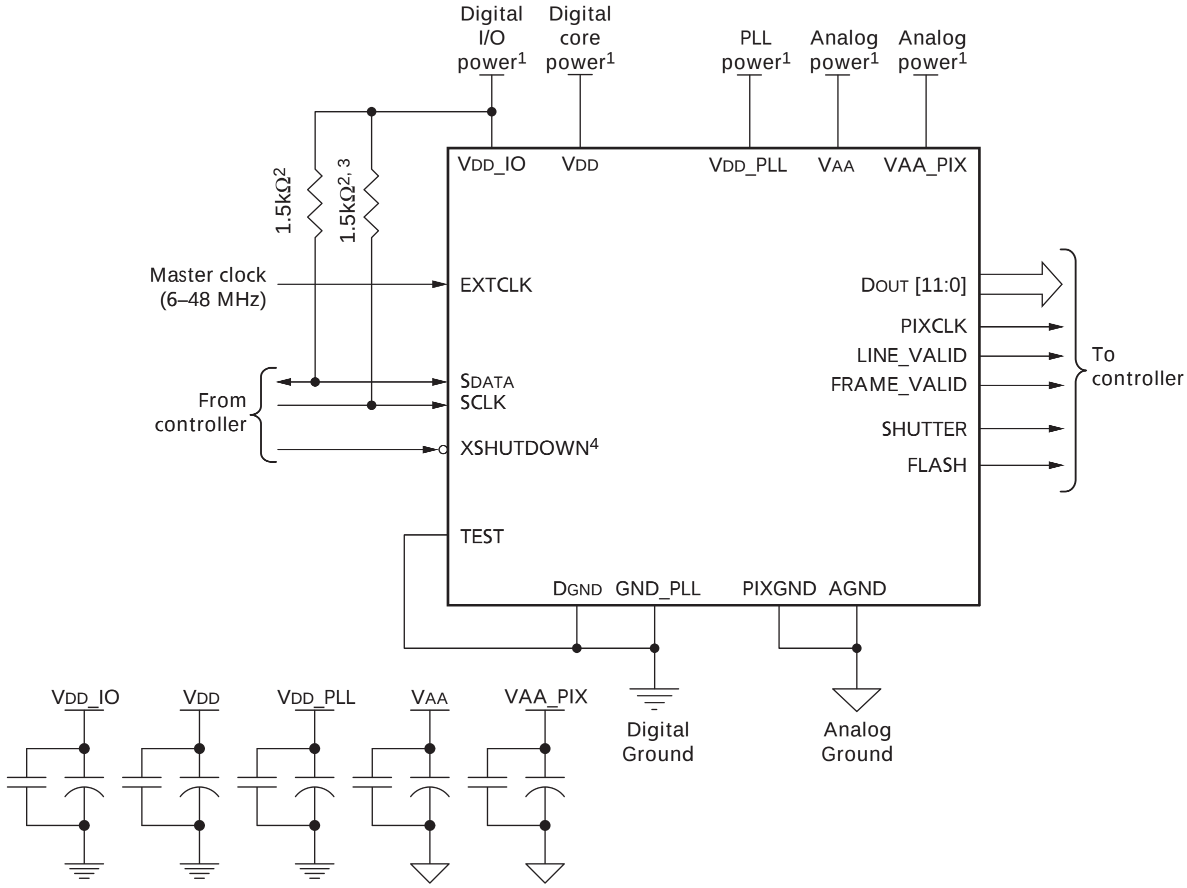
Notes:
1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. Also referred to as RESET_BAR.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 1. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Micron recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Figure 2: Typical Configuration: Serial Two-Lane MIPI Pixel Data Interface



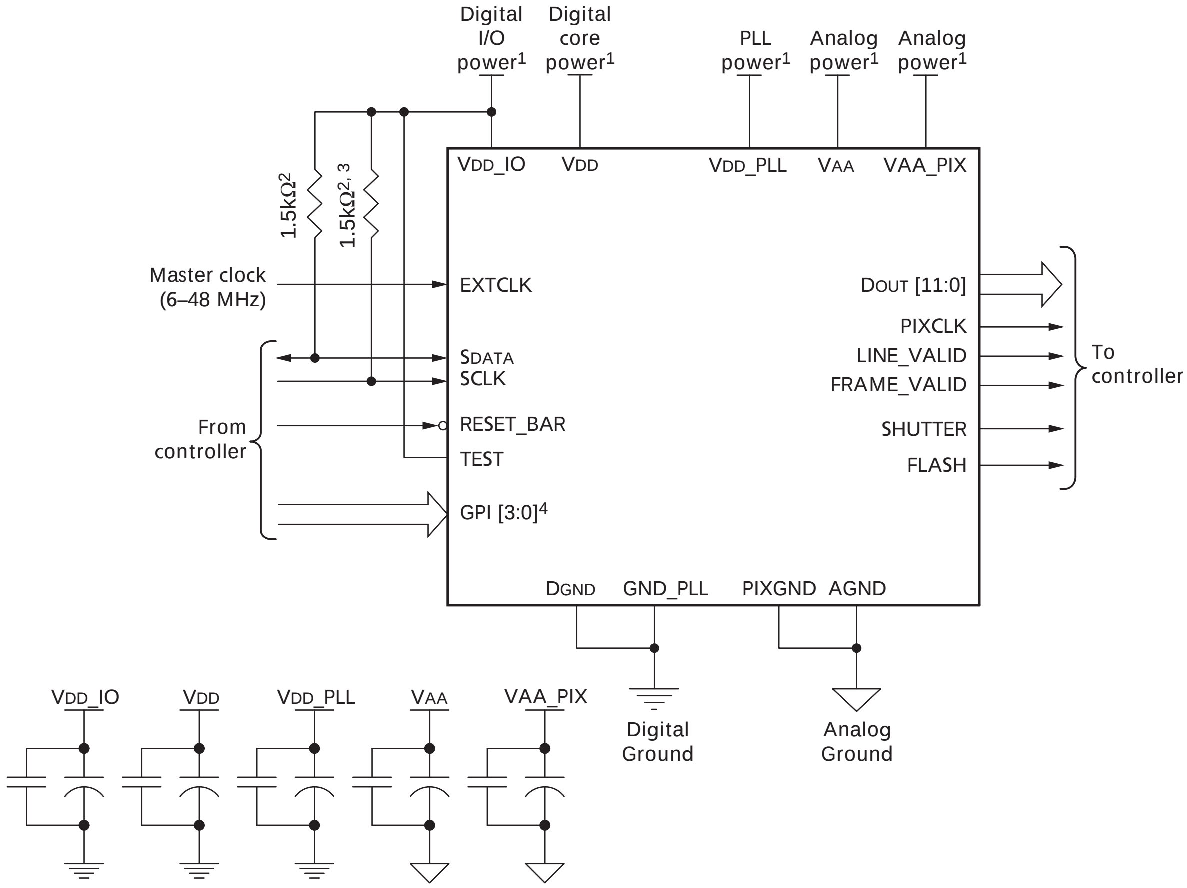
Notes:
1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. Also referred to as XSHUTDOWN.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 2. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Micron recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Figure 3: Typical Configuration: Parallel CCP2 Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. Also referred to as RESET_BAR.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 3. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Micron recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Figure 4: Typical Configuration: Parallel MIPI Pixel Data Interface



Notes:

1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The GPI pins can be statically pulled HIGH or LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_N, SADDR, STANDBY) to be dynamically controlled.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 4. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Micron recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Bond Pad Identification Tables

Table 1: MT9N001 Bond Pad Location From Center of Pad 1

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_IO9	0.00	0.00	0.0000000	0.0000000
2	SDATA	170.53	0.00	0.0067138	0.0000000
3	SCLK	341.05	0.00	0.0134272	0.0000000
4	TEST	511.57	0.00	0.0201406	0.0000000
5	RESET_BAR	682.09	0.00	0.0268539	0.0000000
6	VDD_IO10	1015.01	0.00	0.0399610	0.0000000
7	DGND10	1185.53	0.00	0.0466744	0.0000000
8	VDD5	1356.05	0.00	0.0533878	0.0000000
9	EXTCLK	1526.68	0.00	0.0601053	0.0000000
10	GND_PLL	1697.68	0.00	0.0668378	0.0000000
11	VDD_PLL	1868.19	0.00	0.0735508	0.0000000
12	VDD_TX0	2793.87	0.00	0.1099949	0.0000000
13	CLK_P	3021.97	0.00	0.1189752	0.0000000
14	CLK_N	3251.97	0.00	0.1280303	0.0000000
15	DATA0_P	3481.98	0.00	0.1370856	0.0000000
16	DATA0_N	3711.98	0.00	0.1461407	0.0000000
17	DATA1_P	3941.98	0.00	0.1551961	0.0000000
18	DATA1_N	4171.98	0.00	0.1642512	0.0000000
19	AGND14	8226.73	–224.46	0.3238870	–0.0088370
20	VAA12	8226.73	–394.98	0.3238870	–0.0155504
21	AGND13	8226.73	–565.50	0.3238870	–0.0222638
22	VAA11	8226.73	–736.02	0.3238870	–0.0289772
23	AGND12	8226.73	–906.54	0.3238870	–0.0356906
24	VAA10	8226.73	–1077.06	0.3238870	–0.0424039
25	AGND11	8226.73	–1247.58	0.3238870	–0.0491173
26	VAA9	8226.73	–1418.10	0.3238870	–0.0558307
27	DNU[2]	8226.73	–1588.62	0.3238870	–0.0625441
28	AGND10	8226.73	–1759.14	0.3238870	–0.0692575
29	DNU	8226.73	–1929.66	0.3238870	–0.0759709
30	VAA8	8226.73	–2100.18	0.3238870	–0.0826843
31	AGND9	8226.73	–2270.70	0.3238870	–0.0893976
32	VAA7	8226.73	–3388.36	0.3238870	–0.1334000
33	AGND8	8226.73	–3558.88	0.3238870	–0.1401134
34	PIXGND	8226.73	–3729.40	0.3238870	–0.1468268
35	VAAPIX5	8226.73	–3916.16	0.3238870	–0.1541795
36	VAAPIX4	8226.73	–4086.68	0.3238870	–0.1608929
37	VAAPIX3	8226.73	–4257.20	0.3238870	–0.1676063
38	VAAPIX2	8226.73	–4427.72	0.3238870	–0.1743197
39	VAAPIX1	8226.73	–4598.24	0.3238870	–0.1810331
40	VPP	8226.73	–5533.78	0.3238870	–0.2178654
41	AGND7	8226.73	–5704.30	0.3238870	–0.2245787
42	VAA6	8226.73	–5874.82	0.3238870	–0.2312921
43	AGND6	8226.73	–6045.34	0.3238870	–0.2380055

Table 1: MT9N001 Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	VAA5	8226.73	–6215.86	0.3238870	–0.2447189
45	DNU	8226.73	–6371.88	0.3238870	–0.2508614
46	AGND5	8226.73	–6542.40	0.3238870	–0.2575748
47	DNU	8226.73	–6712.92	0.3238870	–0.2642882
48	VAA4	8226.73	–6883.44	0.3238870	–0.2710016
49	AGND4	8226.73	–7053.96	0.3238870	–0.2777150
50	VAA3	8226.73	–7224.48	0.3238870	–0.2844283
51	AGND3	8226.73	–7395.00	0.3238870	–0.2911417
52	VAA2	8226.73	–7565.52	0.3238870	–0.2978551
53	AGND2	8226.73	–7736.04	0.3238870	–0.3045685
54	VAA1	8226.73	–7906.56	0.3238870	–0.3112819
55	AGND1	8226.73	–8077.08	0.3238870	–0.3179953
56	VDD1	–230.83	–7589.88	–0.0090878	–0.2988142
57	DGND1	–230.83	–7419.36	–0.0090878	–0.2921008
58	VDD_IO1	–230.83	–7248.84	–0.0090878	–0.2853874
59	GPI0	–230.83	–7078.32	–0.0090878	–0.2786740
60	GPI1	–230.83	–6907.80	–0.0090878	–0.2719606
61	GPI2	–230.83	–6737.28	–0.0090878	–0.2652472
62	GPI3	–230.83	–6566.76	–0.0090878	–0.2585339
63	SHUTTER	–230.83	–6388.70	–0.0090878	–0.2515236
64	FLASH	–230.83	–6182.22	–0.0090878	–0.2433945
65	DGND2	–230.83	–6011.70	–0.0090878	–0.2366811
66	VDD_IO2	–230.83	–5841.18	–0.0090878	–0.2299677
67	PIXCLK	–230.83	–5670.66	–0.0090878	–0.2232543
68	FRAME_VALID	–230.83	–5464.18	–0.0090878	–0.2151252
69	LINE_VALID	–230.83	–5257.70	–0.0090878	–0.2069961
70	VDD2	–230.83	–5087.18	–0.0090878	–0.2002827
71	DGND3	–230.83	–4916.66	–0.0090878	–0.1935693
72	VDD_IO3	–230.83	–4746.14	–0.0090878	–0.1868559
73	DOUT6	–230.83	–4575.62	–0.0090878	–0.1801425
74	DOUT5	–230.83	–4369.14	–0.0090878	–0.1720134
75	DGND4	–230.83	–4198.62	–0.0090878	–0.1653000
76	VDD_IO4	–230.83	–4028.10	–0.0090878	–0.1585866
77	DOUT7	–230.83	–3857.58	–0.0090878	–0.1518732
78	DOUT4	–230.83	–3651.10	–0.0090878	–0.1437441
79	DGND5	–230.83	–3480.58	–0.0090878	–0.1370307
80	VDD_IO5	–230.83	–3310.06	–0.0090878	–0.1303173
81	DOUT8	–230.83	–3139.54	–0.0090878	–0.1236039
82	DOUT3	–230.83	–2933.06	–0.0090878	–0.1154748
83	VDD3	–230.83	–2762.54	–0.0090878	–0.1087614
84	DGND6	–230.83	–2592.02	–0.0090878	–0.1020480
85	VDD_IO6	–230.83	–2421.50	–0.0090878	–0.0953346
86	DOUT9	–230.83	–2250.98	–0.0090878	–0.0886213
87	DOUT2	–230.83	–2044.50	–0.0090878	–0.0804921
88	DGND7	–230.83	–1873.98	–0.0090878	–0.0737787

Table 1: MT9N001 Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
89	VDD_IO7	–230.83	–1703.46	–0.0090878	–0.0670654
90	DOUT10	–230.83	–1532.94	–0.0090878	–0.0603520
91	DOUT1	–230.83	–1326.46	–0.0090878	–0.0522228
92	DGND8	–230.83	–1155.94	–0.0090878	–0.0455094
93	VDD_IO8	–230.83	–985.42	–0.0090878	–0.0387961
94	DOUT11	–230.83	–814.90	–0.0090878	–0.0320827
95	DOUT0	–230.83	–608.42	–0.0090878	–0.0239535
96	VDD4	–230.83	–437.90	–0.0090878	–0.0172402
97	DGND9	–230.83	–267.38	–0.0090878	–0.0105268

Notes:
1. Reference to center of each bond pad from center of bond pad number 1.
2. DNU = do not use. See "Bonding Instructions" on page 2.

Table 2: MT9N001 Bond Pad Location From Center of Die (0, 0)

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_IO9	–3997.95	4077.11	–0.1573996	0.1605161
2	SDATA	–3827.42	4077.11	–0.1506858	0.1605161
3	SCLK	–3656.90	4077.11	–0.1439724	0.1605161
4	TEST	–3486.38	4077.11	–0.1372591	0.1605161
5	RESET_BAR	–3315.86	4077.11	–0.1305457	0.1605161
6	VDD_IO10	–2982.94	4077.11	–0.1174386	0.1605161
7	DGND10	–2812.42	4077.11	–0.1107252	0.1605161
8	VDD5	–2641.90	4077.11	–0.1040118	0.1605161
9	EXTCLK	–2471.28	4077.11	–0.0972943	0.1605161
10	GND_PLL	–2300.27	4077.11	–0.0905618	0.1605161
11	VDD_PLL	–2129.76	4077.11	–0.0838488	0.1605161
12	VDD_TX0	–1204.08	4077.11	–0.0474047	0.1605161
13	CLK_P	–975.98	4077.11	–0.0384244	0.1605161
14	CLK_N	–745.98	4077.11	–0.0293693	0.1605161
15	DATA0_P	–515.98	4077.11	–0.0203140	0.1605161
16	DATA0_N	–285.98	4077.11	–0.0112589	0.1605161
17	DATA1_P	–55.97	4077.11	–0.0022035	0.1605161
18	DATA1_N	174.03	4077.11	0.0068516	0.1605161
19	AGND14	4228.78	3852.65	0.1664874	0.1516791
20	VAA12	4228.78	3682.13	0.1664874	0.1449657
21	AGND13	4228.78	3511.61	0.1664874	0.1382524
22	VAA11	4228.78	3341.09	0.1664874	0.1315390
23	AGND12	4228.78	3170.57	0.1664874	0.1248256
24	VAA10	4228.78	3000.05	0.1664874	0.1181122
25	AGND11	4228.78	2829.53	0.1664874	0.1113988
26	VAA9	4228.78	2659.01	0.1664874	0.1046854
27	DNU[2]	4228.78	2488.49	0.1664874	0.0979720
28	AGND10	4228.78	2317.97	0.1664874	0.0912587
29	DNU	4228.78	2147.45	0.1664874	0.0845453
30	VAA8	4228.78	1976.93	0.1664874	0.0778319
31	AGND9	4228.78	1806.41	0.1664874	0.0711185
32	VAA7	4228.78	688.75	0.1664874	0.0271161
33	AGND8	4228.78	518.23	0.1664874	0.0204028
34	PIXGND	4228.78	347.71	0.1664874	0.0136894
35	VAAPIX5	4228.78	160.95	0.1664874	0.0063366
36	VAAPIX4	4228.78	–9.57	0.1664874	–0.0003768
37	VAAPIX3	4228.78	–180.09	0.1664874	–0.0070902
38	VAAPIX2	4228.78	–350.61	0.1664874	–0.0138035
39	VAAPIX1	4228.78	–521.13	0.1664874	–0.0205169
40	VPP	4228.78	–1456.67	0.1664874	–0.0573492
41	AGND7	4228.78	–1627.19	0.1664874	–0.0640626
42	VAA6	4228.78	–1797.71	0.1664874	–0.0707760
43	AGND6	4228.78	–1968.23	0.1664874	–0.0774894
44	VAA5	4228.78	–2138.75	0.1664874	–0.0842028
45	DNU	4228.78	–2294.77	0.1664874	–0.0903453

Table 2: MT9N001 Bond Pad Location From Center of Die (0, 0)

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
46	AGND5	4228.78	–2465.29	0.1664874	–0.0970587
47	DNU	4228.78	–2635.81	0.1664874	–0.1037720
48	VAA4	4228.78	–2806.33	0.1664874	–0.1104854
49	AGND4	4228.78	–2976.85	0.1664874	–0.1171988
50	VAA3	4228.78	–3147.37	0.1664874	–0.1239122
51	AGND3	4228.78	–3317.89	0.1664874	–0.1306256
52	VAA2	4228.78	–3488.41	0.1664874	–0.1373390
53	AGND2	4228.78	–3658.93	0.1664874	–0.1440524
54	VAA1	4228.78	–3829.45	0.1664874	–0.1507657
55	AGND1	4228.78	–3999.97	0.1664874	–0.1574791
56	VDD1	–4228.78	–3512.77	–0.1664874	–0.1382980
57	DGND1	–4228.78	–3342.25	–0.1664874	–0.1315846
58	VDD_IO1	–4228.78	–3171.73	–0.1664874	–0.1248713
59	GPI0	–4228.78	–3001.21	–0.1664874	–0.1181579
60	GPI1	–4228.78	–2830.69	–0.1664874	–0.1114445
61	GPI2	–4228.78	–2660.17	–0.1664874	–0.1047311
62	GPI3	–4228.78	–2489.65	–0.1664874	–0.0980177
63	SHUTTER	–4228.78	–2311.59	–0.1664874	–0.0910075
64	FLASH	–4228.78	–2105.11	–0.1664874	–0.0828783
65	DGND2	–4228.78	–1934.59	–0.1664874	–0.0761650
66	VDD_IO2	–4228.78	–1764.07	–0.1664874	–0.0694516
67	PIXCLK	–4228.78	–1593.55	–0.1664874	–0.0627382
68	FRAME_VALID	–4228.78	–1387.07	–0.1664874	–0.0546091
69	LINE_VALID	–4228.78	–1180.59	–0.1664874	–0.0464799
70	VDD2	–4228.78	–1010.07	–0.1664874	–0.0397665
71	DGND3	–4228.78	–839.55	–0.1664874	–0.0330531
72	VDD_IO3	–4228.78	–669.03	–0.1664874	–0.0263398
73	DOUT6	–4228.78	–498.51	–0.1664874	–0.0196264
74	DOUT5	–4228.78	–292.03	–0.1664874	–0.0114972
75	DGND4	–4228.78	–121.51	–0.1664874	–0.0047839
76	VDD_IO4	–4228.78	49.01	–0.1664874	0.0019295
77	DOUT7	–4228.78	219.53	–0.1664874	0.0086429
78	DOUT4	–4228.78	426.01	–0.1664874	0.0167720
79	DGND5	–4228.78	596.53	–0.1664874	0.0234854
80	VDD_IO5	–4228.78	767.05	–0.1664874	0.0301988
81	DOUT8	–4228.78	937.57	–0.1664874	0.0369122
82	DOUT3	–4228.78	1144.05	–0.1664874	0.0450413
83	VDD3	–4228.78	1314.57	–0.1664874	0.0517547
84	DGND6	–4228.78	1485.09	–0.1664874	0.0584681
85	VDD_IO6	–4228.78	1655.61	–0.1664874	0.0651815
86	DOUT9	–4228.78	1826.13	–0.1664874	0.0718949
87	DOUT2	–4228.78	2032.61	–0.1664874	0.0800240
88	DGND7	–4228.78	2203.13	–0.1664874	0.0867374
89	VDD_IO7	–4228.78	2373.65	–0.1664874	0.0934508
90	DOUT10	–4228.78	2544.17	–0.1664874	0.1001642

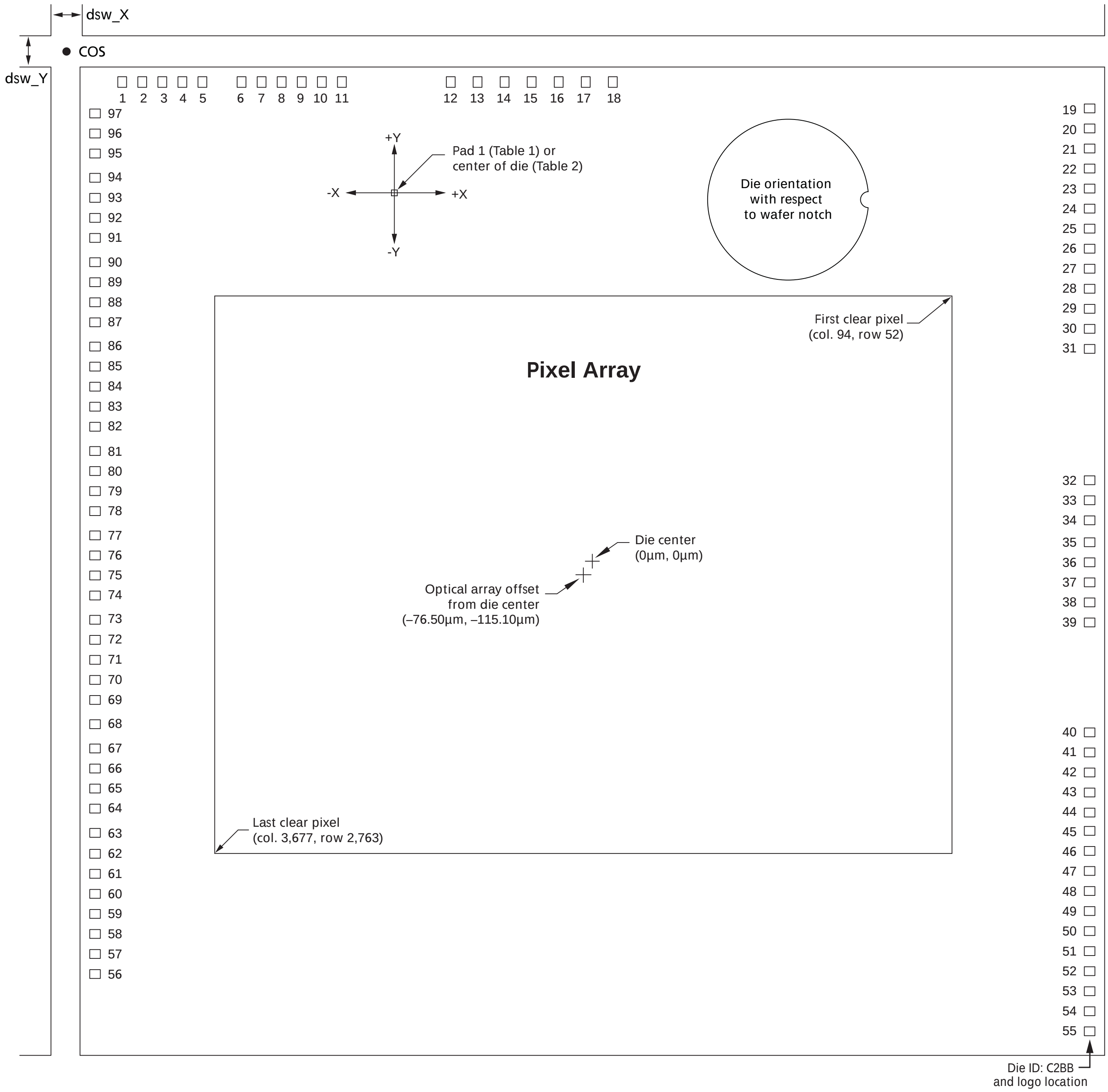
Table 2: MT9N001 Bond Pad Location From Center of Die (0, 0)

Pad	MT9N001	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
91	DOUT1	–4228.78	2750.65	–0.1664874	0.1082933
92	DGND8	–4228.78	2921.17	–0.1664874	0.1150067
93	VDD_IO8	–4228.78	3091.69	–0.1664874	0.1217201
94	DOUT11	–4228.78	3262.21	–0.1664874	0.1284335
95	DOUT0	–4228.78	3468.69	–0.1664874	0.1365626
96	VDD4	–4228.78	3639.21	–0.1664874	0.1432760
97	DGND9	–4228.78	3809.73	–0.1664874	0.1499894

Notes:
1. Reference to center of each bond pad from center of bond pad number 1.
2. DNU = do not use. See "Bonding Instructions" on page 2.

Die Features

Figure 5: Die Outline (Top View)



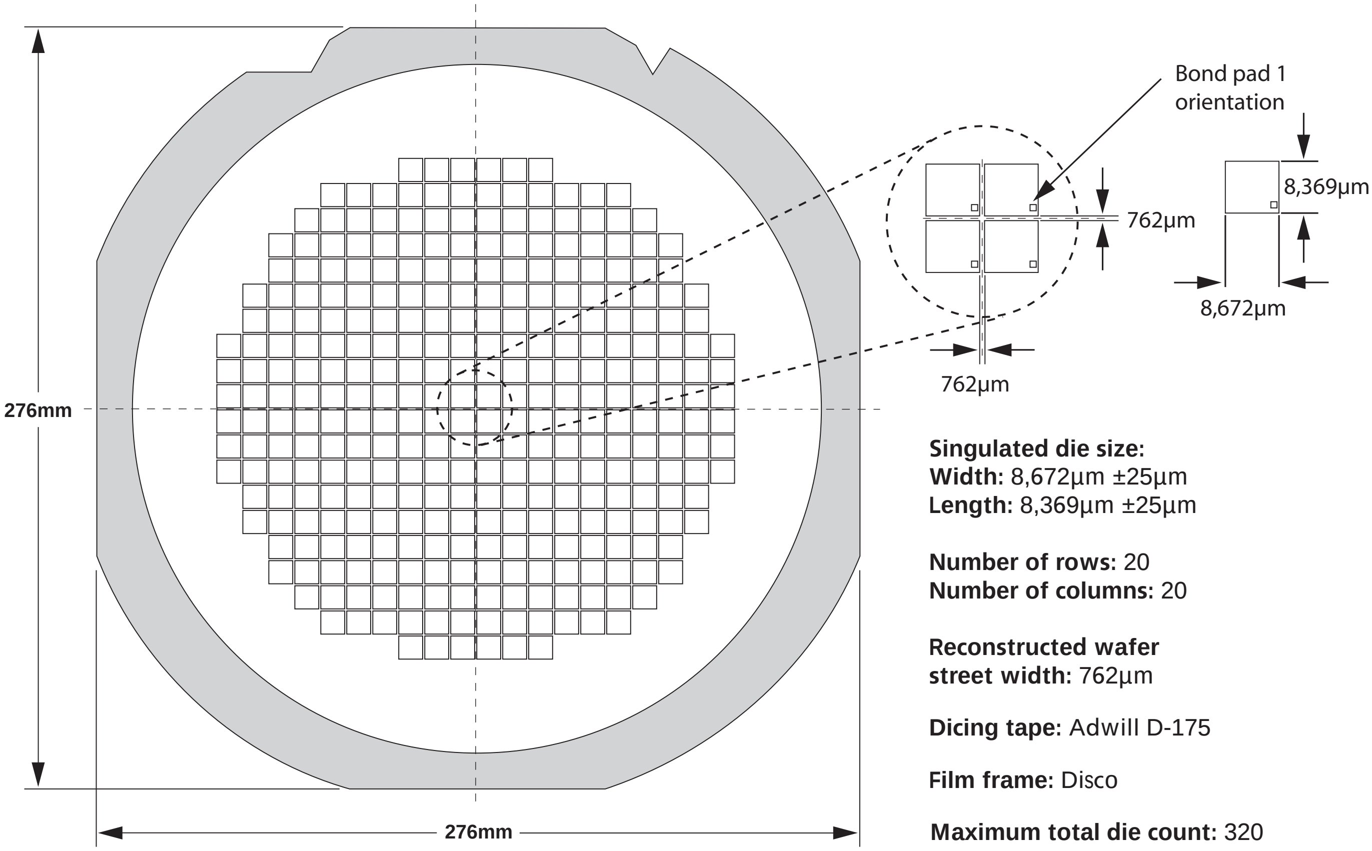
Notes: 1. Die street widths are not drawn to scale.

Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Wafer thickness	750µm ±25µm
Singulated die size (after wafer saw) *Width (X dimension):* *Length (Y dimension):*	 8,672µm ±25µm 8,369µm ±25µm
Die size (stepping interval)	8,713.85µm x 8,410.55µm
Street width along X-axis (dsw_X)	101.65µm
Street width along Y-axis (dsw_Y)	101.65µm
Center of streets (COS) (relative to center of pad 1)	 X = –3581.98µm, Y = 128.17µm
Bond pad size (MIN)	85µm x 100µm
Passivation openings (MIN)	75µm x 90µm
Minimum bond pad pitch	170.52µm
Center of pad 1 to center of die	X = 3,589.90µm, Y = –3,808.28µm
Optical array offset *Optical center from die center:* *Optical center from center of pad 1:*	 X = –76.50µm, Y = –115.10µm X = 3,921.46µm, Y = –4,192.21µm
First clear pixel (col. 94, row 52) *From die center:* *From center of pad 1:*	 X = 3,058.64µm, Y = 2,257.02µm X = 7,056.59µm, Y = –1,820.10µm
Last clear pixel (col. 3,677, row 2,763) *From die center:* *From center of pad 1:*	 X = –3,211.62µm, Y = –2,487.13µm X = 786.34µm, Y = –6,564.24µm
Die offset from center of wafer to center of die (wafer notch at right)	X = –2.999925mm, Y = –-1.435875mm

Figure 6: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 8,672µm ±25µm
Length: 8,369µm ±25µm

Number of rows: 20
Number of columns: 20

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 320

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Revision History

Rev. C, Preliminary **10/5/07**

- Updated "Die Orientation in Reconstructed Wafer" on page 16

Rev. B, Preliminary **9/19/07**

- Update "Features" on page 1
- Update Figure 1: "Typical Configuration: Serial CCP2 Pixel Data Interface," on page 4
- Update Figure 2: "Typical Configuration: Serial Two-Lane MIPI Pixel Data Interface," on page 5
- Update Figure 3: "Typical Configuration: Parallel CCP2 Pixel Data Interface," on page 6
- Update Figure 4: "Typical Configuration: Parallel MIPI Pixel Data Interface," on page 7

Rev. A, Preliminary **8/07**

- Initial release