1/4-Inch High Performance NTSC/PAL Digital Image SOC with Overlay Processor

MT9V136 Data Sheet

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Low-power image sensor with integrated image flow processor (IFP) and video encoder
- 1/4-inch optical format, VGA resolution (640H x 480V)
- ±2.5% additional columns and rows to compensate for lens alignment tolerances
- Overlay generator for dynamic bitmap overlay
- Integrated video encoder for NTSC/PAL with overlay capability and 10-bit I-DAC
- On-chip image flow processor performs sophisticated processing, such as color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, auto white balancing, and auto exposure
- Auto black level calibration
- 10-bit, on-chip analog-to-digital converter (ADC)
- On-chip phase-lock loop (PLL) for serial flash I/F
- Two-wire serial programming interface
- Interface to low cost Flash through SPI bus
- High-level host command interface
- Stand alone operation support
- Comprehensive tool support for overlay generation and lens correction setup
- Development system with DevWare
- Overlay generation and compile tools

Applications

- Analog surveillance CCTV
- Surveillance network IP camera

See "Ordering Information" on page 2

See "New Features" on page 3

Table 1: Key Parameters_1

Parameter	Typical Value
Pixel size and type	5.6µm x 5.6µm active pinned-photodiode with high-sensitivity mode for low-light conditions
Sensor format	680H x 512V (includes ±2.5% of rows and columns for lens alignment)
NTSC output	720H x 480V
PAL output	720H x 576V
Imaging area	Total array size: 3.584mm x 2.688mm
Optical format	¼-inch
Frame rate	50/60 fields/sec
Sensor scan mode	Progressive scan
Color filter array	RGB standard Bayer
Shutter type	Electronic rolling shutter (ERS)
Automatic Functions	Exposure, white balance, black level offset correction, flicker detection and avoidance, color saturation control, on-the-fly defect correction, aperture correction
Programmable Controls	Exposure, white balance, horizontal and vertical blanking, color, sharpness, gamma correction, lens shading correction, horizontal image flip, zoom, windowing, sampling rate, GPIO
Windowing	Programable to any size
Max analog gain	0.5 – 16x
ADC	10-bit, on-chip
Output interface	Analog composite video out, single-ended or differential; 8-, 10-bit parallel digital output
Output data formats[1]	Digital: Raw Bayer 8-,10-bit, CCIR656, 565RGB, 555RGB, 444RGB
Data rate	Parallel: 27 MB/s
	NTSC:60 fields/s
	PAL: 50 fields/s

Key parameters continued on next page.

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Table 2: Key Parameters_2

Parameter		Typical Value
Overlay Support		Utilizes SPI interface to load overlay data from external flash/EEPROM memory with the following features: •Overlay Size 360 x 480 pixel rendered into 720 x 480 pixel display format •Up to four (4) overlays may be blended simultaneously •Selectable readout: Rotating order user selected •Dynamic scenes by loading pre-rendered frames from external memory •Palette of 32 colors out of 64,000 •8 colors per bitmap •Blend factor dynamically programmable for smooth transitions •Fast Update rate of up to 30 fps •Every bitmap object has independent x/y position •Statistic Engine to calibrate optical alignment •Number Generator
Control interface		Two-wire I/F for register interface plus high level command exchange. SPI port to interface to external memory to load overlay data, register settings or firmware extensions.
Input clock for PLL		27 MHz
SPI Clock Frequencies		4.5 - 9.0 - 18 MHz, programmable
Supply voltage		Analog: 2.8V ±5%
		Core: 1.8V ±5%
		IO: 2.8V ±5%
Power consumption		Full resolution at 60 fps: <350mW
Package		48-pin Ceramic LCC, 11.43mm x 11.43mm, 0.5mm pitch
Case temperature		Operating: –30°C to 85°C
		Storage: –50°C to +150°C
Dark Current		< 200e/s at 60°C with a gain of 1
Fixed pattern noise	Column	< 2percent
	Row	< 2percent
Sensitivity		> 11.5 V/lux-s at 550nm
Signal to noise ratio (S/N)		>45dB
Pixel dynamic range		> 80dB

Note: Only CCIR656 format allows lens correction and overlays.

Ordering Information

Table 3: Available Part Numbers

Part Number	Description
MT9V136C12STC	CLCC Production part number
MT9V136C12STC ES	CLCC ES part number
MT9V136D00STC K22BC1 ES	Die Production part number
MT9V136D00STC K22BC1 ES	Die ES part number
MT9V136C12STCD ES	Demo kit
MT9V136C12STCH ES	Head Board

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New Features

Integrated Video Encoder for PAL/NTSC with Overlay Capability

- Composite analog output (NTSC/PAL)
- 8-bit parallel digital output ITU-R BT.656 format
- Raw Bayer format

On-Chip Overlay Generator

- Static and dynamic overlay graphics with four overlay planes plus “number” plane
- Support for serial SPI memory up to 16MBit
- Number generator
- Overlay blending and x/y positioning
- Overlay position adjustment and statistics engine to calibrate overlay
  - Overlay support utilizes SPI interface to load overlay
- EEPROM/Flash memory for achieving the following features:
  - Overlay size 360 x 480 pixel rendered into 720 x
  - Up to four overlays may be blended simultaneously
  - Selectable readout: rotating order user selected
  - Dynamic scenes by loading pre-rendered frames
  - Palette of 32 colors out of 64,000
  - Eight colors per bitmap
  - Blend factor dynamically programmable for smooth
  - Fast update rate of up to 30 fps
  - Every bitmap object has independent x/y position
  - Statistics engine to calibrate optical alignment

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General Description

The Aptina® Imaging MT9V136 is a VGA-format, single-chip active-pixel digital image sensor for surveillance applications. It captures high-quality color images at VGA resolution and outputs NTSC or PAL interlaced composite video.

The VGA image sensor features DigitalClarity®–Aptina's breakthrough low-noise imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of Aptina's advanced active pixel CMOS process technology.

The MT9V136 is a complete camera-on-a-chip. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface or by an attached SPI Flash memory that contains setup information automatically at startup.

The MT9V136 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction.

The MT9V136 outputs interlaced-scan images at 30 or 25 fps, supporting both NTSC and PAL video formats. The image data can be output on one or two output ports:

- Composite analog video (single-ended and differential output support)
- Parallel 8-, 10-bit digital

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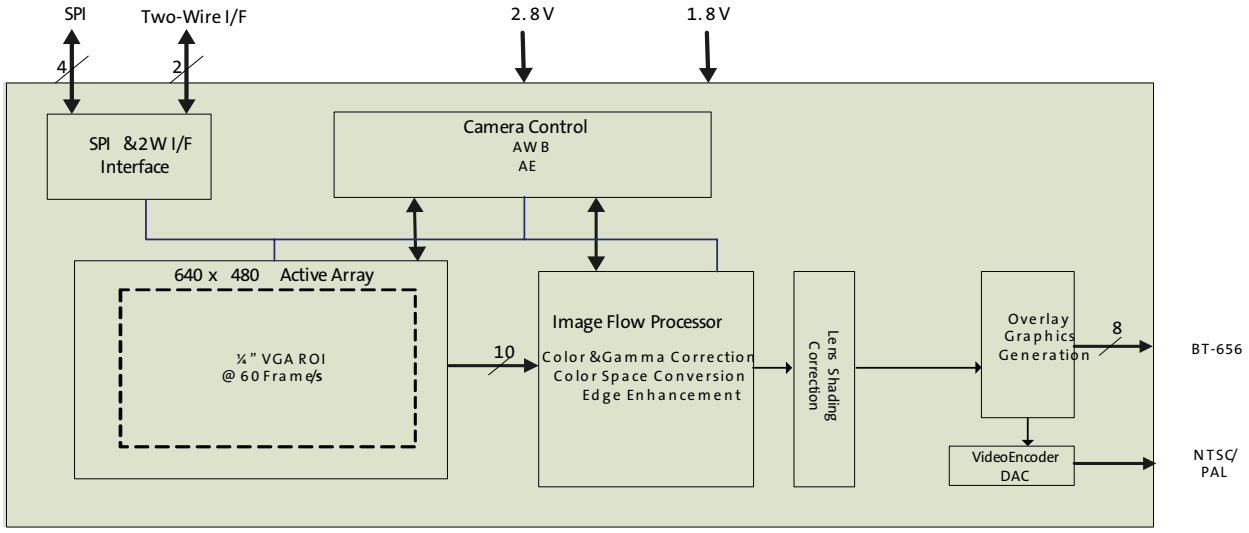
Architecture

Internal Block Diagram

Figure 1: Internal Block Diagram



Note: The active array is smaller than the sensor array.

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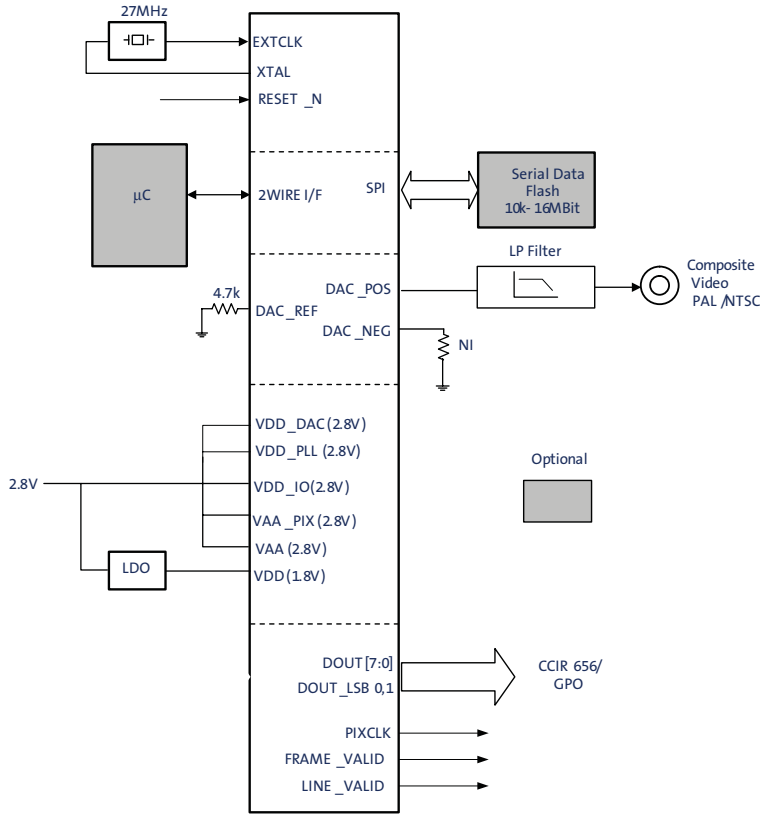
System Block Diagram

The system block diagram will depend on the application. The system block diagram in Figure 2 shows all components; optional peripheral components are highlighted. The optional microcontroller controls MT9V136 sensor using the two-wire serial bus. Optional components will vary by application. For further details, see "Register Summary" on page 50.

Figure 2: System Block Diagram



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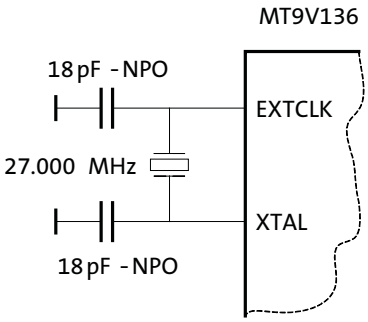
Crystal Usage

As an alternative to using an external oscillator, a fundamental 27 MHz crystal may be connected between EXTCLK and XTAL. Two small loading capacitors of 15–33pF of NPO dielectric should be added as shown in Figure 3.

Aptina does not recommend using the crystal option for surveillance applications above 85°C. A crystal oscillator with temperature compensation is recommended.

Figure 3: Using a Crystal Instead of an External Oscillator



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Pin Descriptions and Assignments

Table 4: Pin Descriptions

Pin Number	Pin Name	Type	Description
			Clock and Reset
9	CLKIN	Input	Master input clock (27MHz): This either can be a square-wave generated from an oscillator (in which case the XTAL input must be left unconnected) or connected directly to a crystal.
10	XTAL	Output	If CLKIN is connected to one pin of a crystal, this signal is connected to the other pin; otherwise this signal must be left unconnected.
12	RESET_N	Input	Asynchronous active-low reset: When asserted, the device will return all interfaces to their reset state. When released, the device will initiate the boot sequence.
			Register Interface
17	SCLK	Input	These two signals implement serial communications protocol for access to the internal register set and memory.
18	SDATA	Input/OD	
16	SADDR	Input	This signal controls the device ID that will respond to serial communication commands. Two-wire serial interface device ID selection: 0: 0x90 1: 0xBA
			SPI Interface
22	SPI_SCLK	Output	Clock output for interfacing to an external SPI memory such as Flash/EEPROM. Tristated when RESET_N is asserted.
21	SPI_SDI	Input	Data in from SPI device. This signal has an internal pull-up resistor.
20	SPI_SDO	Output	Data out to SPI device. Tristated when RESET_N is asserted.
19	SPI_CS_N	Output	Chip selects to SPI device. Tristated when RESET_N is asserted.
			(Parallel) Pixel Data Input
32	FRAME_VALID	Output	Pixel data from the MT9V136 can be routed out on this interface and processed externally. To save power, these signals are driven to a constant logic level unless the parallel pixel data output or alternate (GPIO) function is enabled for these pins. This interface is disabled by default. The slew rate of these outputs is programmable. These signals can also be used as general purpose input/outputs.
31	LINE_VALID	Output	
33	PIXCLK	Output	
39, 40, 41, 42, 43, 44, 45, 46	DOUT[7:0]	Output	
38	DOUT_LSB1	Output	When the sensor core is running in bypass mode, it will generate 10 bits of output data per pixel. These two pins make the two LSB of pixel data available externally. Leave unconnected if not used. To save power, these signals are driven to a constant logic level unless the sensor core is running in bypass mode or the alternate function is enabled for these pins. The slew rate of these outputs is programmable.
37	DOUT_LSB0	Output/Input	
			Composite Video Output
6	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single-ended mode. This interface is enabled by default using NTSC/PAL signalling. For applications where composite video output is not required, the video DAC can be placed in a power-down state under software control.
4	DAC_NEG	Output	Negative video DAC output in differential mode. Connect to AGND in single-ended mode.
2	DAC_REF	Output	External reference resistor for the video DAC.

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Table 4: Pin Descriptions (continued)

Pin Number	Pin Name	Type	Description
Manufacturing Test Interface			
27	TDI	Input	JTAG Test pin (Reserved for Test Mode)
26	TDO	Output	JTAG Test pin (Reserved for Test Mode)
25	TMS	Input	JTAG Test pin (Reserved for Test Mode)
24	TCK	Input	JTAG Test pin (Reserved for Test Mode)
23	TRST_N	Input	Connect to GND
Power			
8, 14, 35, 48	DGND	Supply	Digital ground.
3	GND_DAC	Supply	Video DAC GND
1, 7, 15, 34	VDD	Supply	Supply for VDD core: 1.8V nominal.
13, 36, 47	VDD_IO	Supply	Supply for digital IOs: 2.8V nominal.
5	VDD_DAC	Supply	Supply for video DAC: 2.8V nominal.
11	VDD_PLL	Supply	Supply for PLL: 2.8V nominal.
29	AGND	Supply	Analog ground.
28	VAA	Supply	Analog power: 2.8V nominal.
30	VAA_PIX	Supply	Analog pixel array power: 2.8V nominal. Must be at same voltage potential as VAA.

Pin Assignments

Figure 4: Pin Assignments

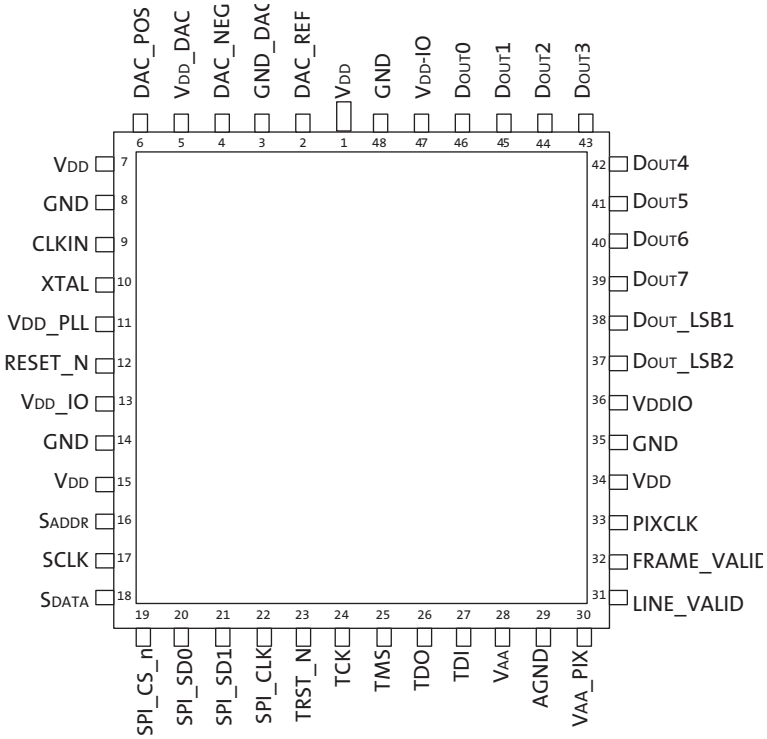

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Table 5: Reset/Default State of Interfaces

Name	Reset State	Default State	Notes
EXTCK	(clock running or stopped).	(clock running).	Input
XTAL	N/A	N/A	Input
RESET_N	(asserted)	(negated).	Input
SCLK	N/A	N/A	Input. Must always be driven to a valid logic level.
SDATA	High-impedance.	High Impedance.	Input/Output. A valid logic level should be established by pull-up resistor.
SADDR	N/A	N/A	Input. Must always be driven to a valid logic level. Should be permanently tied to VDD_IO or GND.
SPI_SCLK	High-impedance.	Driven, logic 0.	Output. Output enable is R0x0032[9].
SPI_SDI	Internal pull-up enabled.	Internal pull-up enabled.	Input. Internal pull-up permanently enabled.
SPI_SDO	High-impedance.	Driven, logic 0.	Output enable is R0x0032[9].
SPI_CS_N	High-impedance.	Driven, logic 1.	Output enable is R0x0032[9].
FRAME_VALID	High Impedance.	High Impedance.	Input/Output. Interface disabled by default. Input buffers (used for GPIO function) powered-down by default, so these pins can be left unconnected (floating). After reset these pins are powered-up, sampled then powered-down again as part of the auto-configuration mechanism. See Note 2.
LINE_VALID			
PIXCLK	High Impedance.	Driven, logic 0.	Output. Interface disabled by default. See Note 1.
DOUT7			
DOUT6			
DOUT5			
DOUT4			
DOUT3			
DOUT2			
DOUT1			
DOUT0			
DOUT_LSB1	High Impedance.	High Impedance.	Input/Output. Interface disabled by default. Input buffers (used for GPIO function) powered-down by default, so these pins can be left unconnected (floating). After reset these pins are powered-up, sampled then powered-down again as part of the auto-configuration mechanism. See Auto-Configuration in Usage Mode.
DOUT_LSB0	High Impedance.	Driven, logic 0.	
DAC_POS	High Impedance.	Driven.	Output. Interface disabled by hardware reset and enabled by default when the device starts streaming.
DAC_NEG			
DAC_REF			
TDI	Internal pull-up enabled.	Internal pull-up enabled.	Input. Internal pull-up means that this pin can be left unconnected (floating).
TDO	High Impedance.	High Impedance.	Output. Only driven during appropriate parts of the JTAG shifter sequence.

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Table 5: Reset/Default State of Interfaces (continued)

Name	Reset State	Default State	Notes
TMS	Internal pull-up enabled.	Internal pull-up enabled.	Input. Internal pull-up means that this pin can be left unconnected (floating).
TCK	Internal pull-up enabled.	Internal pull-up enabled.	Input. Internal pull-up means that this pin can be left unconnected (floating).
TRST_N	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND to for normal operation.

Notes:
1. The reason for defining the default state as logic 0 rather than high-impedance is this: when wired in a system (for example, on our demo boards), these outputs will be connected, and the inputs to which they are connected will want to see a valid logic level. No current drain should result from driving these to a valid logic level (unless there is a pull-up at the system level).
2. In Rev2 silicon and Rev1 silicon, these pads have their input circuitry powered down, but they are not output-enabled. Therefore, they can be left floating but they will not drive a valid logic level to an attached device.

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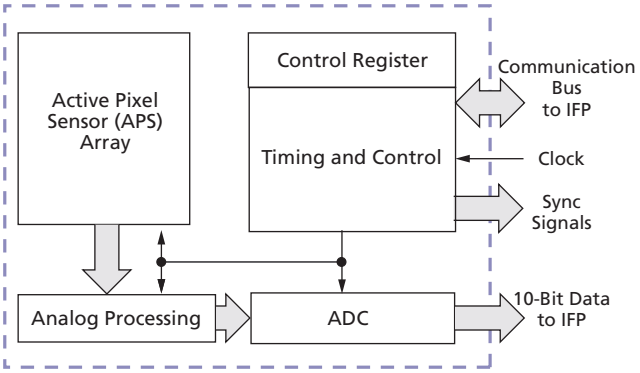
SOC Description

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array, an analog readout chain, a 10-bit ADC with programmable gain and black offset, and timing and control as illustrated in Figure 5.

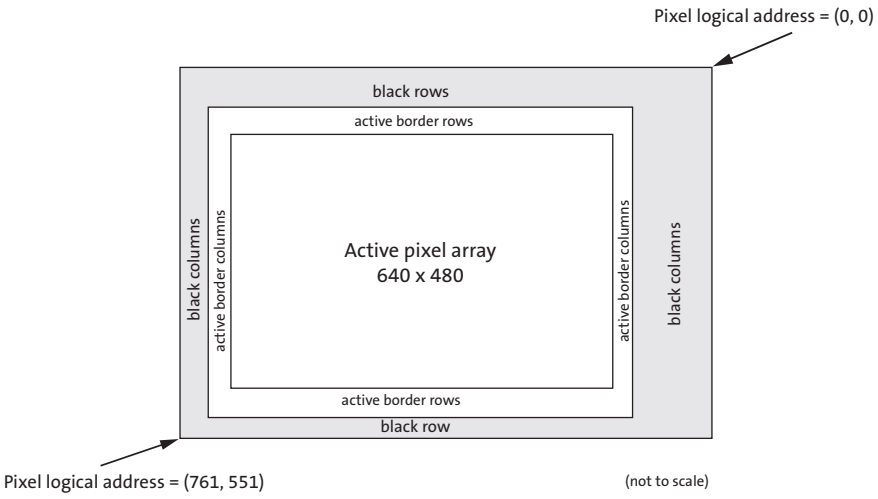
Figure 5: Sensor Core Block Diagram



Pixel Array Structure

The sensor core pixel array is configured as 672 columns by 520 rows, as shown in Figure 6. This includes black rows and columns.

Figure 6: Pixel Array Description



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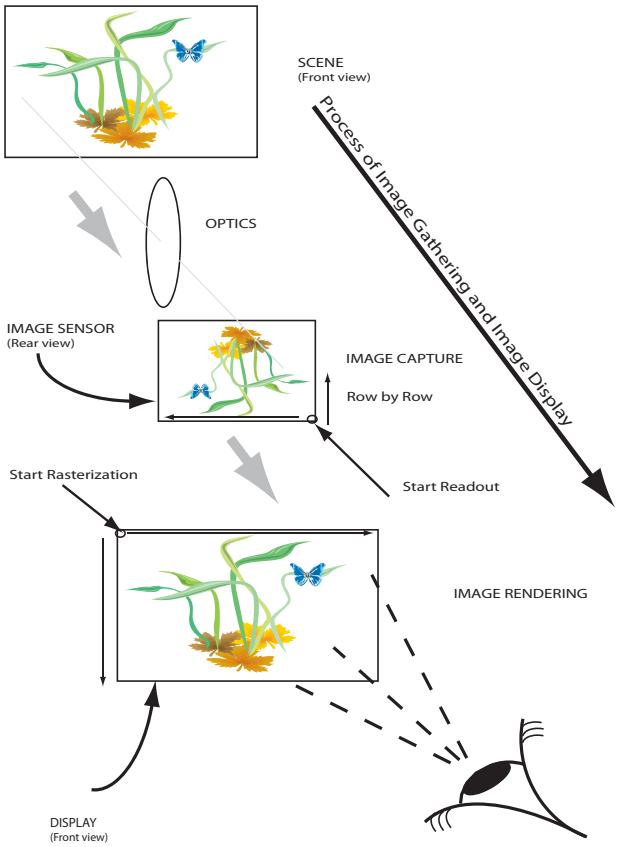
The black row data are used internally for the automatic black level adjustment. However, these black rows can also be read out by setting the sensor to raw data output mode.

There are 762 columns by 552 rows of optically-active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

The one additional active column and two additional active rows are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 7 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right corner. The image is presented in true orientation by the output display.

Figure 7: Image Capture Example



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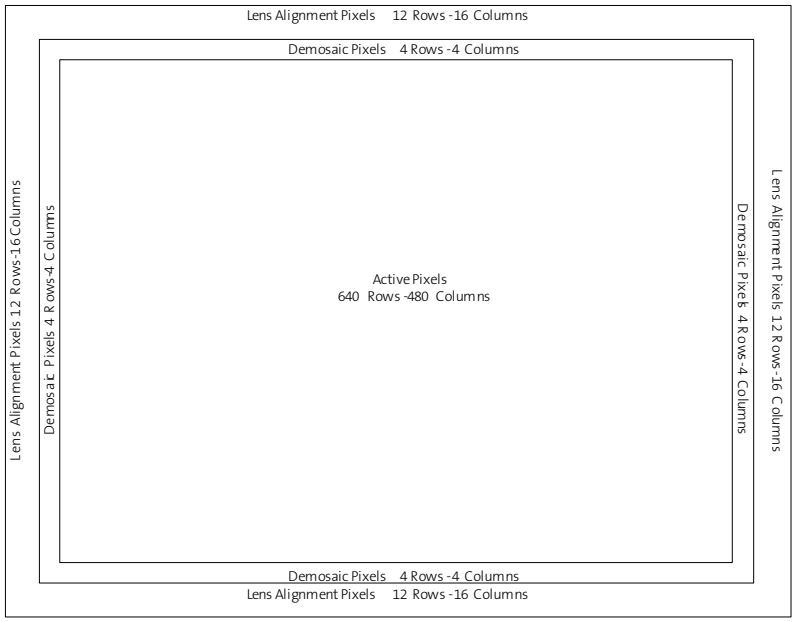
Sensor Pixel Array

The active pixel array is 640 x 480 pixels. In addition, there are rows and columns for lens alignment and demosaic.

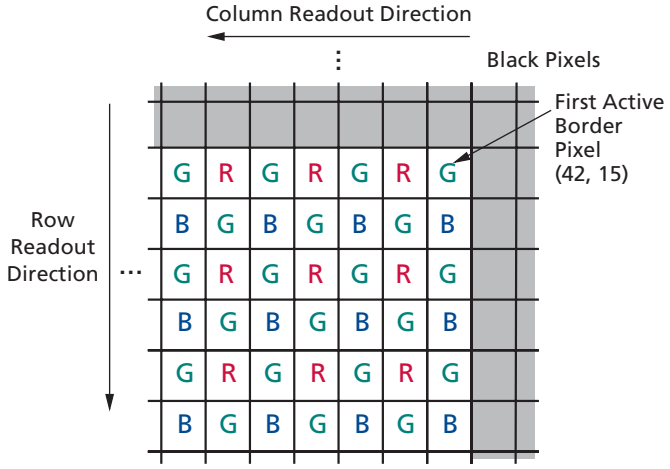
The sensor is sampled twice for every video frame. Not shown in Figure 8 are pixels for black level calibration.

Figure 8: Sensor Pixel Array



The range of adjustment is from Row 0 to 22 and Column 0 to 30. There are 4 rows/ columns needed to calculate the RGB values. The window should be moved only at even numbers.

Figure 9: Pixel Color Pattern Detail (Top Right Corner)



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Output Data Format

The sensor core image data are read out in progressive scan order. Valid image data are surrounded by horizontal and vertical blanking, shown in Figure 10.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field.

Figure 10: Spatial Illustration of Image Readout

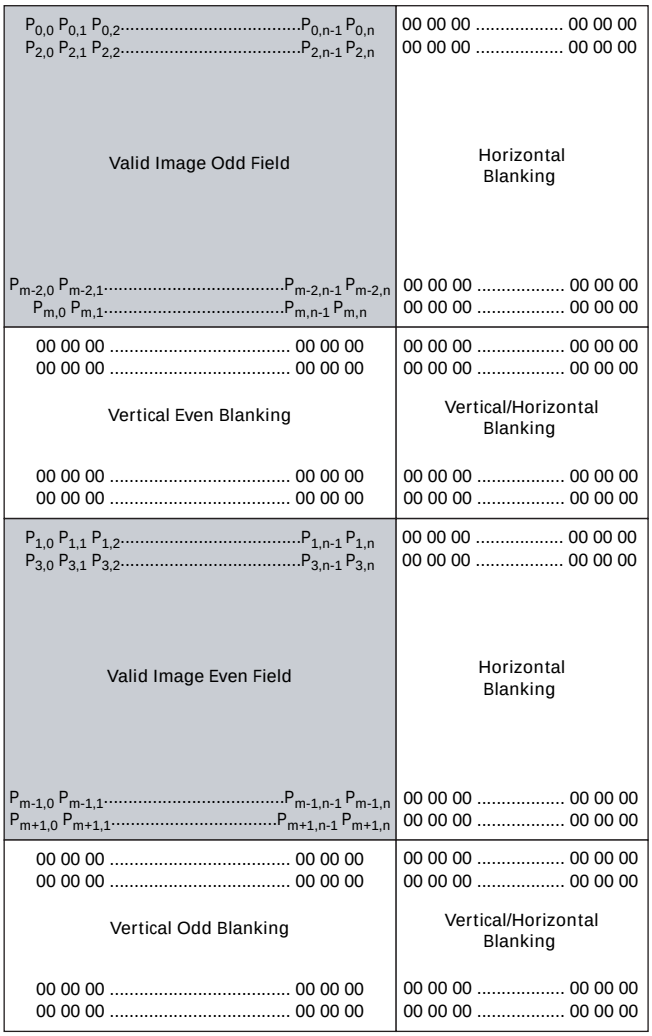

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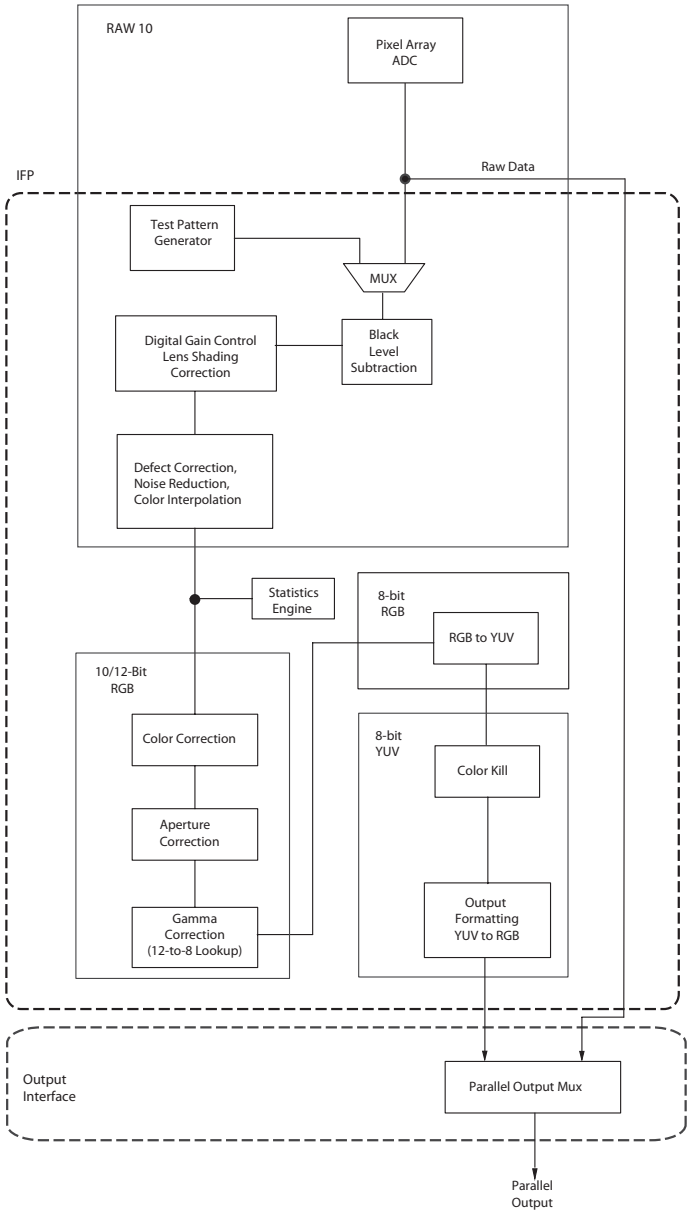
Image Flow Processor

Image and color processing in the MT9V136 are implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operation parameters. The IFP is broken down into different sections, as outlined in Figure 11.

Figure 11: Color Pipeline



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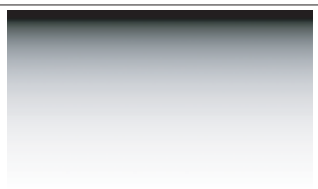
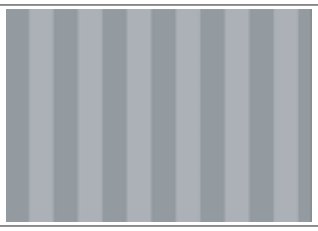
Test Patterns

During normal operation of the MT9V136, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

Test patterns are accessible by programming a register and are shown in Figure 12. Disabling the MCU is recommended before enabling test patterns.

Figure 12: Color Bar Test Pattern

Test Pattern	Example
Flat Field	
Vertical Ramp	
Color Bar	
Vertical Stripes	
Pseudo-Random	

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NTSC/PAL Test Pattern Generation

There is a built-in standard EIA (NTSC) and EBU (PAL) color bars to support hue and color saturation characterization. Each pattern consists of seven color bars (white, yellow, cyan, green, magenta, red, and blue). The Y, Cb and Cr values for each bar are detailed in Tables 6 and 7.

The test pattern is invoked through a Host Command call to the TX Manager. See the MT9V126/MT9V136 Host Command Specification.

Figure 13: Color Bars

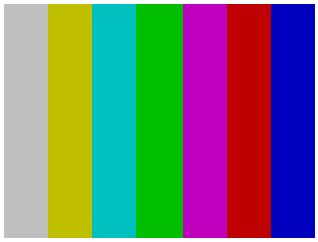

Table 6: EIA Color Bars (NTSC)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	180	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

Table 7: EBU Color Bars (PAL)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	235	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

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CCIR-656 Format

The color bar data is encoded in 656 data streams. The duration of the blanking and active video periods of the generated 656 data are summarized in Table 8 and Table 9.

Table 8: NTSC

Line Numbers	Field	Description
1-3	2	Blanking
4-19	1	Blanking
20-263	1	Active video
264-265	1	Blanking
266-282	2	Blanking
283-525	2	Active Video

Table 9: PAL

Line Numbers	Field	Description
1-22	1	Blanking
23-310	1	Active video
311-312	1	Blanking
313-335	2	Blanking
336-623	2	Active video
624-625	2	Blanking

Black Level Subtraction and Digital Gain

Image stream processing starts with black level subtraction and multiplication of all pixel values by a programmable digital gain. Both operations can be independently set to separate values for each color channel (R, Gr, Gb, B). Independent color channel digital gain can be adjusted with registers. Independent color channel black level adjustments can also be made. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to "0."

Automatic Positional Gain Adjustments (APGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The MT9V136 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

In some cases, different lighting conditions can introduce different color shading response. To compensate for the dependency of the lens shading to the illuminant that can result, different settings of lens shading correction (LC) coefficients can be used. The MT9V136 provides up to three settings to be stored. Each PGA setting should be optimized at a particular color temperature. In the MT9V136, color temperature is detected, stored in the firmware variable ccmPosition, and an appropriate PGA setting is applied.

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The variable (ccmPosition) has a range from 0 through 255 and reflects the current color temperature, 0 corresponding to lowest color temperature, 255 the highest. The host specifies a range of ccmPosition values for a particular PGA setting. The ranges should overlap to provide hysteresis and prevent thrashing between PGA settings.

The Correction Function

For each illuminant, color-dependent solutions are calibrated using the sensor, lens system, and an image of an evenly illuminated, featureless gray calibration field. From the resulting image, the color correction functions can be derived.

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row,col) = P_{sensor}(row,col) * f(row,col) \quad \text{(EQ 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer number, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10-bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12-bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through register settings.

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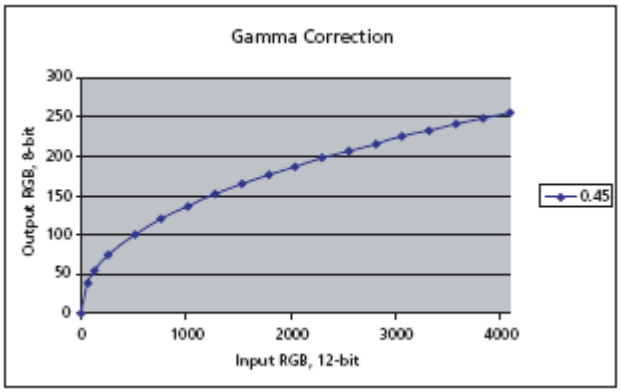
Gamma Correction

The MT9V136 IFP includes a block for gamma correction that can adjust its shape based on brightness to enhance the performance under certain lighting conditions .Two custom gamma correction tables may be uploaded corresponding to a brighter lighting condition and a darker lighting condition. At power-up, the IFP loads the two tables with default values. The final gamma correction table used depends on the brightness of the scene and takes the form of an interpolated version of the two tables.

The gamma correction curve (as shown in Figure 14) is implemented as a piecewise linear function with 19 knee points, taking 12-bit arguments and mapping them to 8-bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096. The 8-bit ordinates are programmable through IFP registers.

Figure 14: Gamma Correction Curve



RGB to YUV Conversion

For further processing, the data is converted from RGB color space to YUV color space.

Color Kill

To remove high or low light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one-dimensional low-pass filtering of Y and/or UV signals is possible. A 3- or 5-tap filter can be selected for each signal.

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YUV-to-RGB/YUV Conversion and Output Formatting

The YUV data stream emerging from the scaling module can either exit the color pipeline as-is or be converted before exit to an alternative YUV or RGB data format.

Output Format and Timing

YUV/RGB Data Ordering

The MT9V136 supports swapping YCrCb mode, as illustrated in Table 10.

Table 10: YCrCb Output Data Ordering

Mode	Data Sequence			
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

The RGB output data ordering in default mode is shown in Table 11. The odd and even bytes are swapped when luma/chroma swap is enabled. R and B channels are bit-wise swapped when chroma swap is enabled.

Table 11: RGB Ordering in Default Mode

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$
555RGB	Odd	$0\ R_7R_6R_5R_4R_3G_7G_6$
	Even	$G_5G_4G_3B_7B_6B_5B_4B_3$
444xRGB	Odd	$R_7R_6R_5R_4G_7G_6G_5G_4$
	Even	$B_7B_6B_5B_4\ 0\ 0\ 0\ 0$
x444RGB	Odd	$0\ 0\ 0\ 0\ R_7R_6R_5R_4$
	Even	$G_7G_6G_5G_4B_7B_6B_5B_4$

Uncompressed 10-Bit Bypass Output

Raw 10-bit Bayer data from the sensor core can be output in bypass mode in two ways:

- Using 8 data output signals (DOUT[7:0]) and GPIO[1:0]. The GPIO signals are the least significant 2 bits of data.
- Using only 8 signals (DOUT[7:0]) and a special 8 + 2 data format, shown in Table 12.

Table 12: 2-Byte RGB Format

Byte	Bits Used	Bit Sequence
Odd bytes	8 data bits	$D_9D_8D_7D_6D_5D_4D_3D_2$
Even bytes	2 data bits + 6 unused bits	$0\ 0\ 0\ 0\ 0\ 0\ D_1D_0$

Readout Formats

Progressive format is used for raw Bayer output.

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Output Formats

ITU-R BT.656 and RGB Output

The MT9V136 can output processed video as a standard ITU-R BT.656 (CCIR656) stream, an RGB stream, or as unprocessed Bayer data. The ITU-R BT.656 stream contains YCbCr 4:2:2 data with fixed embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression.

Colorpipe data (pre-lens correction and overlay) can also be output in YCbCr 4:2:2 and a variety of RGB formats in 640 by 480 progressive format in conjuction with LINE_VALID and FRAME_VALID.

The MT9V136 can be configured to output 16-bit RGB (565RGB), 15-bit RGB (555RGB), and two types of 12-bit RGB (444RGB). Refer to Table 54 and Table 55 on page 102 for details.

Bayer Output

Unprocessed paired Bayer data are generated when bypassing the IFP completely—that is, by simply outputting the sensor-paired Bayer stream as usual, using FV, LV, and PIXCLK to time the data. This mode is called sensor stand-alone mode.

Output Ports

Composite Video Output

The composite video output DAC is external-resistor-programmable and supports both single-ended and differential output. The DAC is driven by the on-chip video encoder output.

Parallel Output

Parallel output uses either 8-bit or 10-bit output. Eight-bit output is used for ITU-R BT.656 and RGB output. Ten-bit output is used for raw Bayer output.

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Usage Modes

How a camera based on the MT9V136 will be configured depends on what features are used. In the simplest case, only an MT9V136 plus an external flash memory, or an 8-bit µC might be sufficient. Flash sizes vary depending on the data for registers, firmware, and overlay data—somewhere between 2Kb to 16Mb. The two-wire bus is adequate since only high-level commands are used to invoke overlays, load registers from memory or set up lens correction parameters. Overlay data can alternatively be issued by the external µC if the rate of refreshing data is deemed adequate. If there are no commands in the Flash image the device can be in"Auto Configuration" mode by which the sensor is set up according to the status of pins FRAME_VALID, LINE_VALID and DOUT_LSB_0. For further information, see “Auto-Configuration” on page 33 .

In the simplest case no Flash memory or µC is required as shown inFigure 15 . This is truly single chip operation.

Figure 15: Auto-Config Mode

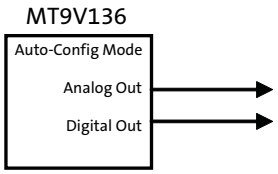

Figure 16: Flash Mose

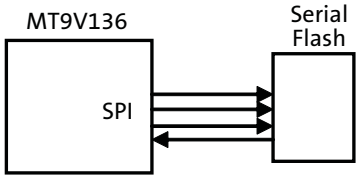

Figure 17: Host Mode with Flash

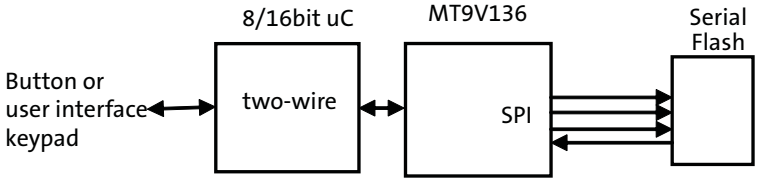

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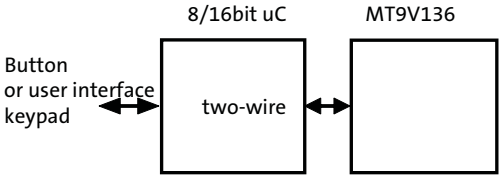
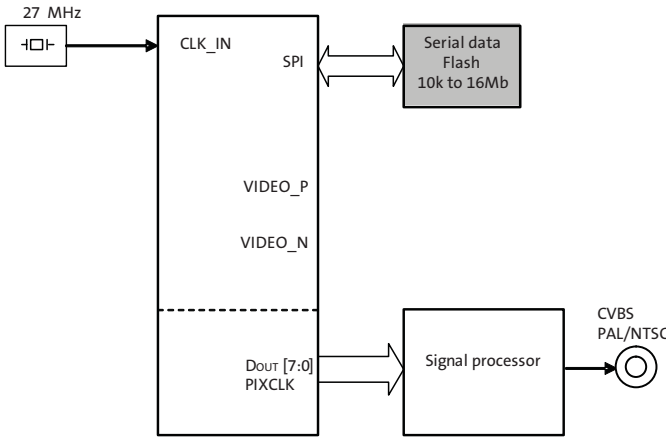
Figure 18: Host Mode



External Signal Processing

An external signal processor can take data from ITU656 or raw Bayer output format and post-process or compress the data in various formats.

Figure 19: External Signal Processing Block Diagram



How to Access Registers and Variables

Registers and variables are accessed in different ways.

Registers

All the registers shown in Table 26, “0: Core Registers,” on page 50 can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

“Two-Wire Serial Bus Timing” on page 115 describes the interface protocol of the two-wire serial interface in more detail. The on-chip microcontroller can also access all the registers through physical address as shown below.

Variables

Variables are located in the microcontroller RAM memory. Each driver, such as auto exposure, auto white balance, and flicker detection, has a unique driver ID (0..31) number and a set of variables associated with that driver. Each variable associated with that driver is uniquely identified by its offset.

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All driver variables can be accessed through the mcu_variable_address and mcu_variable_data registers in the XDMA register map. The variables are accessed using a logical address. This address, which is set in the mcu_variable_address register, consists of a 5-bit driver ID number and a 8-bit variable offset.

To view how variables are written, you may also turn on Log in DevWare and select "Split to REG=."

For instance, to access to cam1, which is in page 18, you would see something like this:

```
REG= 0x098E, 0x4800 // LOGICAL_ADDRESS_ACCESS
[CAM1_SENSOR_0_Y_ADDR_START]

REG= 0x0990, 0x000C // MCU_VARIABLE_DATA0


REG= 0x098E, 0x4818 // LOGICAL_ADDRESS_ACCESS
[CAM1_SENSOR_0_CPIPE_LAST_ROW]

REG= 0x0990, 0x01E3 // MCU_VARIABLE_DATA0
```

The address is calculated as follows:

```
#define MAKE_RB_MCU_ADDRESS(c,d,a) ( (((c)==1)<<15) | ((d)<<10) |
((a)&0x3FF) )

Where:

C - is8 (set to 2)

D - driver

A - offset
```

The offset is then the variable address, that is, 48 18 for cam1 address with offset 18.

Reserved

Do not change any of the reserved bits.

Device Configuration

After power is applied and the device is out of reset by deasserting the RESET_N pin, it will enter a boot sequence to configure it's operating mode. There are essentially four modes, two when Flash is present and two when Flash is not present.

Flash is present and:

1. Valid ID is detected and Configuration exist in Flash header then
   - Disable Auto-Config
   - Parse Flash Content
   - Load Flash Configuration ->Flash Configuration Mode then
2. Valid ID is detected and no Configuration exist
   - Enter Host Configuration.

Flash is not present and:

3. SPI_SDI == 0 then
   - Enter Host Configuration.
4. SPI_SDI != 0
   - Enter Auto Configuration

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Flash Configuration Mode

If a valid Flash is detected (by reading device ID other than 0x00 or 0xFF) and configuration section is within the TOC of the Flash is detected then the configuration present in Flash is executed.

Host Configuration

This mode is entered if no Flash is present or if Flash is present but there are no commands.

Auto-Configuration

The System Manager supports an auto-configuration feature. During system start-up, the System Manager (internal FW of the device) first detects whether an SPI Flash device is attached to the MT9V136. If not, it will then sample the state of a number of GPI inputs including FRAME_VALID, LINE_VALID and DOUT_LSB0. The state of these inputs then determines the configuration of a number of subsystems of the device such as readout mode, pedestal and video format, respectively.

Auto-configuration feature can be disabled by grounding the SPI_DIN pin. The System Manager samples the state of this pin during the Flash device detection process. If no SPI Flash device is detected (read device ID of 0x00 or 0xFF), AND the SPI_DIN pin is grounded, then auto-configuration is disabled.

Power-up Sequence

The core voltage should trail the IO voltage by a positive number. All 2.8V rails should be turned on at the same time from a single linear regulator with appropriate decoupling between power planes particularly VAA, VAA_PIX is crucial. See Reference Schematic for details.

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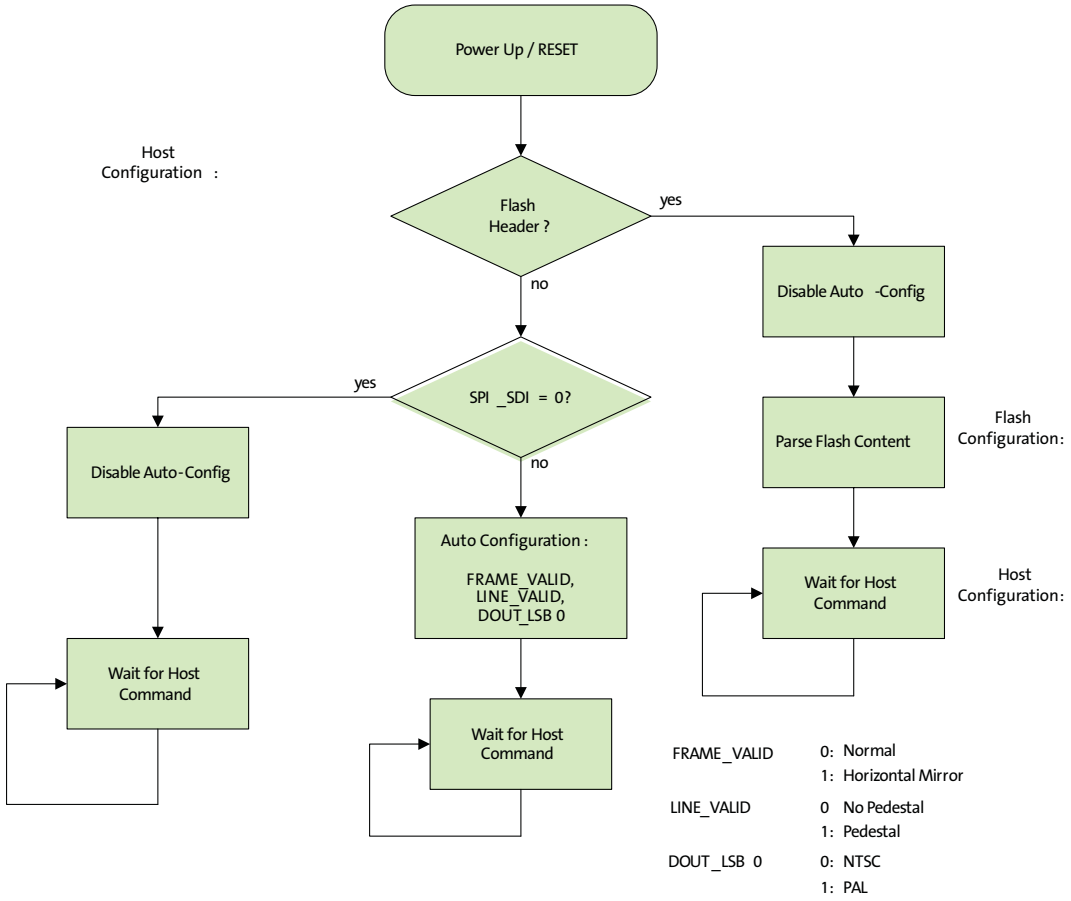
Figure 20: Power-Up Sequence – Configuration Options Flow Chart



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Supported SPI Devices

Table 13 lists supported Flash devices. Devices not compatible will require a firmware patch. Contact Aptina for additional support.

Table 13: SPI Flash Devices

Type	Density	Mfg	Decive	Speed (MHz)	Standard	Temp Range (°F)	Supported
Flash	8 MBit	Atmel	AT26DF081A[1]	70	JEDEC/Device ID	–20 to +85	Yes
Flash	1 MBit	ST	M25P10-AVMB3	50		–4 to +125	With s/w patch[2]

Notes:
1. The MT9V136 Rev1 firmware supports the AT26DF081A which:
   4a. Has 4K erase blocks
   4b. Uses the 0x20 command to block erase
   4c. Uses the 0x60 command to chip erase
2. Other devices will require firmware patches

Supported SPI Commands

The following SPI commands (as shown in Table 14) are supported by the MT9V136.

Table 14: SPI Commands Supported by the MT9V136

Command	Value
Read Array	03
Block Erase	20
Chip Erase	60
Read Status	05
Write status	0x01
Byte Page Program	0x02
Write Enable	0x06

Note: An array READ by DMA is a byte stream.

Table 15: Read Manufactacturing ID:9F

Data	Byte Number
Manu ID	Byte[0]
Device ID (part 1)	Byte[1]
Device ID (part 2)	Byte[2]

The System Manager configures the system as follows:

- Overlay block enabled, but no layers enabled.
- Reads GPI[2..0] one time only at initialization stage.
- PAL Select state used to configure lens correction, overlay and sensor/colorpipe.
- Automatically transitions to the enter streaming state.

Table 16: GPIO Bit Descriptions

	GPI[2] (DOUT_LSB0)	GPI[1] (FRAME_VALID)	GPI[0] (LINE_VALID)
Low ("0")	NTSC	Normal	No Pedestal
High ("1")	PAL	Horizontal mirror	Pedestal

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Host Command Interface

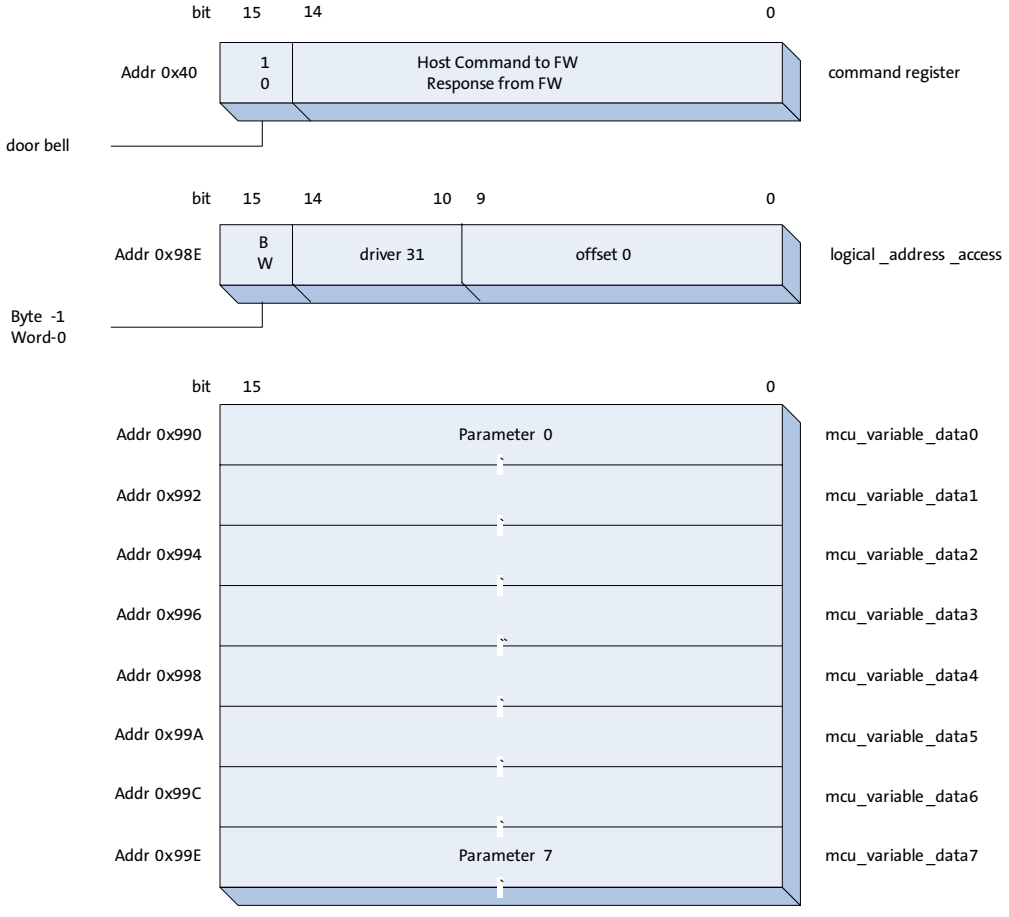
Aptina's sensors and SOCs contain numerous registers that are accessed through a two-wire interface with speeds up to 400 kHz.

The MT9V136, in addition to writing or reading straight to/from registers or firmware variables, has a mechanism to write higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on chip firmware and the results are reported back. In general, registers shall not be accessed with the exception of registers that are marked for "User Access."

Flash memory is also available to store commands for later execution. Under DMA control, a command is written into the SOC and executed.

For a complete spec on host commands, refer to the MT9V126 /MT9V136 Host Command Interface Specification.

Figure 21: Interface Structure



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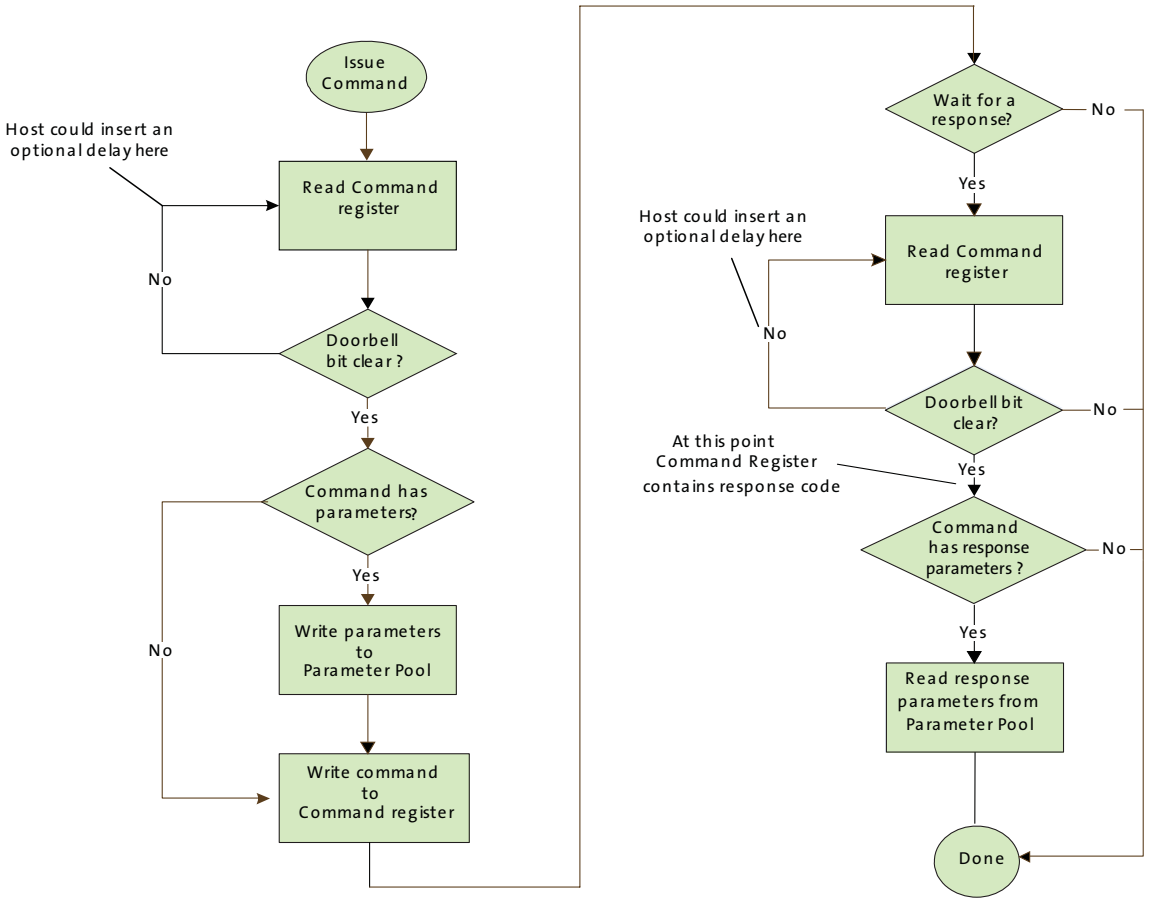
Host Command Process Flow



Command Flow

A host command would be written by a host by first polling the door bell bit in the command register. Once this bit is clear the host would open up a parameter window by writing the driver number and parameter offset into the “logical_address_access” register and subsequenly the parameter pool.

Finally, a command code is written to the command register with the door bell bit set. Once the command is executed, bit 15 in the command register is cleared after a response code has been placed into the command register bits [14:0].

Only at this point may the host proceed to issue a new command.

For a complete command list and further information consult the Host Comman Interface Specification.

A number of examples of how (using DevWare) a command may be initiated in the form of a “Preset” follow.

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Set Parallel Mode - Normal (Overlay i656)

The Presets for DevWare are checking the doorbell bit at the end of the command sequence and not as suggested at the beginning. This is permissible since the host command driver is always ready to receive commands.

```
FIELD_WR = LOGICAL_ADDRESS_ACCESS, LOGICAL_ACCESS_DRV_NUM, 31
FIELD_WR = LOGICAL_ADDRESS_ACCESS, LOGICAL_ACCESS_OFFSET, 0
FIELD_WR = MCU_VARIABLE_DATA0, 0x1000          // Overlay, enable FVLV
FIELD_WR = COMMAND_REGISTER, 0x8801
POLL_FIELD = COMMAND_REGISTER, DOORBELL, ! = 0, DELAY = 10,TIMEOUT = 100
ERROR_IF = COMMAND_REGISTER, HOST_COMMAND, ! = 0, “Command failed”,
```

Summary of Host Commands

Table 17 on page 38 through Table 22 on page 39 show summaries of the host commands. The commands are divided into the following sections:

- System Manager
- Overlay
- GPIO Host interface
- Flash Manager Host
- Patch Loader Interface
- TX Manager

Following is a summary of the overlay function. The description gives a quick orientation as to the function. The “Type" column shows if it is an asynchronous (A) or synchronous (S) command. For a complete list of all commands, consult the Host Command Interface Specification document.

Table 17: System Manager Commands

System Manager Host Command	Value	Type	Description
Set State	0x8100	A	Request the system enter a new state
Get State	0x8101	S	Get the current state of the system

Table 18: Overlay Host Commands

Overlay Host Command	Value	Type	Description
Enable Overlay	0x8200	S	Enable or disable the overlay subsystem
Get Overlay State	0x8201	S	Retrieves the state of the overlay subsystem
Set Calibration	0x8202	S	Set the calibration offset
Set Bitmap Property	0x8203	S	Set a property of a bitmap
Get Bitmap Property	0x8204	S	Get a property of a bitmap
Set String Property	0x8205	S	Set a property of a character string
Load Buffer	0x8206	A	Load an overlay buffer with a bitmap (from Flash)
Load Status	0x8207	S	Retrieve status of an active load buffer operation
Write Buffer	0x8208	S	Write directly to an overlay buffer
Read Buffer	0x8209	S	Read directly from an overlay buffer
Enable Layer	0x820A	S	Enable or disable an overlay layer
Get Layer Status	0x820B	S	Retrieve the status of an overlay layer
Set String	0x820C	S	Set the character string
Load String	0x820E	A	Load a character string (from Flash)

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Table 19: GPIO Host Commands

GPIO Host Command	Value	Type	Description
Set GPIO Property	0x8400	S	Set a property of one or more GPIO pins
Get GPIO Property	0x8401	S	Retrieve a property of a GPIO pin
Set GPO State	0x8402	S	Set the state of a GPO pin or pins
Get GPIO State	0x8403	S	Get the state of a GPI pin or pins
Set GPI Association	0x8404	S	Associate a GPI pin state with a Command Sequence stored in SPI Flash

Table 20: Flash Manager Host Commands

Flash Manager Host Command	Value	Type	Description
Get Lock	0x8500	A	Request the Flash Manager access lock
Lock Status	0x8501	S	Retrieve the status of the access lock request
Release Lock	0x8502	S	Release the Flash Manager access lock
Config	0x8503	S	Configure the Flash Manager and underlying SPI Flash subsystem
Read	0x8504	A	Read data from the SPI Flash
Write	0x8505	A	Write data to the SPI Flash
Erase Block	0x8506	A	Erase a block of data from the SPI Flash
Erase Device	0x8507	A	Erase the SPI Flash device
Query Device	0x8508	A	Query device-specific information
Status	0x8509	S	Obtain status of current A operation

Table 21: Sequencer Host Commands

Sequencer Host Command	Value	Type	Description
Set Encoding Mode	0x8603	S	Set the encoding mode
Enable Horizontal Flip	0x8604	S	Enable or disable horizontal flip
Set Flicker Frequency	0x8605	S	Set the flicker frequency
Refresh Mode	0x8606	S	Refresh the Sequencer mode/context

Table 22: TX Manager Host Commands

TX Manager Host Command	Value	Type	Description
Config DAC	0x8800	S	Configure the Video DAC
Set Parallel Mode	0x8801	S	Configure the Parallel output port
Enable UART	0x8802	S	Enable the diagnostic UART

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Slave Two-Wire Serial Interface

The two-wire serial interface bus enables read/write access to control and status registers within the MT9V136. This interface is designed to be compatible with the MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) 1.0, which uses the electrical characteristics and transfer protocols of the two-wire serial interface specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a pull-up resistor in the range of 1.5 to 4.7kΩ resistor.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16-bit register address
- an acknowledge or a no-acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 23.

Table 23: Two-Wire Interface ID Address Switching

SADDR	Two-Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

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Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a write, and a "1" indicates a read. The default slave addresses used by the MT9V136 are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two-wire serial interface specification.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Typical Operation

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a "0" indicates a WRITE and a "1" indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which a WRITE will take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16-bit data, as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, just as in the write request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

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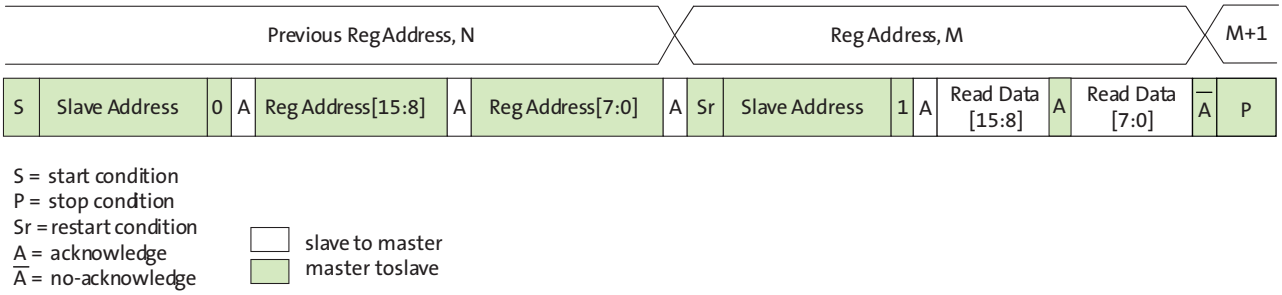
Single READ from Random Location

Figure 22 shows the typical READ cycle of the host to MT9V136. The first two bytes sent by the host are an internal 16-bit register address. The following 2-byte READ cycle sends the contents of the registers to host.

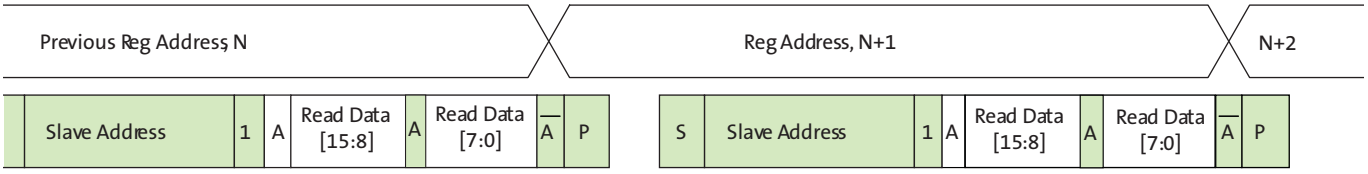
Figure 22: Single READ from Random Location



Single READ from Current Location

Figure 23 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

Figure 23: Single Read from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 24) starts in the same way as the single READ from random location (Figure 22). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

Figure 24: Sequential READ, Start from Random Location

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Sequential READ, Start from Current Location

This sequence (Figure 25) starts in the same way as the single READ from current location (Figure 23 on page 42). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until "L" bytes have been read.

Figure 25: Sequential READ, Start from Current Location

Single Write to Random Location

Figure 26 shows the typical WRITE cycle from the host to the MT9V136. The first 2 bytes indicate a 16-bit address of the internal registers with most-significant byte first. The following 2 bytes indicate the 16-bit data.

Figure 26: Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 27) starts in the same way as the single WRITE to random location (Figure 26). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 27: Sequential WRITE, Start at Random Location

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Overlay Capability

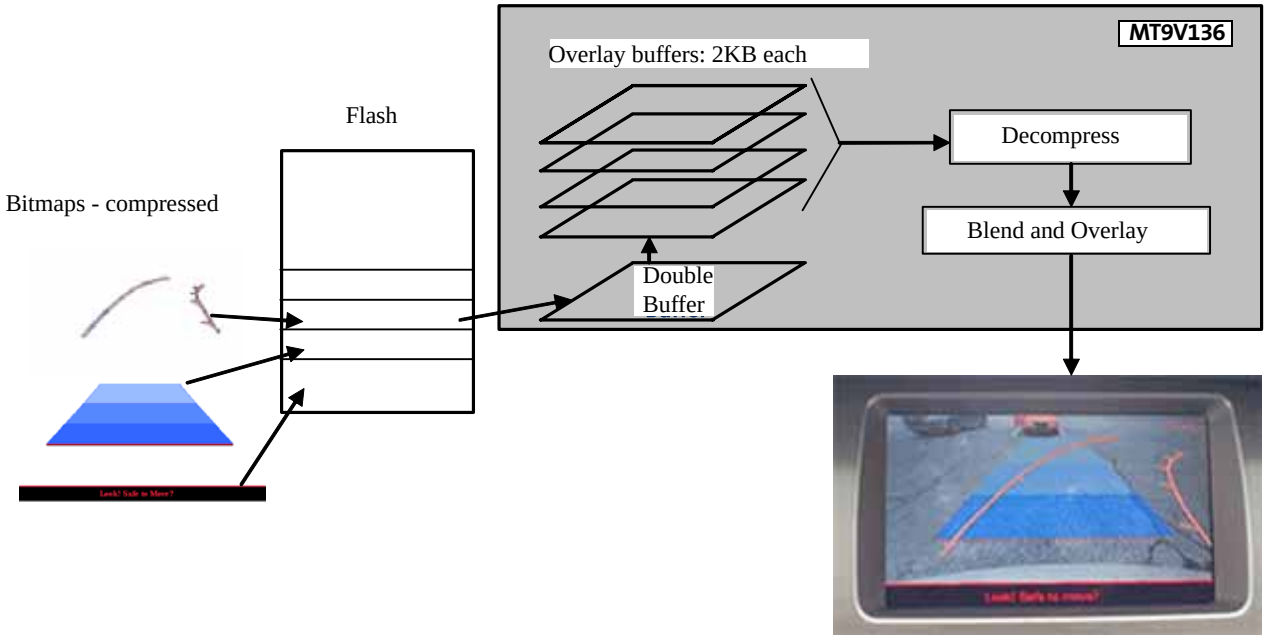
Figure 28 highlights the graphical overlay data flow of the MT9V136. The images are separated to fit into 2KB blocks of memory after compression. The graphics overlay data block does not have a minimum size although the overhead as a percentage of data will increase.

- Up to four overlays may be blended simultaneously
- Overlay size 360 x 480 pixels rendered into a display area of 720 x 480 pixels
- Selectable readout: rotating order is user programmable
- Dynamic movement through predefined overlay images
- Palette of 32 colors out of 64,000 with eight colors per bitmap
- Blend factors may be changed dynamically to achieve smooth transitions

A memory block is individually addressable in memory. Multiple passes may be required to fit an image into a 2KB block of memory; alternatively, the memory block can be divided into two or more blocks to make the image fit. Every graphic image may be positioned in an x/y direction and overlap with other graphic images.

The host may load an image at any time. Under control of DMA assist, data are transferred to the double buffer in compressed form. This assures that no display data are corrupted during the replenishment of the four active overlay buffers.

Figure 28: Overlay Data Flow



Note: These images are not actually rendered, but show conceptual objects and object blending.

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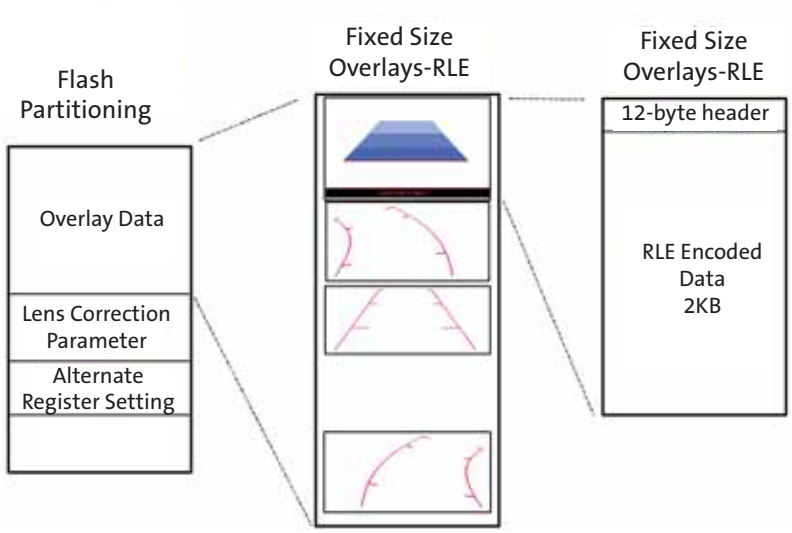
Serial Memory Partition

The contents of the Flash/EEPROM memory partition logically into three blocks:

- Memory for overlay data and descriptors
- Memory for register settings, which may be loaded at boot-up
- Firmware extensions or software patches; in addition to the on-chip firmware, extensions reside in this block of memory

These blocks are not necessarily contiguous.

Figure 29: Memory Partitioning



For a complete desctiption of memory organization, refer to the MT9V136 Encoding Specification.

External Memory Speed Requirement

For a 2KB block of overlay to be transferred within a frame time to achieve maximum update rate, the serial memory has to be a certain speed.

Table 24: Transfer Time Estimate

Frame Time	SPI Clock	Transfer Time to 2KB
16.6ms	4.5 MHz	3–4ms

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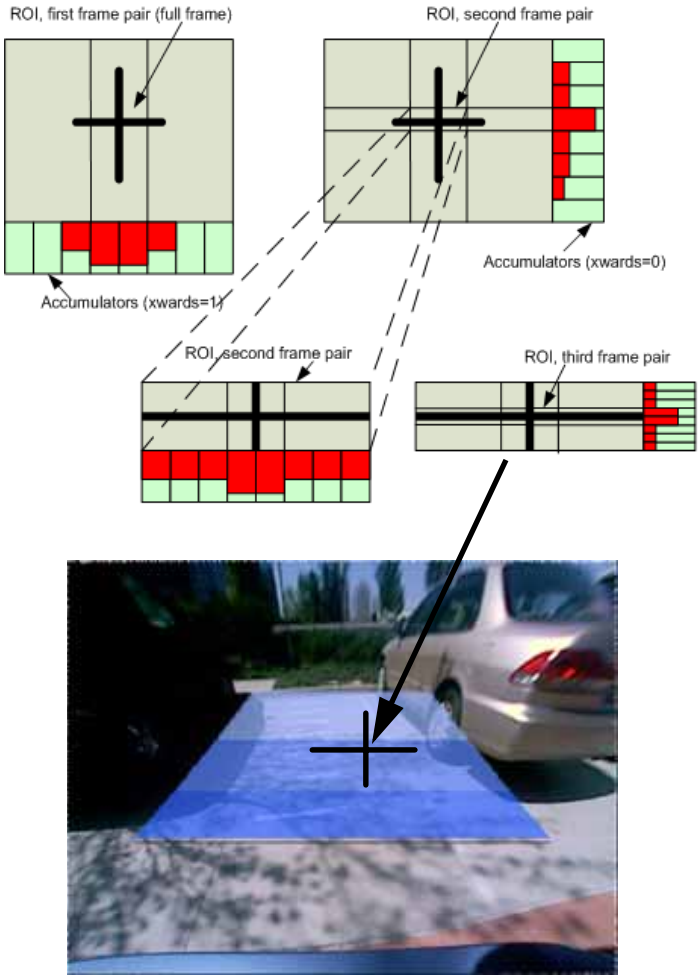
Overlay Adjustment

To ensure a correct position of the overlay to compensate for assembly deviation, the overlay can be adjusted with assistance from the overlay statistics engine:

- The overlay statistics engine provides a coarse horizontal (in the first frame) and then vertical (in the second frame) 8-bin luma histogram.
- In subsequent measurements, the region of interest (ROI) for the histogram can be reduced to zoom to a pixel accurate location of the target.
- The determined location of the target can be used to assign a calibration value to offset the overlay graphics position within the output frame.

Figure 30: Overlay Calibration



The position of the target will be used to determine the calibration value that shifts the X,Y position of adjustable overlay graphics.

Unlike the lens distortion correction and perspective correction, the overlay calibration is intended to be applied on a device by device basis "in system," which means after the camera has been installed. Aptina provides basic programming scripts that may reside in the SPI Flash memory to assist in this effort.

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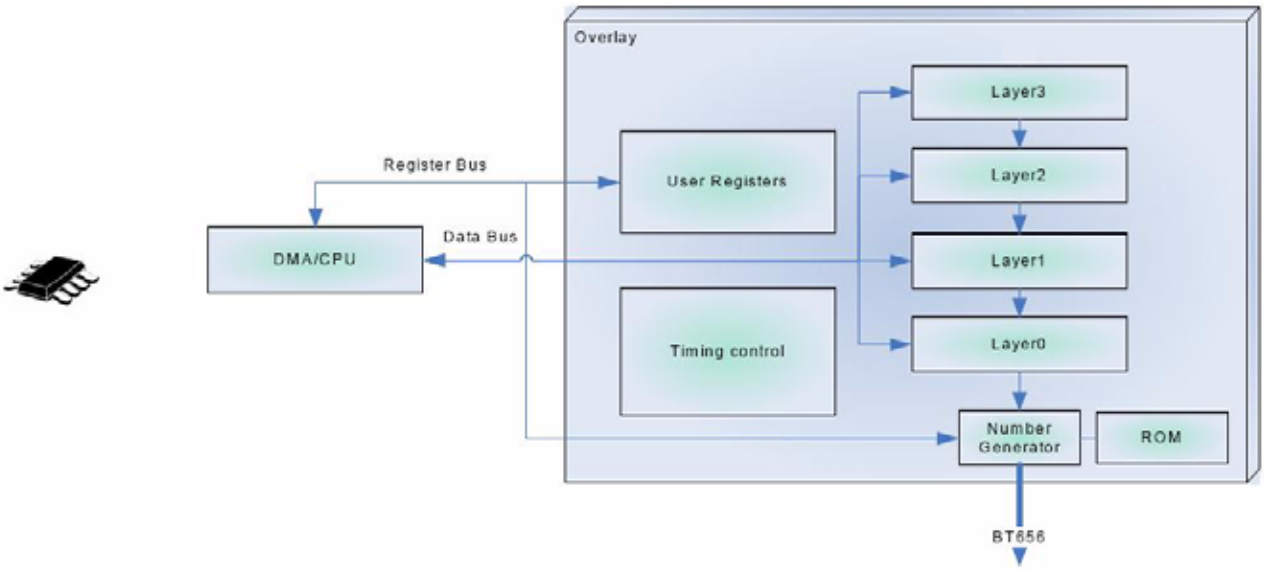
Overlay Number Generator

In addition to the four overlay buffers, a fifth plane exists for a number character overlay.

There are a total of:

- 16 alphanumeric characters available
- 22 characters maximum per line
- 16 x 32 pixels with 1-bit color depth

Figure 31: Internal Block Diagram Overlay



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Character Generator

The character generator can be seen as the fifth top layer, but instead of getting the source from RLE data in the memory buffers, it has a predefined 16 characters stored in ROM.

All the characters are 1-bit depth color and are sharing the same YCbCr look up table.

Figure 32: Example of Character Descriptor 0 Stored in ROM

ROM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x06	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x08	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x0a	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x0c	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0
0x0e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x10	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x12	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x14	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x16	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x18	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1a	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1c	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1e	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x20	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x22	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x24	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x26	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x28	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x2a	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x2c	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x2e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x30	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
0x32	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x34	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x36	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x38	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x3a	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3c	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

...

It can show a row of up to 22 characters of 16 x 32 pixels resolution (32 x 32 pixels when blended with the bt656 data).

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Character Generator Details

Table 25 shows the characters that can be generated.

Table 25: Character Generator Details

Item	Quantity	Description
16-bit character	22	Coder for one of these characters: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, /, (space), :, –, (comma), (period)
1 bpp color	1	Depth of the bit map is 1 bpp

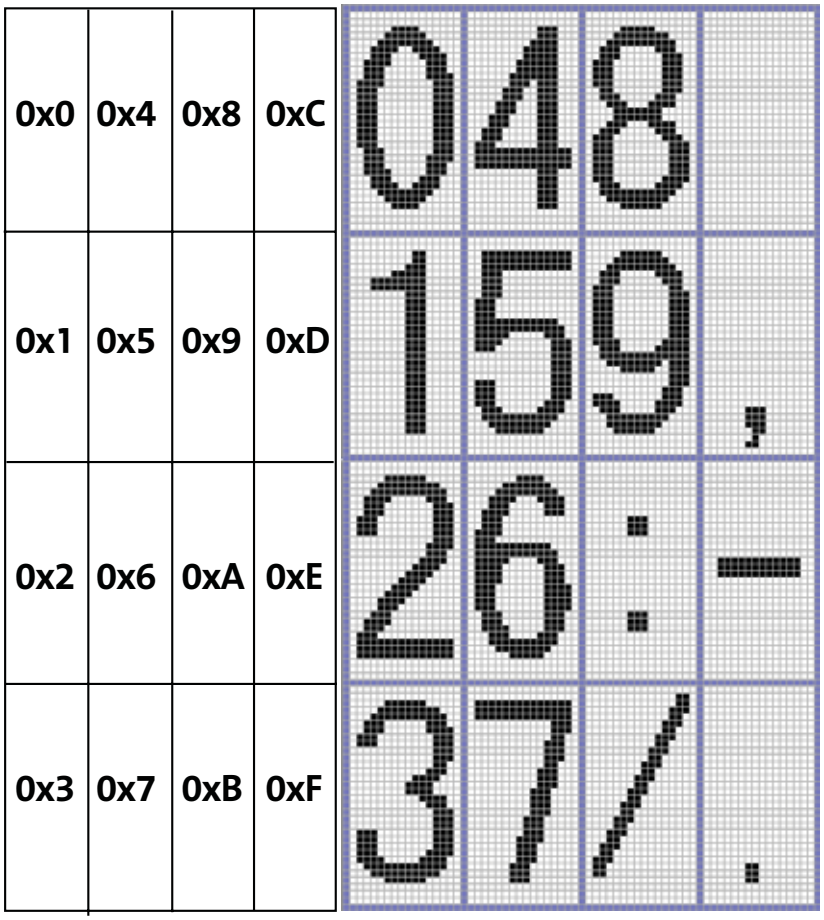
It is responsibility of the user to set up proper values in the character positioning to fit them in the same row (that is one of the reasons that 22 is the maximum number of characters).

Note: No error is generated if the character row overruns the horizontal or vertical limits.

Full Character Set for Overlay

Figure 33 shows all of the characters that can be generated by the MT9V136.

Figure 33: Full Character Set for Overlay



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Register Summary

Table 26: 0: Core Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288(R0x00003000)	model_id_	0000 0000 0000 0000 dddd dddd dddd dddd	8833 (0x00002281)
R12290(R0x00003002)	y_addr_start_	0000 0000 0000 0000 0000 dddd dddd dddd	12 (0x0000000C)
R12292(R0x00003004)	x_addr_start_	0000 0000 0000 0000 0000 00dd dddd dddd	16 (0x00000010)
R12294(R0x00003006)	y_addr_end_	0000 0000 0000 0000 0000 dddd dddd dddd	499 (0x000001F3)
R12296(R0x00003008)	x_addr_end_	0000 0000 0000 0000 0000 00dd dddd dddd	663 (0x00000297)
R12298(R0x0000300A)	frame_length_lines_	0000 0000 0000 0000 dddd dddd dddd dddd	525 (0x0000020D)
R12300(R0x0000300C)	line_length_pck_	0000 0000 0000 0000 0000 dddd dddd dddd	858 (0x0000035A)
R12304(R0x00003010)	fine_correction	0000 0000 0000 0000 0000 dddd dddd dddd	49 (0x00000031)
R12306(R0x00003012)	coarse_integration_time_	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R12308(R0x00003014)	fine_integration_time_	0000 0000 0000 0000 0000 dddd dddd dddd	164 (0x000000A4)
R12310(R0x00003016)	row_speed	0000 0000 0000 0000 0000 0ddd 0ddd 0ddd	273 (0x00000111)
R12312(R0x00003018)	extra_delay	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12314(R0x0000301A)	reset_register	0000 0000 0000 0000 dd0d 0ddd dddd dddd	4312 (0x000010D8)
R12318(R0x0000301E)	data_pedestal_	0000 0000 0000 0000 0000 00dd dddd dddd	42 (0x0000002A)
R12320(R0x00003020)	software_reset_	0000 0000 0000 0000 0000 000d 0000 0000	0 (0x00000000)
R12324(R0x00003024)	pixel_order_	0000 0000 0000 0000 0000 0000 0000 00??	0 (0x00000000)
R12326(R0x00003026)	gpi_status	0000 0000 0000 0000 dddd dd00 0ddd ????	64639 (0x0000FC7F)
R12328(R0x00003028)	analogue_gain_code_global_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12330(R0x0000302A)	analogue_gain_code_greenr_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12332(R0x0000302C)	analogue_gain_code_red_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12334(R0x0000302E)	analogue_gain_code_blue_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12336(R0x00003030)	analogue_gain_code_greenb_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12338(R0x00003032)	digital_gain_greenr_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)

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Table 26: 0: Core Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12340(R0x00003034)	digital_gain_red_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12342(R0x00003036)	digital_gain_blue_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12344(R0x00003038)	digital_gain_greenb_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12348(R0x0000303C)	frame_status	0000 0000 0000 0000 0000 0000 0000 00??	0 (0x00000000)
R12352(R0x00003040)	read_mode	0000 0000 0000 0000 dd00 dddd dddd dddd	65 (0x00000041)
R12354(R0x00003042)	dark_control2	0000 0000 0000 0000 dddd dddd dddd 00dd	8209 (0x00002011)
R12358(R0x00003046)	flash	0000 0000 0000 0000 ??dd dddd d000 0000	1536 (0x00000600)
R12360(R0x00003048)	flash_count	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R12374(R0x00003056)	green1_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12376(R0x00003058)	blue_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12378(R0x0000305A)	red_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12380(R0x0000305C)	green2_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12382(R0x0000305E)	global_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12400(R0x00003070)	test_pattern_mode_	0000 0000 0000 0000 0000 000d 0000 0ddd	0 (0x00000000)
R12402(R0x00003072)	test_data_red_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12404(R0x00003074)	test_data_greenr_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12406(R0x00003076)	test_data_blue_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12408(R0x00003078)	test_data_greenb_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12448(R0x000030A0)	x_even_inc_	0000 0000 0000 0000 0000 0000 0000 000?	1 (0x00000001)
R12450(R0x000030A2)	x_odd_inc_	0000 0000 0000 0000 0000 0000 0000 0ddd	1 (0x00000001)
R12452(R0x000030A4)	y_even_inc_	0000 0000 0000 0000 0000 0000 0000 000?	1 (0x00000001)
R12454(R0x000030A6)	y_odd_inc_	0000 0000 0000 0000 0000 0000 0000 0ddd	1 (0x00000001)
R12470(R0x000030B6)	dark_green1_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12472(R0x000030B8)	dark_blue_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)

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Table 26: 0: Core Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12474(R0x000030BA)	dark_red_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12476(R0x000030BC)	dark_green2_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12500(R0x000030D4)	column_correction	0000 0000 0000 0000 dddd 00dd dddd dddd	32 (0x00000020)
R12776(R0x000031E8)	horizontal_cursor_position_	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12778(R0x000031EA)	vertical_cursor_position_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12780(R0x000031EC)	horizontal_cursor_width_	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12782(R0x000031EE)	vertical_cursor_width_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R16076(R0x00003ECC)	dac_ld_0_1	0000 0000 0000 0000 ???? ???? dddd dddd	271 (0x0000010F)
R16084(R0x00003ED4)	dac_ld_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	2048 (0x00000800)
R16088(R0x00003ED8)	dac_ld_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	34708 (0x00008794)
R16104(R0x00003EE8)	dac_ld_28_29	0000 0000 0000 0000 dddd dddd dddd dddd	11008 (0x00002B00)

Table 27: 1: SOC1 Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12816(R0x00003210)	color_pipeline_control	0000 0000 0000 0000 0000 0d00 d0dd d000	176 (0x000000B0)
R12834(R0x00003222)	zoom_window_x0	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12836(R0x00003224)	zoom_window_x1	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R12838(R0x00003226)	zoom_window_y0	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12840(R0x00003228)	zoom_window_y1	0000 0000 0000 0000 0000 dddd dddd dddd	479 (0x000001DF)
R12852(R0x00003234)	awb_debug_weight	0000 0000 0000 0000 0000 0000 000d dddd	X
R12854(R0x00003236)	awb_norm_sumr	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12856(R0x00003238)	awb_norm_sumg	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12858(R0x0000323A)	awb_norm_sumb	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12860(R0x0000323C)	awb_x_shift	0000 0000 0000 0000 0000 0ddd dddd dddd	3 (0x00000003)
R12862(R0x0000323E)	awb_y_shift	0000 0000 0000 0000 0000 0ddd dddd dddd	3 (0x00000003)

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Table 27: 1: SOC1 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12864(R0x00003240)	awb_xy_scale	0000 0000 0000 0000 0000 0000 dddd dddd	51 (0x00000033)
R12866(R0x00003242)	awb_weight_r0	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12868(R0x00003244)	awb_weight_r1	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12870(R0x00003246)	awb_weight_r2	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12872(R0x00003248)	awb_weight_r3	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12874(R0x0000324A)	awb_weight_r4	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12876(R0x0000324C)	awb_weight_r5	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12878(R0x0000324E)	awb_weight_r6	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12880(R0x00003250)	awb_weight_r7	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12884(R0x00003254)	first_color	0000 0000 0000 0000 0000 0000 0000 00dd	0 (0x00000000)
R12886(R0x00003256)	last_row	0000 0000 0000 0000 0000 0ddd dddd dddd	483 (0x000001E3)
R12888(R0x00003258)	awb_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12890(R0x0000325A)	awb_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12892(R0x0000325C)	awb_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R12894(R0x0000325E)	awb_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R12896(R0x00003260)	awb_weight_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12898(R0x00003262)	awb_luma_th	0000 0000 0000 0000 dddd dddd dddd dddd	65288 (0x0000FF08)
R12902(R0x00003266)	awb_weight_th	0000 0000 0000 0000 0000 0000 dddd dddd	145 (0x00000091)
R12904(R0x00003268)	awb_weight_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12906(R0x0000326A)	aperture_parameters_1d	0000 0000 0000 0000 00dd dddd dddd dddd	4616 (0x00001208)
R12908(R0x0000326C)	aperture_parameters_2d	0000 0000 0000 0000 0ddd dddd dddd dddd	4616 (0x00001208)
R12910(R0x0000326E)	low_pass_yuv_filter	0000 0000 0000 0000 0000 0000 dddd dddd	128 (0x00000080)
R12912(R0x00003270)	threshold_for_y_filter_r_channel	0000 0000 0000 0000 0000 dddd dddd dddd	1962 (0x000007AA)
R12914(R0x00003272)	threshold_for_y_filter_g_channel	0000 0000 0000 0000 0000 dddd dddd dddd	2020 (0x000007E4)

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Table 27: 1: SOC1 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12916(R0x00003274)	threshold_for_y_filter_b_channel	0000 0000 0000 0000 0000 0000 0ddd dddd	42 (0x0000002A)
R12918(R0x00003276)	black_level_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12922(R0x0000327A)	red_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12924(R0x0000327C)	green1_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12926(R0x0000327E)	green2_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12928(R0x00003280)	blue_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12942(R0x0000328E)	dm_edge_th	0000 0000 0000 0000 0000 0000 dddd dddd	12 (0x0000000C)
R12958(R0x0000329E)	preview_hunting_gain_enable	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R12960(R0x000032A0)	dkdelta_ccm_cc1	0000 0000 0000 0000 0000 000d dddd dddd	322 (0x00000142)
R12962(R0x000032A2)	dkdelta_ccm_cc2	0000 0000 0000 0000 0000 000d dddd dddd	217 (0x000000D9)
R12964(R0x000032A4)	dkdelta_ccm_cc3	0000 0000 0000 0000 0000 000d dddd dddd	485 (0x000001E5)
R12966(R0x000032A6)	dkdelta_ccm_cc4	0000 0000 0000 0000 0000 000d dddd dddd	43 (0x0000002B)
R12968(R0x000032A8)	dkdelta_ccm_cc5	0000 0000 0000 0000 0000 000d dddd dddd	327 (0x00000147)
R12970(R0x000032AA)	dkdelta_ccm_cc6	0000 0000 0000 0000 0000 000d dddd dddd	142 (0x0000008E)
R12972(R0x000032AC)	dkdelta_ccm_cc7	0000 0000 0000 0000 0000 000d dddd dddd	490 (0x000001EA)
R12974(R0x000032AE)	dkdelta_ccm_cc8	0000 0000 0000 0000 0000 000d dddd dddd	125 (0x0000007D)
R12976(R0x000032B0)	dkdelta_ccm_cc9	0000 0000 0000 0000 0000 000d dddd dddd	409 (0x00000199)
R12978(R0x000032B2)	dkdelta_ccm_ctl	0000 0000 0000 0000 00dd dddd dddd dddd	8980 (0x00002314)
R12980(R0x000032B4)	dkdelta_ccm_scale	0000 0000 0000 0000 0000 00dd dddd dddd	528 (0x00000210)
R12982(R0x000032B6)	dkdelta_ccm_exp1	0000 0000 0000 0000 0ddd dddd dddd dddd	18724 (0x00004924)
R12984(R0x000032B8)	dkdelta_ccm_exp2	0000 0000 0000 0000 0000 dddd dddd dddd	2340 (0x00000924)
R12986(R0x000032BA)	red_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12988(R0x000032BC)	green_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12990(R0x000032BE)	blue_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

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Table 27: 1: SOC1 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12992(R0x000032C0)	ccm_exp_low_byte	0000 0000 0000 0000 0ddd dddd dddd dddd	14627 (0x00003923)
R12994(R0x000032C2)	ccm_exp_high_byte	0000 0000 0000 0000 0000 dddd dddd dddd	1828 (0x00000724)
R12996(R0x000032C4)	ccm_elements_1_and_2	0000 0000 0000 0000 dddd dddd dddd dddd	55790 (0x0000D9EE)
R12998(R0x000032C6)	ccm_elements_3_and_4	0000 0000 0000 0000 dddd dddd dddd dddd	11035 (0x00002B1B)
R13000(R0x000032C8)	ccm_elements_5_and_6	0000 0000 0000 0000 dddd dddd dddd dddd	35818 (0x00008BEA)
R13002(R0x000032CA)	ccm_elements_7_and_8	0000 0000 0000 0000 dddd dddd dddd dddd	32022 (0x00007D16)
R13004(R0x000032CC)	ccm_elements_9_and_signs	0000 0000 0000 0000 00dd dddd dddd dddd	11714 (0x00002DC2)
R13012(R0x000032D4)	red_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13014(R0x000032D6)	green1_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13016(R0x000032D8)	green2_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13018(R0x000032DA)	blue_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13020(R0x000032DC)	second_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13022(R0x000032DE)	fd_win_size_lo	0000 0000 0000 0000 dddd dddd dddd dddd	3200 (0x00000C80)
R13040(R0x000032F0)	fd_win_size_hi	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13042(R0x000032F2)	fd_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13044(R0x000032F4)	fd_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13048(R0x000032F8)	fd_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13050(R0x000032FA)	fd_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	4 (0x00000004)
R13052(R0x000032FC)	fd_avg	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R13100(R0x0000332C)	fm_blank_frames	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R13102(R0x0000332E)	output_format_configuration	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13104(R0x00003330)	output_format_test	0000 0000 0000 0000 0000 d00d d0dd dddd	0 (0x00000000)
R13106(R0x00003332)	fm_line_count	0000 0000 0000 0000 0000 ???? ???? ????	0 (0x00000000)
R13108(R0x00003334)	fm_frame_count	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)

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Table 27: 1: SOC1 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13128(R0x00003348)	special_effect_parameters	0000 0000 0000 0000 dddd dddd 0ddd dddd	25664 (0x00006440)
R13130(R0x0000334A)	sepia_constants	0000 0000 0000 0000 dddd dddd dddd dddd	45091 (0x0000B023)
R13180(R0x0000337C)	yuv_ycbcr_control	0000 0000 0000 0000 0000 0000 0000 dddd	6 (0x00000006)
R13182(R0x0000337E)	y_rgb_offset	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13300(R0x000033F4)	kernel_config	0000 0000 0000 0000 0000 0000 ddd0 dddd	3 (0x00000003)
R13302(R0x000033F6)	nr_red_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020)
R13304(R0x000033F8)	nr_green_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020)
R13306(R0x000033FA)	nr_blue_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020)
R13308(R0x000033FC)	nr_mm_th	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)

Table 28: 2: SOC2 Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13438(R0x0000347E)	clip1_config	0000 0000 0000 0000 0000 0000 0000 0ddd	2 (0x00000002)
R13440(R0x00003480)	clip2_config	0000 0000 0000 0000 0000 0000 0000 00dd	2 (0x00000002)
R13632(R0x00003540)	enable_tonal_curve	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R13634(R0x00003542)	tonal_x0	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13636(R0x00003544)	tonal_x1	0000 0000 0000 0000 0000 00dd dddd dddd	256 (0x00000100)
R13638(R0x00003546)	tonal_x2	0000 0000 0000 0000 0000 00dd dddd dddd	384 (0x00000180)
R13640(R0x00003548)	tonal_x3	0000 0000 0000 0000 0000 00dd dddd dddd	512 (0x00000200)
R13642(R0x0000354A)	tonal_x4	0000 0000 0000 0000 0000 00dd dddd dddd	640 (0x00000280)
R13644(R0x0000354C)	tonal_x5	0000 0000 0000 0000 0000 00dd dddd dddd	768 (0x00000300)
R13646(R0x0000354E)	tonal_x6	0000 0000 0000 0000 0000 00dd dddd dddd	896 (0x00000380)
R13648(R0x00003550)	tonal_y0	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13650(R0x00003552)	tonal_y1	0000 0000 0000 0000 0000 00dd dddd dddd	256 (0x00000100)
R13652(R0x00003554)	tonal_y2	0000 0000 0000 0000 0000 00dd dddd dddd	384 (0x00000180)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13654(R0x00003556)	tonal_y3	0000 0000 0000 0000 0000 00dd dddd dddd	512 (0x00000200)
R13656(R0x00003558)	tonal_y4	0000 0000 0000 0000 0000 00dd dddd dddd	640 (0x00000280)
R13658(R0x0000355A)	tonal_y5	0000 0000 0000 0000 0000 00dd dddd dddd	768 (0x00000300)
R13660(R0x0000355C)	tonal_y6	0000 0000 0000 0000 0000 00dd dddd dddd	896 (0x00000380)
R13664(R0x00003560)	reciprocal_of_x0_minus_zero	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13666(R0x00003562)	reciprocal_of_x1_minus_x0	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13668(R0x00003564)	reciprocal_of_x2_minus_x1	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13670(R0x00003566)	reciprocal_of_x3_minus_x2	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13672(R0x00003568)	reciprocal_of_x4_minus_x3	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13674(R0x0000356A)	reciprocal_of_x5_minus_x4	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13676(R0x0000356C)	reciprocal_of_x6_minus_x5	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13678(R0x0000356E)	reciprocal_of_400_minus_x6	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13686(R0x00003576)	ae_zone_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	X
R13688(R0x00003578)	ae_zone_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	X
R13694(R0x0000357E)	ae_zone_width	0000 0000 0000 0000 0000 dddd dddd dddd	X
R13696(R0x00003580)	ae_zone_height	0000 0000 0000 0000 0000 0ddd dddd dddd	X
R13698(R0x00003582)	ae_zone_size_lo	0000 0000 0000 0000 dddd dddd dddd dddd	X
R13700(R0x00003584)	ae_zone_size_hi	0000 0000 0000 0000 dddd dddd dddd dddd	X
R13704(R0x00003588)	ae_avg_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13706(R0x0000358A)	ae_avg_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13708(R0x0000358C)	ae_avg_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13712(R0x00003590)	hist1b_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13714(R0x00003592)	hist1a_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13716(R0x00003594)	hist0_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13718(R0x00003596)	hist1a_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)
R13720(R0x00003598)	hist1b_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)
R13722(R0x0000359A)	hist0_bin_config	0000 0000 0000 0000 0000 0000 ddd0 dddd	13 (0x0000000D)
R13724(R0x0000359C)	hist1a_bin_config	0000 0000 0000 0000 0000 0000 000d dddd	10 (0x0000000A)
R13726(R0x0000359E)	hist1b_bin_config	0000 0000 0000 0000 0000 0000 000d dddd	8 (0x00000008)
R13728(R0x000035A0)	hist0_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13730(R0x000035A2)	dark_color_kill_controls	0000 0000 0000 0000 0000 0000 dddd dddd	20 (0x00000014)
R13732(R0x000035A4)	bright_color_kill_controls	0000 0000 0000 0000 0000 0ddd dddd dddd	1428 (0x00000594)
R13736(R0x000035A8)	clip2_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13738(R0x000035AA)	clip1_min	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13740(R0x000035AC)	clip1_max	0000 0000 0000 0000 0000 dddd dddd dddd	4095 (0x00000FFF)
R13742(R0x000035AE)	clip2_min	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13744(R0x000035B0)	clip2_max	0000 0000 0000 0000 0000 dddd dddd dddd	4095 (0x00000FFF)
R13746(R0x000035B2)	clip2_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F
R13748(R0x000035B4)	hist0_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13750(R0x000035B6)	hist0_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13752(R0x000035B8)	hist0_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13754(R0x000035BA)	hist0_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13756(R0x000035BC)	hist1a_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13758(R0x000035BE)	hist1a_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13760(R0x000035C0)	hist1a_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13762(R0x000035C2)	hist1a_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13764(R0x000035C4)	hist1b_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13766(R0x000035C6)	hist1b_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13768(R0x000035C8)	hist1b_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13770(R0x000035CA)	hist1b_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13772(R0x000035CC)	clip2_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13774(R0x000035CE)	clip2_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13776(R0x000035D0)	hist_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13778(R0x000035D2)	hist_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13780(R0x000035D4)	hist_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13782(R0x000035D6)	hist_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13784(R0x000035D8)	clip1_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13786(R0x000035DA)	clip1_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13792(R0x000035E0)	clip2_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13794(R0x000035E2)	clip2_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13796(R0x000035E4)	clip1_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13798(R0x000035E6)	clip1_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13800(R0x000035E8)	clip1_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13802(R0x000035EA)	clip1_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13828(R0x00003604)	r_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13830(R0x00003606)	r_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13832(R0x00003608)	r_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13834(R0x0000360A)	r_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13836(R0x0000360C)	r_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13838(R0x0000360E)	r_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13840(R0x00003610)	r_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE)
R13842(R0x00003612)	r_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13844(R0x00003614)	r_gamma_curve_knees_16_17	0000 0000 0000 0000 dddd dddd dddd dddd	65019 (0x0000FDFB)
R13846(R0x00003616)	r_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13848(R0x00003618)	g_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13850(R0x0000361A)	g_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13852(R0x0000361C)	g_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13854(R0x0000361E)	g_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13856(R0x00003620)	g_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13858(R0x00003622)	g_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13860(R0x00003624)	g_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE)
R13862(R0x00003626)	g_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13864(R0x00003628)	g_gamma_curve_knees_16_17	0000 0000 0000 0000 dddd dddd dddd dddd	65019 (0x0000FDFB)
R13866(R0x0000362A)	g_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13868(R0x0000362C)	b_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13870(R0x0000362E)	b_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13872(R0x00003630)	b_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13874(R0x00003632)	b_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13876(R0x00003634)	b_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13878(R0x00003636)	b_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13880(R0x00003638)	b_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE)
R13882(R0x0000363A)	b_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13884(R0x0000363C)	b_gamma_curve_knees_16_17	0000 0000 0000 0000 dddd dddd dddd dddd	65019 (0x0000FDFB)
R13886(R0x0000363E)	b_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13888(R0x00003640)	p_g1_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13890(R0x00003642)	p_g1_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13892(R0x00003644)	p_g1_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13894(R0x00003646)	p_g1_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13896(R0x00003648)	p_g1_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13898(R0x0000364A)	p_r_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13900(R0x0000364C)	p_r_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13902(R0x0000364E)	p_r_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13904(R0x00003650)	p_r_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13906(R0x00003652)	p_r_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13908(R0x00003654)	p_b_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13910(R0x00003656)	p_b_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13912(R0x00003658)	p_b_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13914(R0x0000365A)	p_b_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13916(R0x0000365C)	p_b_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13918(R0x0000365E)	p_g2_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13920(R0x00003660)	p_g2_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13922(R0x00003662)	p_g2_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13924(R0x00003664)	p_g2_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13926(R0x00003666)	p_g2_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13952(R0x00003680)	p_g1_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13954(R0x00003682)	p_g1_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13956(R0x00003684)	p_g1_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13958(R0x00003686)	p_g1_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13960(R0x00003688)	p_g1_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13962(R0x0000368A)	p_r_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13964(R0x0000368C)	p_r_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13966(R0x0000368E)	p_r_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13968(R0x00003690)	p_r_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13970(R0x00003692)	p_r_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13972(R0x00003694)	p_b_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13974(R0x00003696)	p_b_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13976(R0x00003698)	p_b_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13978(R0x0000369A)	p_b_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13980(R0x0000369C)	p_b_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13982(R0x0000369E)	p_g2_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13984(R0x000036A0)	p_g2_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13986(R0x000036A2)	p_g2_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13988(R0x000036A4)	p_g2_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13990(R0x000036A6)	p_g2_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14016(R0x000036C0)	p_g1_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0(0x00000000)
R14018(R0x000036C2)	p_g1_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14020(R0x000036C4)	p_g1_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14022(R0x000036C6)	p_g1_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14024(R0x000036C8)	p_g1_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14026(R0x000036CA)	p_r_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14028(R0x000036CC)	p_r_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14030(R0x000036CE)	p_r_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14032(R0x000036D0)	p_r_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14034(R0x000036D2)	p_r_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14036(R0x000036D4)	p_b_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14038(R0x000036D6)	p_b_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14040(R0x000036D8)	p_b_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14042(R0x000036DA)	p_b_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14044(R0x000036DC)	p_b_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14046(R0x000036DE)	p_g2_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14048(R0x000036E0)	p_g2_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14050(R0x000036E2)	p_g2_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14052(R0x000036E4)	p_g2_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14054(R0x000036E6)	p_g2_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14080(R0x00003700)	p_g1_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14082(R0x00003702)	p_g1_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14084(R0x00003704)	p_g1_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14086(R0x00003706)	p_g1_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14088(R0x00003708)	p_g1_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14090(R0x0000370A)	p_r_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14092(R0x0000370C)	p_r_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14094(R0x0000370E)	p_r_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14096(R0x00003710)	p_r_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14098(R0x00003712)	p_r_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14100(R0x00003714)	p_b_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14102(R0x00003716)	p_b_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14104(R0x00003718)	p_b_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14106(R0x0000371A)	p_b_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14108(R0x0000371C)	p_b_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14110(R0x0000371E)	p_g2_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14112(R0x00003720)	p_g2_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14114(R0x00003722)	p_g2_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14116(R0x00003724)	p_g2_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14118(R0x00003726)	p_g2_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14144(R0x00003740)	p_g1_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14146(R0x00003742)	p_g1_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14148(R0x00003744)	p_g1_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14150(R0x00003746)	p_g1_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14152(R0x00003748)	p_g1_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14154(R0x0000374A)	p_r_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14156(R0x0000374C)	p_r_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14158(R0x0000374E)	p_r_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14160(R0x00003750)	p_r_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14162(R0x00003752)	p_r_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14164(R0x00003754)	p_b_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14166(R0x00003756)	p_b_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14168(R0x00003758)	p_b_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14170(R0x0000375A)	p_b_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14172(R0x0000375C)	p_b_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14174(R0x0000375E)	p_g2_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14176(R0x00003760)	p_g2_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14178(R0x00003762)	p_g2_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 28: 2: SOC2 Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14180(R0x00003764)	p_g2_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14182(R0x00003766)	p_g2_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

Table 29: SYSCTL Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R0(R0x00000000)	k22b_chip_id	0000 0000 0000 0000 ???? ???? ???? ????	8833 (0x00002281)
R6(R0x00000006)	i2c_control	0000 0000 0000 0000 dd0? ddd? 0000 0000	0 (0x00000000)
R16(R0x00000010)	pll_dividers	0000 0000 0000 0000 00dd dddd dddd dddd	530 (0x00000212)
R18(R0x00000012)	pll_p_dividers	0000 0000 0000 0000 00dd dddd ???? ????	0 (0x00000000)
R20(R0x00000014)	pll_control	0000 0000 0000 0000 ?d0d dddd dddd dddd	22596 (0x00005844)
R22(R0x00000016)	clocks_control	0000 0000 0000 0000 0ddd dddd 0ddd dddd	6783 (0x00001A7F)
R24(R0x00000018)	standby_control_and_status	0000 0000 0000 0000 0?00 0000 0?d? ?00?	16425 (0x00004029
R26(R0x0000001A)	reset_and_misc_control	0000 0000 0000 0000 dddd 0000 0000 000d	0 (0x00000000)
R28(R0x0000001C)	mcu_boot_mode	0000 0000 0000 0000 ???? ???? dddd dddd	1 (0x00000001)
R38(R0x00000026)	initialize_sensor	0000 0000 0000 0000 0000 0000 0000 00dd	1 (0x00000001)
R48(R0x00000030)	pad_slew	0000 0000 0000 0000 0ddd 0ddd 0ddd 0ddd	1024 (0x00000400)
R50(R0x00000032)	pad_control	0000 0000 0000 0000 dddd 00d0 dd0d 000d	209 (0x000000D1)
R52(R0x00000034)	pad_gpi_status	0000 0000 0000 0000 ???? 000? ???? ????	0 (0x00000000)
R64(R0x00000040)	command_register	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R80(R0x00000050)	k22b_rtl_ver	0000 0000 0000 0000 ???? ???? ???? ????	2 (0x00000002)
R96(R0x00000060)	bist_control	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R98(R0x00000062)	bist_test	0000 0000 0000 0000 000d dddd dddd dddd	0 (0x00000000)
R100(R0x00000064)	bist_test_resume	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R102(R0x00000066)	bist_debug	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R104(R0x00000068)	bist_hold	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)

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Table 29: SYSCTL Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R106(R0x0000006A)	bist_test_done	0000 0000 0000 0000 000? ???? ???? ????	0 (0x00000000)
R108(R0x0000006C)	bist_fail	0000 0000 0000 0000 000? ???? ???? ????	0 (0x00000000)
R110(R0x0000006E)	bist_start_retention	0000 0000 0000 0000 0000 ???? ???? ????	0 (0x00000000)

Table 30: RX_SS Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R256(R0x00000100)	testp_ctl	0000 0000 0000 0000 0000 0ddd ddd0 0ddd	0 (0x00000000)
R258(R0x00000102)	test_pxl_red	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R260(R0x00000104)	test_pxl_g1	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R262(R0x00000106)	test_pxl_g2	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R264(R0x00000108)	test_pxl_blue	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R266(R0x0000010A)	row_start	0000 0000 0000 0000 0000 0ddd dddd dddd	22 (0x00000016)
R268(R0x0000010C)	col_start	0000 0000 0000 0000 0000 dddd dddd dddd	109 (0x0000006D)
R270(R0x0000010E)	row_end	0000 0000 0000 0000 0000 0ddd dddd dddd	510 (0x000001FE)
R272(R0x00000110)	col_end	0000 0000 0000 0000 0000 dddd dddd dddd	757 (0x000002F5)
R276(R0x00000114)	testp_x	0000 0000 0000 0000 000d dddd dddd dddd	857 (0x00000359)
R278(R0x00000116)	testp_y	0000 0000 0000 0000 000d dddd dddd dddd	524 (0x0000020C)

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Table 31: XDMA Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R2434(R0x00000982)	access_ctl_stat	0000 0000 0000 0000 0000 0000 dd0? ???d	0 (0x00000000)
R2442(R0x0000098A)	physical_address_access	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2446(R0x0000098E)	logical_address_access	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2448(R0x00000990)	mcu_variable_data0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2450(R0x00000992)	mcu_variable_data1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2452(R0x00000994)	mcu_variable_data2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2454(R0x00000996)	mcu_variable_data3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2456(R0x00000998)	mcu_variable_data4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2458(R0x0000099A)	mcu_variable_data5	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2460(R0x0000099C)	mcu_variable_data6	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2462(R0x0000099E)	mcu_variable_data7	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

Table 32: TX_SS Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R15360(R0x00003C00)	parallel_bus_ctrl	0000 0000 0000 0000 000d 000d 000d 0ddd	4096 (0x00001000)
R15362(R0x00003C02)	gpo	0000 0000 0000 0000 dddd 000d dddd dddd	0 (0x00000000)
R15364(R0x00003C04)	vdac_cal_1	0000 0000 0000 0000 00dd dddd dd0d dddd	8400 (0x000020D0)
R15366(R0x00003C06)	vdac_cal_2	0000 0000 0000 0000 0000 0000 0000 dddd	0 (0x00000000)
R15368(R0x00003C08)	tvenc_ctrl_1	0000 0000 0000 0000 00dd 000d 000d 000d	8193 (0x00002001)
R15370(R0x00003C0A)	tvenc_ctrl_2	0000 0000 0000 0000 00dd 00dd 00dd 00dd	0 (0x00000000)
R15372(R0x00003C0C)	checksum_ctrl	0000 0000 0000 0000 0000 0000 0000 000d	1 (0x00000001)
R15374(R0x00003C0E)	checksum_data	0000 0000 0000 0000 ???? ???? ???? ????	65535 (0x0000FFFF)
R15376(R0x00003C10)	vdac_test	0000 0000 0000 0000 00dd 00dd dddd dddd	0 (0x00000000)

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Table 33: OVERLAY_SS Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20224(R0x00004F00)	overlay_status	0000 0000 0000 0000 ??00 0000 00?? ????	49152 (0x0000C000)
R20226(R0x00004F02)	overlay_control	0000 0000 0000 0000 d000 0000 0000 000d	0 (0x00000000)
R20228(R0x00004F04)	overlay_interrupt_control	0000 0000 0000 0000 0000 0000 0000 0ddd	X
R20230(R0x00004F06)	overlay_interrupt_mask	0000 0000 0000 0000 0000 0000 0000 0ddd	7 (0x00000007)
R20232(R0x00004F08)	overlay_layer0_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000
R20234(R0x00004F0A)	overlay_layer1_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20236(R0x00004F0C)	overlay_layer2_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20238(R0x00004F0E)	overlay_layer3_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20240(R0x00004F10)	overlay_calibration	0000 0000 0000 0000 00dd dddd 00dd dddd	8224 (0x00002020)
R20242(R0x00004F12)	overlay_testmode	0000 0000 0000 0000 0000 0000 0000 dddd	0 (0x00000000)
R20246(R0x00004F16)	overlay_char_control0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R20248(R0x00004F18)	overlay_char_control1	0000 0000 0000 0000 d000 0000 00dd dddd	0 (0x00000000)
R20250(R0x00004F1A)	overlay_char_descriptor0_1	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20252(R0x00004F1C)	overlay_char_descriptor2_3	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20254(R0x00004F1E)	overlay_char_descriptor4_5	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20256(R0x00004F20)	overlay_char_descriptor6_7	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20258(R0x00004F22)	overlay_char_descriptor8_9	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20260(R0x00004F24)	overlay_char_descriptor10_11	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20262(R0x00004F26)	overlay_char_descriptor12_13	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20264(R0x00004F28)	overlay_char_descriptor14_15	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20266(R0x00004F2A)	overlay_char_descriptor16_17	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20268(R0x00004F2C)	overlay_char_descriptor18_19	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20270(R0x00004F2E)	overlay_char_descriptor20_21	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20272(R0x00004F30)	overlay_char_backcolour0	0000 0000 0000 0000 dddd dd00 dddd d000	0 (0x00000000)

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Table 33: OVERLAY_SS Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20274(R0x00004F32)	overlay_char_backcolour1	0000 0000 0000 0000 dddd d000 dddd 0000	0 (0x00000000)
R20276(R0x00004F34)	overlay_char_colour0	0000 0000 0000 0000 dddd dd00 dddd d000	0 (0x00000000)
R20278(R0x00004F36)	overlay_char_colour1	0000 0000 0000 0000 dddd d000 dddd 0000	0 (0x00000000)
R20280(R0x00004F38)	overlay_char_x_offset	0000 0000 0000 0000 0000 000d dddd dddd	0 (0x00000000)
R20282(R0x00004F3A)	overlay_char_y_offset	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

Table 34: CALIB_STATS_SS Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R19712(R0x00004D00)	calib_stats_acc0_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19714(R0x00004D02)	calib_stats_acc0_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19716(R0x00004D04)	calib_stats_acc1_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19718(R0x00004D06)	calib_stats_acc1_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19720(R0x00004D08)	calib_stats_acc2_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19722(R0x00004D0A)	calib_stats_acc2_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19724(R0x00004D0C)	calib_stats_acc3_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19726(R0x00004D0E)	calib_stats_acc3_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19728(R0x00004D10)	calib_stats_acc4_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19730(R0x00004D12)	calib_stats_acc4_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19732(R0x00004D14)	calib_stats_acc5_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19734(R0x00004D16)	calib_stats_acc5_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19736(R0x00004D18)	calib_stats_acc6_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19738(R0x00004D1A)	calib_stats_acc6_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19740(R0x00004D1C)	calib_stats_acc7_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19742(R0x00004D1E)	calib_stats_acc7_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19744(R0x00004D20)	calib_stats_x_addr_start	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

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Table 34: CALIB_STATS_SS Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R19746(R0x00004D22)	calib_stats_x_addr_end	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19748(R0x00004D24)	calib_stats_y_addr_start	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19750(R0x00004D26)	calib_stats_y_addr_end	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19752(R0x00004D28)	calib_stats_ctrl	0000 0000 0000 0000 0000 0000 0000 0d?d	0 (0x00000000)

Table 35: KEEPSYNC_SSRegisters

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20192(R0x00004EE0)	keepsync_status	0000 0000 0000 0000 0000 0000 0000 000?	0 (0x00000000)
R20194(R0x00004EE2)	keepsync_control	0000 0000 0000 0000 0000 0000 0000 dddd	1 (0x00000001)

Variables Sorted by Address

Table 36: 10: AE_Track Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(10, 2) VAR(0x0A, 0x00000002)	ae_track_mode	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(10, 4) VAR(0x0A, 0x00000004)	ae_track_algo	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(10, 18) VAR(0x0A, 0x00000012)	ae_track_target	0000 0000 0000 0000 dddd dddd dddd dddd	75 (0x0000004B)
VAR(10, 20) VAR(0x0A, 0x00000014)	ae_track_gate	0000 0000 0000 0000 dddd dddd dddd dddd	4 (0x00000004)
VAR(10, 26) VAR(0x0A, 0x0000001A)	ae_track_jump_divisor	0000 0000 0000 0000 dddd dddd dddd dddd	3 (0x00000003)

Table 37: 11: AWB Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(11, 10) VAR(0x0B, 0x0000000A)	awb_ccm_0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 12) VAR(0x0B, 0x0000000C)	awb_ccm_1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000
VAR(11, 14) VAR(0x0B, 0x0000000E)	awb_ccm_2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 16) VAR(0x0B, 0x00000010)	awb_ccm_3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 18) VAR(0x0B, 0x00000012)	awb_ccm_4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 37: 11: AWB Variables (continued)

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(11, 20) VAR(0x0B, 0x00000014)	awb_ccm_5	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11,22) VAR(0x0B, 0x00000016)	awb_ccm_6	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 24) VAR(0x0B, 0x00000018)	awb_ccm_7	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000
VAR(11, 26) VAR(0x0B, 0x0000001A)	awb_ccm_8	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 28) VAR(0x0B, 0x0000001C)	awb_ccm_9	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 30) VAR(0x0B, 0x0000001E)	awb_ccm_10	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(11, 54) VAR(0x0B, 0x00000036)	awb_ccmposition	0000 0000 0000 0000 dddd dddd dddd dddd	64 (0x00000040)

Table 38: 14: Stat Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(14, 120) VAR(0x0E, 0x00000078)	stat_inv_brightness_metric	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

Table 39: Low Light Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(15, 4) VAR(0x0F, 0x00000004)	ll_algo	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(15, 60) VAR(0x0F, 0x00000006)	ll_cluster_dc_th	0000 0000 0000 0000 dddd dddd dddd dddd	1 (0x00000001)
VAR(15,98) VAR(0x0F, 0x00000062)	ll_tonal_curve_med	0000 0000 0000 0000 dddd dddd dddd dddd	127 (0x0000007F)
VAR(15, 100) VAR(0x0F,0x00000064)	ll_tonal_curve_low	0000 0000 0000 0000 dddd dddd dddd dddd	127 (0x0000007F)

Table 40: Cam1Control Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(18, 22) VAR(0x12, 0x00000016)	cam1_sensor_0_fine_correction	0000 0000 0000 0000 dddd dddd dddd dddd	49 (0x00000031)
VAR(18, 34) VAR(0x12, 0x00000022)	cam1_sensor_0_ae_initial_window_xstart	0000 0000 0000 0000 dddd dddd dddd dddd	4 (0x00000004)
VAR(18, 36) VAR(0x12, 0x00000024)	cam1_sensor_0_ae_initial_window_ystart	0000 0000 0000 0000 dddd dddd dddd dddd	4 (0x00000004)
VAR(18, 38) VAR(0x12, 0x00000026)	cam1_sensor_0_ae_initial_window_xend	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 40) VAR(0x12, 0x00000028)	cam1_sensor_0_ae_initial_window_yend	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 40: Cam1Control Variables (continued)

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(18, 76) VAR(0x12, 0x0000004C)	cam1_sensor_1_fine_correction	0000 0000 0000 0000 dddd dddd dddd dddd	104 (0x00000068)
VAR(18, 146) VAR(0x12, 0x00000092)	cam1_sensor_x_offset	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 148) VAR(0x12, 0x00000094)	cam1_sensor_y_offset	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 154) VAR(0x12, 0x0000009A)	cam1_aet_skip_frames	0000 0000 0000 0000 dddd dddd dddd dddd	1 (0x00000001)
VAR(18, 172) VAR(0x12, 0x000000AC)	cam1_aet_ae_virt_gain_th_cg	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 174) VAR(0x12, 0x000000AE)	cam1_aet_ae_virt_gain_th_dcg	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 176) VAR(0x12, 0x000000B0)	cam1_aet_ae_column_gain_0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 178) VAR(0x12, 0x000000B2)	cam1_aet_ae_column_gain_1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 180) VAR(0x12, 0x000000B4)	cam1_aet_ae_column_gain_2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 182) VAR(0x12, 0x000000B6)	cam1_aet_ae_column_gain_3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 184) VAR(0x12, 0x000000B8)	cam1_aet_ae_column_gain_4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 186) VAR(0x12, 0x000000BA)	cam1_aet_ae_dcgain	0000 0000 0000 0000 dddd dddd dddd dddd	160 (0x000000A0)
VAR(18, 206) VAR(0x12, 0x000000CE)	cam1_awb_ccm_l_0	0000 0000 0000 0000 dddd dddd dddd dddd	473 (0x000001D9)
VAR(18, 208) VAR(0x12, 0x000000D0)	cam1_awb_ccm_l_1	0000 0000 0000 0000 dddd dddd dddd dddd	65285 (0x0000FF05)
VAR(18, 210) VAR(0x12, 0x000000D2)	cam1_awb_ccm_l_2	0000 0000 0000 0000 dddd dddd dddd dddd	63 (0x0000003F)
VAR(18, 212) VAR(0x12, 0x000000D4)	cam1_awb_ccm_l_3	0000 0000 0000 0000 dddd dddd dddd dddd	65475 (0x0000FFC3)
VAR(18,l 214) VAR(0x12, 0x000000D6)	cam1_awb_ccm_l_4	0000 0000 0000 0000 dddd dddd dddd dddd	306 (0x00000132)
VAR(18, 216) VAR(0x12, 0x000000D8)	cam1_awb_ccm_l_5	0000 0000 0000 0000 dddd dddd dddd dddd	39 (0x00000027)
VAR(18, 218) VAR(0x12, 0x000000DA)	cam1_awb_ccm_l_6	0000 0000 0000 0000 dddd dddd dddd dddd	65461 (0x0000FFB5)
VAR(18, 220) VAR(0x12, 0x000000DC)	cam1_awb_ccm_l_7	0000 0000 0000 0000 dddd dddd dddd dddd	65188 (0x0000FEA4)
VAR(18, 222) VAR(0x12, 0x000000DE)	cam1_awb_ccm_l_8	0000 0000 0000 0000 dddd dddd dddd dddd	706 (0x000002C2)
VAR(18, 224) VAR(0x12, 0x000000E0)	cam1_awb_ccm_l_9	0000 0000 0000 0000 dddd dddd dddd dddd	17 (0x00000011)
VAR(18, 226) VAR(0x12, 0x000000E2)	cam1_awb_ccm_l_10	0000 0000 0000 0000 dddd dddd dddd dddd	82 (0x00000052)
VAR(18, 228) VAR(0x12, 0x000000E4)	cam1_awb_ccm_rl_0	0000 0000 0000 0000 dddd dddd dddd dddd	65423 (0x0000FF8F)

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Table 40: Cam1Control Variables (continued)

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(18, 230) VAR(0x12, 0x000000E6)	cam1_awb_ccm_rl_1	0000 0000 0000 0000 dddd dddd dddd dddd	168 (0x000000A8)
VAR(18, 232) VAR(0x12, 0x000000E8)	cam1_awb_ccm_rl_2	0000 0000 0000 0000 dddd dddd dddd dddd	65480 (0x0000FFC8)
VAR(18, 234) VAR(0x12, 0x000000EA)	cam1_awb_ccm_rl_3	0000 0000 0000 0000 dddd dddd dddd dddd	18 (0x00000012)
VAR(18, 236) VAR(0x12, 0x000000EC)	cam1_awb_ccm_rl_4	0000 0000 0000 0000 dddd dddd dddd dddd	15 (0x0000000F)
VAR(18, 238) VAR(0x12, 0x000000EE)	cam1_awb_ccm_rl_5	0000 0000 0000 0000 dddd dddd dddd dddd	65502 (0x0000FFDE)
VAR(18, 240) VAR(0x12, 0x000000F0)	cam1_awb_ccm_rl_6	0000 0000 0000 0000 dddd dddd dddd dddd	84 (0x00000054)
VAR(18, 242) VAR(0x12, 0x000000F2)	cam1_awb_ccm_rl_7	0000 0000 0000 0000 dddd dddd dddd dddd	160 (0x000000A0)
VAR(18, 244) VAR(0x12, 0x000000F4)	cam1_awb_ccm_rl_8	000 0000 0000 0000 dddd dddd dddd dddd	65290 (0x0000FF0A)
VAR(18, 246) VAR(0x12, 0x000000F6)	cam1_awb_ccm_rl_9	0000 0000 0000 0000 dddd dddd dddd dddd	17 (0x00000011)
VAR(18, 248) VAR(0x12, 0x000000F8)	cam1_awb_ccm_rl_10	0000 0000 0000 0000 dddd dddd dddd dddd	65492 (0x0000FFD4)
VAR(18, 250) VAR(0x12, 0x000000FA)	cam1_awb_ll_ccm_0	0000 0000 0000 0000 dddd dddd dddd dddd	77 (0x0000004D)
VAR(18, 252) VAR(0x12, 0x000000FC)	cam1_awb_ll_ccm_1	0000 0000 0000 0000 dddd dddd dddd dddd	150 (0x00000096)
VAR(18, 254) VAR(0x12, 0x000000FE)	cam1_awb_ll_ccm_2	0000 0000 0000 0000 dddd dddd dddd dddd	29 (0x0000001D)
VAR(18, 256) VAR(0x12, 0x00000100)	cam1_awb_ll_ccm_3	0000 0000 0000 0000 dddd dddd dddd dddd	77 (0x0000004D)
VAR(18, 258) VAR(0x12, 0x00000102)	cam1_awb_ll_ccm_4	0000 0000 0000 0000 dddd dddd dddd dddd	150 (0x00000096)
VAR(18, 260) VAR(0x12, 0x00000104)	cam1_awb_ll_ccm_5	0000 0000 0000 0000 dddd dddd dddd dddd	29 (0x0000001D)
VAR(18, 262) VAR(0x12, 0x00000106)	cam1_awb_ll_ccm_6	0000 0000 0000 0000 dddd dddd dddd dddd	77 (0x0000004D)
VAR(18, 264) VAR(0x12, 0x00000108)	cam1_awb_ll_ccm_7	0000 0000 0000 0000 dddd dddd dddd dddd	150 (0x00000096)
VAR(18, 266) VAR(0x12, 0x0000010A)	cam1_awb_ll_ccm_8	0000 0000 0000 0000 dddd dddd dddd dddd	29 (0x0000001D)
VAR(18, 272) VAR(0x12, 0x00000110)	cam1_awb_awb_xscale	0000 0000 0000 0000 dddd dddd dddd dddd	3 (0x00000003
VAR(18, 274) VAR(0x12, 0x00000112)	cam1_awb_awb_yscale	0000 0000 0000 0000 dddd dddd dddd dddd	2 (0x00000002)
VAR(18, 276) VAR(0x12, 0x00000114)	cam1_awb_awb_weights_0	0000 0000 0000 0000 dddd dddd dddd dddd	18627 (0x000048C3)
VAR(18, 278) VAR(0x12, 0x00000116)	cam1_awb_awb_weights_1	0000 0000 0000 0000 dddd dddd dddd dddd	60589 (0x0000ECAD)
VAR(18, 280) VAR(0x12, 0x00000118)	cam1_awb_awb_weights_2	0000 0000 0000 0000 dddd dddd dddd dddd	65431 (0x0000FF97

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Table 40: Cam1Control Variables (continued)

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(18, 282) VAR(0x12, 0x0000011A)	cam1_awb_awb_weights_3	0000 0000 0000 0000 dddd dddd dddd dddd	6301 (0x0000189D
VAR(18, 284) VAR(0x12, 0x0000011C)	cam1_awb_awb_weights_4	0000 0000 0000 0000 dddd dddd dddd dddd	37123 (0x00009103)
VAR(18, 286) VAR(0x12, 0x0000011E)	cam1_awb_awb_weights_5	0000 0000 0000 0000 dddd dddd dddd dddd	45054 (0x0000AFFE)
VAR(18, 288) VAR(0x12, 0x00000120)	cam1_awb_awb_weights_6	0000 0000 0000 0000 dddd dddd dddd dddd	16431 (0x0000402F)
VAR(18, 290) VAR(0x12, 0x00000122)	cam1_awb_awb_weights_7	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 292) VAR(0x12, 0x00000124)	cam1_awb_awb_xshift_pre_adj	0000 0000 0000 0000 dddd dddd dddd dddd	58 (0x0000003A
VAR(18, 294) VAR(0x12, 0x00000126)	cam1_awb_awb_yshift_pre_adj	0000 0000 0000 0000 dddd dddd dddd dddd	58 (0x0000003A)
VAR(18, 300) VAR(0x12, 0x0000012C)	cam1_stat_gain_metric_predivider	0000 0000 0000 0000 dddd dddd dddd dddd	17 (0x00000011)
VAR(18, 302) VAR(0x12, 0x0000012E)	cam1_stat_brightness_metric_predivider	0000 0000 0000 0000 dddd dddd dddd dddd	10 (0x0000000A)
VAR(18, 304) VAR(0x12, 0x00000130)	cam1_ll_start_brightness	0000 0000 0000 0000 dddd dddd dddd dddd	40 (0x00000028)
VAR(18, 306) VAR(0x12, 0x00000132)	cam1_ll_stop_brightness	0000 0000 0000 0000 dddd dddd dddd dddd	200 (0x000000C8)
VAR(18, 308) VAR(0x12, 0x00000134)	cam1_ll_start_saturation	0000 0000 0000 0000 dddd dddd dddd dddd	128 (0x00000080)
VAR(18, 310) VAR(0x12, 0x00000136)	cam1_ll_end_saturation	0000 0000 0000 0000 dddd dddd dddd dddd	48 (0x00000030)
VAR(18, 312) VAR(0x12, 0x00000138)	cam1_ll_start_desaturation	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(18, 318) VAR(0x12, 0x0000013E)	cam1_ll_ll_start_1	0000 0000 0000 0000 dddd dddd dddd dddd	2 (0x00000002)
VAR(18, 320) VAR(0x12, 0x00000140)	cam1_ll_ll_start_2	0000 0000 0000 0000 dddd dddd dddd dddd	2 (0x00000002)
VAR(18, 322) VAR(0x12, 0x00000142)	cam1_ll_ll_stop_0	0000 0000 0000 0000 dddd dddd dddd dddd	104 (0x00000068)
VAR(18, 324) VAR(0x12, 0x00000144)	cam1_ll_ll_stop_1	0000 0000 0000 0000 dddd dddd dddd dddd	1 (0x00000001)
VAR(18, 326) VAR(0x12, 0x00000146)	cam1_ll_ll_stop_2	0000 0000 0000 0000 dddd dddd dddd dddd	9 (0x00000009)
VAR(18, 344) VAR(0x12, 0x00000158)	cam1_ll_start_gamma_bm	0000 0000 0000 0000 dddd dddd dddd dddd	40 (0x00000028)
VAR(18, 346) VAR(0x12, 0x0000015A)	cam1_ll_stop_gamma_bm	0000 0000 0000 0000 dddd dddd dddd dddd	200 (0x000000C8)

Table 41: 23: SysCtrl Variables

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(23, 40) VAR(0x17, 0x00000028)	sys_refresh_mask	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 42: 31: Command Handler

Variable Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
VAR(31, 0) VAR(0x1F, 0x00000000)	cmd_handler_params_pool_0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31,2) VAR(0x1F, 0x00000002)	cmd_handler_params_pool_1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31, 4) VAR(0x1F, 0x00000004)	cmd_handler_params_pool_2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31,6) VAR(0x1F, 0x00000006)	cmd_handler_params_pool_3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31, 8) VAR(0x1F, 0x00000008)	cmd_handler_params_pool_4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31, 10) VAR(0x1F, 0x0000000A)	cmd_handler_params_pool_5	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31, 12) VAR(0x1F, 0x0000000C)	cmd_handler_params_pool_6	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
VAR(31, 14) VAR(0x1F, 0x0000000E)	cmd_handler_params_pool_7	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Registers and Variables Sorted by Name

Registers Sorted by Name

Table 43: 0: Core Registers Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12334(R0x0000302E)	analogue_gain_code_blue_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12328(R0x00003028)	analogue_gain_code_global_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12336(R0x00003030)	analogue_gain_code_greenb_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12330(R0x0000302A)	analogue_gain_code_greenr_	0000 0000 0000 0000 0000 0000 0ddd dddd	12(0x0000000C)
R12332(R0x0000302C)	analogue_gain_code_red_	0000 0000 0000 0000 0000 0000 0ddd dddd	12 (0x0000000C)
R12376(R0x00003058)	blue_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12306(R0x00003012)	coarse_integration_time_	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R12500(R0x000030D4)	column_correction	0000 0000 0000 0000 dddd 00dd dddd dddd	32 (0x00000020)
R16076(R0x00003ECC)	dac_ld_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	271 (0x0000010F)
R16088(R0x00003ED8)	dac_ld_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	34708 (0x00008794)
R16104(R0x00003EE8)	dac_ld_28_29	0000 0000 0000 0000 dddd dddd dddd dddd	11008 (0x00002B00)
R16084(R0x00003ED4)	dac_ld_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	2048 (0x00000800)
R12472(R0x000030B8)	dark_blue_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12354(R0x00003042)	dark_control2	0000 0000 0000 0000 dddd dddd dddd 00dd	8209 (0x00002011)
R12470(R0x000030B6)	dark_green1_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12476(R0x000030BC)	dark_green2_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12474(R0x000030BA)	dark_red_average	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R12318(R0x0000301E)	data_pedestal_	0000 0000 0000 0000 0000 00dd dddd dddd	42 (0x0000002A)
R12342(R0x00003036)	digital_gain_blue_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12344(R0x00003038)	digital_gain_greenb_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12338(R0x00003032)	digital_gain_greenr_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)

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Table 43: 0: Core Registers Sorted by Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12340(R0x00003034)	digital_gain_red_	0000 0000 0000 0000 0000 0ddd 0000 0000	256 (0x00000100)
R12312(R0x00003018)	extra_delay	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12304(R0x00003010)	fine_correction	0000 0000 0000 0000 0000 dddd dddd dddd	49 (0x00000031)
R12308(R0x00003014)	fine_integration_time_	0000 0000 0000 0000 0000 dddd dddd dddd	164 (0x000000A4)
R12358(R0x00003046)	flash	0000 0000 0000 0000 dddd dddd d000 0000	1536 (0x00000600)
R12360(R0x00003048)	flash_count	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R12298(R0x0000300A)	frame_length_lines_	0000 0000 0000 0000 dddd dddd dddd dddd	525 (0x0000020D)
R12348(R0x0000303C)	frame_status	0000 0000 0000 0000 0000 0000 0000 00??	0 (0x00000000)
R12382(R0x0000305E)	global_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12326(R0x00003026)	gpi_status	0000 0000 0000 0000 dddd dd00 0ddd dddd	64639 (0x0000FC7F)
R12374(R0x00003056)	green1_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12380(R0x0000305C)	green2_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12776(R0x000031E8)	horizontal_cursor_position_	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12780(R0x000031EC)	horizontal_cursor_width_	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12300(R0x0000300C)	line_length_pck_	0000 0000 0000 0000 0000 dddd dddd dddd	858 (0x0000035A)
R12288(R0x00003000)	model_id_	0000 0000 0000 0000 dddd dddd dddd dddd	8833 (0x00002281)
R12324(R0x00003024)	pixel_order_	0000 0000 0000 0000 0000 0000 0000 00??	0 (0x00000000)
R12352(R0x00003040)	read_mode	0000 0000 0000 0000 dd00 dddd dddd dddd	65 (0x00000041)
R12378(R0x0000305A)	red_gain	0000 0000 0000 0000 0ddd 0000 dddd dddd	4144 (0x00001030)
R12314(R0x0000301A)	reset_register	0000 0000 0000 0000 dd0d 0ddd dddd dddd	4312 (0x000010D8)
R12310(R0x00003016)	row_speed	0000 0000 0000 0000 0000 0ddd 0ddd 0ddd	273 (0x00000111)
R12320(R0x00003020)	software_reset_	0000 0000 0000 0000 0000 000d 0000 0000	0 (0x00000000)
R12406(R0x00003076)	test_data_blue_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12408(R0x00003078)	test_data_greenb_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

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Table 43: 0: Core Registers Sorted by Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12404(R0x00003074)	test_data_greenr_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12402(R0x00003072)	test_data_red_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12400(R0x00003070)	test_pattern_mode_	0000 0000 0000 0000 0000 000d 0000 0ddd	0 (0x00000000)
R12778(R0x000031EA)	vertical_cursor_position_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12782(R0x000031EE)	vertical_cursor_width_	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12296(R0x00003008)	x_addr_end_	0000 0000 0000 0000 0000 00dd dddd dddd	663 (0x00000297)
R12292(R0x00003004)	x_addr_start_	0000 0000 0000 0000 0000 00dd dddd dddd	16 (0x00000010)
R12448(R0x000030A0)	x_even_inc_	0000 0000 0000 0000 0000 0000 0000 000?	1 (0x00000001)
R12450(R0x000030A2)	x_odd_inc_	0000 0000 0000 0000 0000 0000 0000 0ddd	1 (0x00000001)
R12294(R0x00003006)	y_addr_end_	0000 0000 0000 0000 0000 dddd dddd dddd	499 (0x000001F3)
R12290(R0x00003002)	y_addr_start_	0000 0000 0000 0000 0000 dddd dddd dddd	12 (0x0000000C)
R12452(R0x000030A4)	y_even_inc_	0000 0000 0000 0000 0000 0000 0000 000?	1 (0x00000001)
R12454(R0x000030A6)	y_odd_inc_	0000 0000 0000 0000 0000 0000 0000 0ddd	1 (0x00000001)

Table 44: 1: SOC1 Registers Sorted By Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12906(R0x0000326A)	aperture_parameters_1d	0000 0000 0000 0000 00dd dddd dddd dddd	4616 (0x00001208
R12908(R0x0000326C)	aperture_parameters_2d	0000 0000 0000 0000 0ddd dddd dddd dddd	4616 (0x00001208)
R12852(R0x00003234)	awb_debug_weight	0000 0000 0000 0000 0000 0000 000d dddd	1 (0x00000001)
R12898(R0x00003262)	awb_luma_th	0000 0000 0000 0000 dddd dddd dddd dddd	65288 (0x0000FF08)
R12858(R0x0000323A)	awb_norm_sumb	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12856(R0x00003238)	wb_norm_sumg	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12854(R0x00003236)	awb_norm_sumr	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12896(R0x00003260)	awb_weight_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)

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Table 44: 1: SOC1 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12904(R0x00003268)	awb_weight_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R12866(R0x00003242)	awb_weight_r0	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12868(R0x00003244)	awb_weight_r1	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12870(R0x00003246)	awb_weight_r2	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12872(R0x00003248)	awb_weight_r3	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12874(R0x0000324A)	awb_weight_r4	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12876(R0x0000324C)	awb_weight_r5	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12878(R0x0000324E)	awb_weight_r6	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12880(R0x00003250)	awb_weight_r7	0000 0000 0000 0000 dddd dddd dddd dddd	20480 (0x00005000)
R12902(R0x00003266)	awb_weight_th	0000 0000 0000 0000 0000 0000 dddd dddd	145 (0x00000091)
R12892(R0x0000325C)	awb_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R12888(R0x00003258)	awb_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000
R12894(R0x0000325E)	awb_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R12890(R0x0000325A)	awb_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000
R12864(R0x00003240)	awb_xy_scale	0000 0000 0000 0000 0000 0000 dddd dddd	51 (0x00000033)
R12860(R0x0000323C)	awb_x_shift	0000 0000 0000 0000 0000 0ddd dddd dddd	3 (0x00000003)
R12862(R0x0000323E)	awb_y_shift	0000 0000 0000 0000 0000 0ddd dddd dddd	3 (0x00000003)
R12918(R0x00003276)	black_level_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R13018(R0x000032DA)	blue_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R12928(R0x00003280)	blue_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12990(R0x000032BE)	blue_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R12996(R0x000032C4)	ccm_elements_1_and_2	0000 0000 0000 0000 dddd dddd dddd dddd	55790 (0x0000D9EE)
R12998(R0x000032C6)	ccm_elements_3_and_4	0000 0000 0000 0000 dddd dddd dddd dddd	11035 (0x00002B1B)
R13000(R0x000032C8)	ccm_elements_5_and_6	0000 0000 0000 0000 dddd dddd dddd dddd	35818 (0x00008BEA)

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Table 44: 1: SOC1 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13002(R0x000032CA)	ccm_elements_7_and_8	0000 0000 0000 0000 dddd dddd dddd dddd	32022 (0x00007D16)
R13004(R0x000032CC)	ccm_elements_9_and_signs	0000 0000 0000 0000 00dd dddd dddd dddd	11714 (0x00002DC2)
R12994(R0x000032C2)	ccm_exp_high_byte	0000 0000 0000 0000 0000 dddd dddd dddd	1828 (0x00000724)
R12992(R0x000032C0)	ccm_exp_low_byte	0000 0000 0000 0000 0ddd dddd dddd dddd	14627 (0x00003923)
R12816(R0x00003210)	color_pipeline_control	0000 0000 0000 0000 0000 0d00 d0dd d000	176 (0x000000B0)
R12960(R0x000032A0)	dkdelta_ccm_cc1	0000 0000 0000 0000 0000 000d dddd dddd	322 (0x00000142)
R12962(R0x000032A2)	dkdelta_ccm_cc2	0000 0000 0000 0000 0000 000d dddd dddd	217 (0x000000D9)
R12964(R0x000032A4)	dkdelta_ccm_cc3	0000 0000 0000 0000 0000 000d dddd dddd	485 (0x000001E5)
R12966(R0x000032A6)	dkdelta_ccm_cc4	0000 0000 0000 0000 0000 000d dddd dddd	43 (0x0000002B)
R12968(R0x000032A8)	dkdelta_ccm_cc5	0000 0000 0000 0000 0000 000d dddd dddd	327 (0x00000147)
R12970(R0x000032AA)	dkdelta_ccm_cc6	0000 0000 0000 0000 0000 000d dddd dddd	142 (0x0000008E)
R12972(R0x000032AC)	dkdelta_ccm_cc7	0000 0000 0000 0000 0000 000d dddd dddd	490 (0x000001EA)
R12974(R0x000032AE)	dkdelta_ccm_cc8	0000 0000 0000 0000 0000 000d dddd dddd	125 (0x0000007D
R12976(R0x000032B0)	dkdelta_ccm_cc9	0000 0000 0000 0000 0000 000d dddd dddd	409 (0x00000199)
R12978(R0x000032B2)	dkdelta_ccm_ctl	0000 0000 0000 0000 00dd dddd dddd dddd	8980 (0x00002314)
R12982(R0x000032B6)	dkdelta_ccm_exp1	0000 0000 0000 0000 0ddd dddd dddd dddd	18724 (0x00004924)
R12984(R0x000032B8)	dkdelta_ccm_exp2	0000 0000 0000 0000 0000 dddd dddd dddd	2340 (0x00000924
R12980(R0x000032B4)	dkdelta_ccm_scale	0000 0000 0000 0000 0000 00dd dddd dddd	528 (0x00000210
R12942(R0x0000328E)	dm_edge_th	0000 0000 0000 0000 0000 0000 dddd dddd	12 (0x0000000C)
R13052(R0x000032FC)	fd_avg	0000 0000 0000 0000 0000 0000 ???? ????	0 (0x00000000)
R13040(R0x000032F0)	fd_win_size_hi	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000
R13022(R0x000032DE)	fd_win_size_lo	0000 0000 0000 0000 dddd dddd dddd dddd	3200 (0x00000C80)
R13048(R0x000032F8)	fd_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13042(R0x000032F2)	fd_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)

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Table 44: 1: SOC1 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13050(R0x000032FA)	fd_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	4 (0x00000004)
R13044(R0x000032F4)	fd_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R12884(R0x00003254)	first_color	0000 0000 0000 0000 0000 0000 0000 00dd	0 (0x00000000)
R13100(R0x0000332C)	fm_blank_frames	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R13108(R0x00003334)	fm_frame_count	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13106(R0x00003332)	fm_line_count	0000 0000 0000 0000 0000 ???? ???? ????	0 (0x00000000)
R13014(R0x000032D6)	green1_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R12924(R0x0000327C)	green1_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R13016(R0x000032D8)	green2_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R12926(R0x0000327E)	green2_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8)
R12988(R0x000032BC)	green_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R13300(R0x000033F4)	kernel_config	0000 0000 0000 0000 0000 0000 ddd0 dddd	3 (0x00000003)
R12886(R0x00003256)	last_row	0000 0000 0000 0000 0000 0ddd dddd dddd	483 (0x000001E3
R12910(R0x0000326E)	low_pass_yuv_filter	0000 0000 0000 0000 0000 0000 dddd dddd	128 (0x00000080)
R13306(R0x000033FA)	nr_blue_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020
R13304(R0x000033F8)	nr_green_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020)
R13308(R0x000033FC)	nr_mm_th	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13302(R0x000033F6)	nr_red_th	0000 0000 0000 0000 0000 0000 dddd dddd	32 (0x00000020)
R13102(R0x0000332E)	output_format_configuration	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13104(R0x00003330)	output_format_test	0000 0000 0000 0000 0000 d00d d0dd dddd	0 (0x00000000
R12958(R0x0000329E)	preview_hunting_gain_enable	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R13012(R0x000032D4)	red_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R12922(R0x0000327A)	red_offset	0000 0000 0000 0000 0000 000d dddd dddd	168 (0x000000A8
R12986(R0x000032BA)	red_offset_to_ccm	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

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Table 44: 1: SOC1 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13020(R0x000032DC)	second_digital_gain	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13130(R0x0000334A)	sepia_constants	0000 0000 0000 0000 dddd dddd dddd dddd	45091 (0x0000B023)
R13128(R0x00003348)	special_effect_parameters	0000 0000 0000 0000 dddd dddd 0ddd dddd	25664 (0x00006440)
R12916(R0x00003274)	threshold_for_y_filter_b_channel	0000 0000 0000 0000 0000 0000 0ddd dddd	42 (0x0000002A
R12914(R0x00003272)	threshold_for_y_filter_g_channel	0000 0000 0000 0000 0000 dddd dddd dddd	2020 (0x000007E4)
R12912(R0x00003270)	threshold_for_y_filter_r_channel	0000 0000 0000 0000 0000 dddd dddd dddd	1962 (0x000007AA)
R13180(R0x0000337C)	yuv_ycbcr_control	0000 0000 0000 0000 0000 0000 0000 dddd	6 (0x00000006)
R13182(R0x0000337E)	y_rgb_offset	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R12834(R0x00003222)	zoom_window_x0	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000
R12836(R0x00003224)	zoom_window_x1	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R12838(R0x00003226)	zoom_window_y0	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R12840(R0x00003228)	zoom_window_y1	0000 0000 0000 0000 0000 dddd dddd dddd	479 (0x000001DF

Table 45: 2: SOC2 Registers Sorted By Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13704(R0x00003588)	ae_avg_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13706(R0x0000358A)	ae_avg_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13708(R0x0000358C)	ae_avg_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13696(R0x00003580)	ae_zone_height	0000 0000 0000 0000 0000 0ddd dddd dddd	X
R13700(R0x00003584)	ae_zone_size_hi	0000 0000 0000 0000 dddd dddd dddd dddd	X
R13698(R0x00003582)	ae_zone_size_lo	0000 0000 0000 0000 dddd dddd dddd dddd	X
R13694(R0x0000357E)	ae_zone_width	0000 0000 0000 0000 0000 dddd dddd dddd	X
R13686(R0x00003576)	ae_zone_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	X
R13688(R0x00003578)	ae_zone_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	X
R13732(R0x000035A4)	bright_color_kill_controls	0000 0000 0000 0000 0000 0ddd dddd dddd	1428 (0x00000594)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13868(R0x0000362C)	b_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13878(R0x00003636)	b_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13880(R0x00003638)	b_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE)
R13882(R0x0000363A)	b_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13884(R0x0000363C)	b_gamma_curve_knees_16_17	0000 0000 0000 0000 dddd dddd dddd dddd	65019 (0x0000FDFB)
R13870(R0x0000362E)	b_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13872(R0x00003630)	b_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13874(R0x00003632)	b_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13876(R0x00003634)	b_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13886(R0x0000363E)	b_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13786(R0x000035DA)	clip1_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13784(R0x000035D8)	clip1_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13438(R0x0000347E)	clip1_config	0000 0000 0000 0000 0000 0000 0000 0ddd	2 (0x00000002)
R13740(R0x000035AC)	clip1_max	0000 0000 0000 0000 0000 dddd dddd dddd	4095 (0x00000FFF)
R13738(R0x000035AA)	clip1_min	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13800(R0x000035E8)	clip1_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F
R13796(R0x000035E4)	clip1_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13802(R0x000035EA)	clip1_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13798(R0x000035E6)	clip1_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13794(R0x000035E2)	clip2_cnt_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13792(R0x000035E0)	clip2_cnt_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13440(R0x00003480)	clip2_config	0000 0000 0000 0000 0000 0000 0000 00dd	2 (0x00000002)
R13744(R0x000035B0)	clip2_max	0000 0000 0000 0000 0000 dddd dddd dddd	4095 (0x00000FFF)
R13742(R0x000035AE)	clip2_min	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13746(R0x000035B2)	clip2_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13772(R0x000035CC)	clip2_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13736(R0x000035A8)	clip2_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13774(R0x000035CE)	clip2_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13730(R0x000035A2)	dark_color_kill_controls	0000 0000 0000 0000 0000 0000 dddd dddd	20 (0x00000014)
R13632(R0x00003540)	enable_tonal_curve	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R13848(R0x00003618)	g_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13858(R0x00003622)	g_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13860(R0x00003624)	g_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE
R13862(R0x00003626)	g_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13864(R0x00003628)	g_gamma_curve_knees_16_17x	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13850(R0x0000361A)	g_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13852(R0x0000361C)	g_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13854(R0x0000361E)	g_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13856(R0x00003620)	g_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13866(R0x0000362A)	g_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13722(R0x0000359A)	hist0_bin_config	0000 0000 0000 0000 0000 0000 ddd0 dddd	13 (0x0000000D)
R13728(R0x000035A0)	hist0_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13748(R0x000035B4)	hist0_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13750(R0x000035B6)	hist0_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13752(R0x000035B8)	hist0_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13754(R0x000035BA)	hist0_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13716(R0x00003594)	hist0_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)
R13724(R0x0000359C)	hist1a_bin_config	0000 0000 0000 0000 0000 0000 000d dddd	10 (0x0000000A)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13714(R0x00003592)	hist1a_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13756(R0x000035BC)	hist1a_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13758(R0x000035BE)	hist1a_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13760(R0x000035C0)	hist1a_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13762(R0x000035C2)	hist1a_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13718(R0x00003596)	hist1a_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)
R13726(R0x0000359E)	hist1b_bin_config	0000 0000 0000 0000 0000 0000 000d dddd	8 (0x00000008)
R13712(R0x00003590)	hist1b_bin_offset	0000 0000 0000 0000 0000 dddd dddd dddd	10 (0x0000000A)
R13764(R0x000035C4)	hist1b_bin_stats1	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13766(R0x000035C6)	hist1b_bin_stats2	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13768(R0x000035C8)	hist1b_bin_stats3	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13770(R0x000035CA)	hist1b_bin_stats4	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R13720(R0x00003598)	hist1b_pre_divider	0000 0000 0000 0000 dddd dddd dddd dddd	778 (0x0000030A)
R13780(R0x000035D4)	hist_win_x_end	0000 0000 0000 0000 0000 dddd dddd dddd	639 (0x0000027F)
R13776(R0x000035D0)	hist_win_x_start	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R13782(R0x000035D6)	hist_win_y_end	0000 0000 0000 0000 0000 0ddd dddd dddd	479 (0x000001DF)
R13778(R0x000035D2)	hist_win_y_start	0000 0000 0000 0000 0000 0ddd dddd dddd	0 (0x00000000)
R13908(R0x00003654)	p_b_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13910(R0x00003656)	p_b_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13912(R0x00003658)	p_b_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13914(R0x0000365A)	p_b_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13916(R0x0000365C)	p_b_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13972(R0x00003694)	p_b_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13974(R0x00003696)	p_b_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13976(R0x00003698)	p_b_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13978(R0x0000369A)	p_b_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13980(R0x0000369C)	p_b_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14036(R0x000036D4)	p_b_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14038(R0x000036D6)	p_b_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14040(R0x000036D8)	p_b_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14042(R0x000036DA)	p_b_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14044(R0x000036DC)	p_b_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14100(R0x00003714)	p_b_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14102(R0x00003716)	p_b_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14104(R0x00003718)	p_b_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14106(R0x0000371A)	p_b_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14108(R0x0000371C)	p_b_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14164(R0x00003754)	p_b_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14166(R0x00003756)	p_b_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14168(R0x00003758)	p_b_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14170(R0x0000375A)	p_b_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14172(R0x0000375C)	p_b_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13888(R0x00003640)	p_g1_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13890(R0x00003642)	p_g1_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13892(R0x00003644)	p_g1_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13894(R0x00003646)	p_g1_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13896(R0x00003648)	p_g1_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13952(R0x00003680)	p_g1_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13954(R0x00003682)	p_g1_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13956(R0x00003684)	p_g1_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13958(R0x00003686)	p_g1_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13960(R0x00003688)	p_g1_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14016(R0x000036C0)	p_g1_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14018(R0x000036C2)	p_g1_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14020(R0x000036C4)	p_g1_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14022(R0x000036C6)	p_g1_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14024(R0x000036C8)	p_g1_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14080(R0x00003700)	p_g1_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14082(R0x00003702)	p_g1_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14084(R0x00003704)	p_g1_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14086(R0x00003706)	p_g1_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14088(R0x00003708)	p_g1_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14144(R0x00003740)	p_g1_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14146(R0x00003742)	p_g1_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14148(R0x00003744)	p_g1_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14150(R0x00003746)	p_g1_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14152(R0x00003748)	p_g1_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13918(R0x0000365E)	p_g2_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13920(R0x00003660)	p_g2_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13922(R0x00003662)	p_g2_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13924(R0x00003664)	p_g2_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13926(R0x00003666)	p_g2_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13982(R0x0000369E)	p_g2_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13984(R0x000036A0)	p_g2_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13986(R0x000036A2)	p_g2_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13988(R0x000036A4)	p_g2_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13990(R0x000036A6)	p_g2_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14046(R0x000036DE)	p_g2_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14048(R0x000036E0)	p_g2_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14050(R0x000036E2)	p_g2_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14052(R0x000036E4)	p_g2_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14054(R0x000036E6)	p_g2_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14110(R0x0000371E)	p_g2_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14112(R0x00003720)	p_g2_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14114(R0x00003722)	p_g2_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd0	(0x00000000)
R14116(R0x00003724)	p_g2_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14118(R0x00003726)	p_g2_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14174(R0x0000375E)	p_g2_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14176(R0x00003760)	p_g2_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14178(R0x00003762)	p_g2_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14180(R0x00003764)	p_g2_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14182(R0x00003766)	p_g2_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13898(R0x0000364A)	p_r_p0q0	0000 0000 0000 0000 dddd dddd dddd dddd	16 (0x00000010)
R13900(R0x0000364C)	p_r_p0q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13902(R0x0000364E)	p_r_p0q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13904(R0x00003650)	p_r_p0q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13906(R0x00003652)	p_r_p0q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13962(R0x0000368A)	p_r_p1q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13964(R0x0000368C)	p_r_p1q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13966(R0x0000368E)	p_r_p1q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13968(R0x00003690)	p_r_p1q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13970(R0x00003692)	p_r_p1q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14026(R0x000036CA)	p_r_p2q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14028(R0x000036CC)	p_r_p2q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14030(R0x000036CE)	p_r_p2q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14032(R0x000036D0)	p_r_p2q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14034(R0x000036D2)	p_r_p2q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14090(R0x0000370A)	p_r_p3q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14092(R0x0000370C)	p_r_p3q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14094(R0x0000370E)	p_r_p3q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14096(R0x00003710)	p_r_p3q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14098(R0x00003712)	p_r_p3q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14154(R0x0000374A)	p_r_p4q0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14156(R0x0000374C)	p_r_p4q1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14158(R0x0000374E)	p_r_p4q2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14160(R0x00003750)	p_r_p4q3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R14162(R0x00003752)	p_r_p4q4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R13678(R0x0000356E)	reciprocal_of_400_minus_x6	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13664(R0x00003560)	reciprocal_of_x0_minus_zero	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13666(R0x00003562)	reciprocal_of_x1_minus_x0	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13668(R0x00003564)	reciprocal_of_x2_minus_x1	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13670(R0x00003566)	reciprocal_of_x3_minus_x2	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13672(R0x00003568)	reciprocal_of_x4_minus_x3	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13674(R0x0000356A)	reciprocal_of_x5_minus_x4	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13676(R0x0000356C)	reciprocal_of_x6_minus_x5	0000 0000 0000 0000 0000 00dd dddd dddd	8 (0x00000008)
R13828(R0x00003604)	r_gamma_curve_knees_0_1	0000 0000 0000 0000 dddd dddd dddd dddd	6912 (0x00001B00)
R13838(R0x0000360E)	r_gamma_curve_knees_10_11	0000 0000 0000 0000 dddd dddd dddd dddd	59617 (0x0000E8E1)
R13840(R0x00003610)	r_gamma_curve_knees_12_13	0000 0000 0000 0000 dddd dddd dddd dddd	62190 (0x0000F2EE)
R13842(R0x00003612)	r_gamma_curve_knees_14_15	0000 0000 0000 0000 dddd dddd dddd dddd	63990 (0x0000F9F6)
R13844(R0x00003614)	r_gamma_curve_knees_16_17	0000 0000 0000 0000 dddd dddd dddd dddd	65019 (0x0000FDFB)
R13830(R0x00003606)	r_gamma_curve_knees_2_3	0000 0000 0000 0000 dddd dddd dddd dddd	19502 (0x00004C2E)
R13832(R0x00003608)	r_gamma_curve_knees_4_5	0000 0000 0000 0000 dddd dddd dddd dddd	39032 (0x00009878)
R13834(R0x0000360A)	r_gamma_curve_knees_6_7	0000 0000 0000 0000 dddd dddd dddd dddd	49584 (0x0000C1B0)
R13836(R0x0000360C)	r_gamma_curve_knees_8_9	0000 0000 0000 0000 dddd dddd dddd dddd	55759 (0x0000D9CF)
R13846(R0x00003616)	r_gamma_curve_knee_18	0000 0000 0000 0000 0000 0000 dddd dddd	255 (0x000000FF)
R13634(R0x00003542)	tonal_x0	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13636(R0x00003544)	tonal_x1	0000 0000 0000 0000 0000 00dd dddd dddd	256 (0x00000100)
R13638(R0x00003546)	tonal_x2	0000 0000 0000 0000 0000 00dd dddd dddd	384 (0x00000180)
R13640(R0x00003548)	tonal_x3	0000 0000 0000 0000 0000 00dd dddd dddd	512 (0x00000200)
R13642(R0x0000354A)	tonal_x4	0000 0000 0000 0000 0000 00dd dddd dddd	640 (0x00000280)
R13644(R0x0000354C)	tonal_x5	0000 0000 0000 0000 0000 00dd dddd dddd	768 (0x00000300)
R13646(R0x0000354E)	tonal_x6	0000 0000 0000 0000 0000 00dd dddd dddd	896 (0x00000380)
R13648(R0x00003550)	tonal_y0	0000 0000 0000 0000 0000 00dd dddd dddd	128 (0x00000080)
R13650(R0x00003552)	tonal_y1	0000 0000 0000 0000 0000 00dd dddd dddd	256 (0x00000100)

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Table 45: 2: SOC2 Registers Sorted By Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13652(R0x00003554)	tonal_y2	0000 0000 0000 0000 0000 00dd dddd dddd	384 (0x00000180)
R13654(R0x00003556)	tonal_y3	0000 0000 0000 0000 0000 00dd dddd dddd	512 (0x00000200)
R13656(R0x00003558)	tonal_y4	0000 0000 0000 0000 0000 00dd dddd dddd	640 (0x00000280)
R13658(R0x0000355A)	tonal_y5	0000 0000 0000 0000 0000 00dd dddd dddd	768 (0x00000300)
R13660(R0x0000355C)	tonal_y6	0000 0000 0000 0000 0000 00dd dddd dddd	896 (0x00000380)

Table 46: SYSCTL Registers Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R96(R0x00000060)	bist_control	0000 0000 0000 0000 0000 0000 0000 000d	0 (0x00000000)
R102(R0x00000066)	bist_debug	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R108(R0x0000006C)	bist_fail	0000 0000 0000 0000 000? ???? ???? ????	0 (0x00000000)
R104(R0x00000068)	bist_hold	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R110(R0x0000006E)	bist_start_retention	0000 0000 0000 0000 0000 ???? ???? ????	0 (0x00000000)
R98(R0x00000062)	bist_test	0000 0000 0000 0000 000d dddd dddd dddd	0 (0x00000000)
R106(R0x0000006A)	bist_test_done	0000 0000 0000 0000 000? ???? ???? ????	0 (0x00000000)
R100(R0x00000064)	bist_test_resume	0000 0000 0000 0000 0000 dddd dddd dddd	0 (0x00000000)
R22(R0x00000016)	clocks_control	0000 0000 0000 0000 0ddd dddd 0ddd dddd	6783 (0x00001A7F)
R64(R0x00000040)	command_register	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R6(R0x00000006)	i2c_controx	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R38(R0x00000026)	initialize_sensor	0000 0000 0000 0000 0000 0000 0000 00dd	1 (0x00000001)
R0(R0x00000000)	k22b_chip_idx	0000 0000 0000 0000 0000 0000 0000 00dd	1 (0x00000001)
R80(R0x00000050)	k22b_rtl_ver	0000 0000 0000 0000 ???? ???? ???? ????	2 (0x00000002)
R28(R0x0000001C)	mcu_boot_mode	0000 0000 0000 0000 dddd dddd dddd dddd	1 (0x00000001)
R50(R0x00000032)	pad_control	0000 0000 0000 0000 dddd 00d0 dd0d 000d	209 (0x000000D1)
R52(R0x00000034)	pad_gpi_status	0000 0000 0000 0000 ???? 000? ???? ????	0 (0x00000000)

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Table 46: SYSCTL Registers Sorted by Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R48(R0x00000030)	pad_slew	0000 0000 0000 0000 0ddd 0ddd 0ddd 0ddd	1024 (0x00000400)
R20(R0x00000014)	pll_control	0000 0000 0000 0000 dd0d dddd dddd dddd	22596 (0x00005844)
R16(R0x00000010)	pll_dividers	0000 0000 0000 0000 00dd dddd dddd dddd	530 (0x00000212
R18(R0x00000012)	pll_p_dividers	0000 0000 0000 0000 00dd dddd dddd dddd	0 (0x00000000)
R26(R0x0000001A)	reset_and_misc_control	0000 0000 0000 0000 dddd 0000 0000 000d	0 (0x00000000)
R24(R0x00000018)	standby_control_and_status	0000 0000 0000 0000 0d00 0000 0ddd d00d	16425 (0x00004029)

Table 47: RX_SS Registers Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R272(R0x00000110)	col_end	0000 0000 0000 0000 0000 dddd dddd dddd	757 (0x000002F5)
R268(R0x0000010C)	col_start	0000 0000 0000 0000 0000 dddd dddd dddd	109 (0x0000006D)
R270(R0x0000010E)	row_end	0000 0000 0000 0000 0000 0ddd dddd dddd	510 (0x000001FE)
R266(R0x0000010A)	row_start	0000 0000 0000 0000 0000 0ddd dddd dddd	22 (0x00000016)
R256(R0x00000100)	testp_ctl	0000 0000 0000 0000 0000 0ddd ddd0 0ddd	0 (0x00000000)
R276(R0x00000114)	testp_x	0000 0000 0000 0000 000d dddd dddd dddd	857 (0x00000359)
R278(R0x00000116)	testp_y	0000 0000 0000 0000 000d dddd dddd dddd	524 (0x0000020C)
R264(R0x00000108)	test_pxl_blue	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R260(R0x00000104)	test_pxl_g1	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R262(R0x00000106)	test_pxl_g2	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)
R258(R0x00000102)	test_pxl_red	0000 0000 0000 0000 0000 dddd dddd dddd	511 (0x000001FF)

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Table 48: XDMA Registers Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R2434(R0x00000982)	access_ctl_stat	0000 0000 0000 0000 0000 0000 dd0d dddd	0 (0x00000000)
R2446(R0x0000098E)	logical_address_access	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2448(R0x00000990)	mcu_variable_data0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2450(R0x00000992)	mcu_variable_data1	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2452(R0x00000994)	mcu_variable_data2	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2454(R0x00000996)	mcu_variable_data3	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2456(R0x00000998)	mcu_variable_data4	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2458(R0x0000099A)	mcu_variable_data5	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2460(R0x0000099C)	mcu_variable_data6	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2462(R0x0000099E)	mcu_variable_data7	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R2442(R0x0000098A)	physical_address_access	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)

Table 49: TX_SS Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R15372(R0x00003C0C)	checksum_ctrl	0000 0000 0000 0000 0000 0000 0000 000d	1 (0x00000001)
R15374(R0x00003C0E)	checksum_data	0000 0000 0000 0000 ???? ???? ???? ????	65535 (0x0000FFFF)
R15362(R0x00003C02)	gpo	0000 0000 0000 0000 dddd 000d dddd dddd	0 (0x00000000)
R15360(R0x00003C00)	parallel_bus_ctrl	0000 0000 0000 0000 000d 000d 000d 0ddd	4096 (0x00001000)
R15368(R0x00003C08)	tvenc_ctrl_1	0000 0000 0000 0000 00dd 000d 000d 000d	8193 (0x00002001)
R15370(R0x00003C0A)	tvenc_ctrl_2	0000 0000 0000 0000 00dd 00dd 00dd 00dd	0 (0x00000000)
R15364(R0x00003C04)	vdac_cal_1	0000 0000 0000 0000 00dd dddd dd0d dddd	8400 (0x000020D0)
R15366(R0x00003C06)	vdac_cal_2	0000 0000 0000 0000 0000 0000 0000 dddd	0 (0x00000000)
R15376(R0x00003C10)	vdac_test	0000 0000 0000 0000 00dd 00dd dddd dddd	0 (0x00000000)

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Table 50: OVERLAY_SS Registers Sorted by Name

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20240(R0x00004F10)	overlay_calibration	0000 0000 0000 0000 00dd dddd 00dd dddd	8224 (0x00002020)
R20272(R0x00004F30)	overlay_char_backcolour0	0000 0000 0000 0000 dddd dd00 dddd d000	0 (0x00000000)
R20274(R0x00004F32)	overlay_char_backcolour1	0000 0000 0000 0000 dddd d000 dddd 0000	0 (0x00000000)
R20276(R0x00004F34)	overlay_char_colour0	0000 0000 0000 0000 dddd dd00 dddd d000	0 (0x00000000)
R20278(R0x00004F36)	overlay_char_colour1	0000 0000 0000 0000 dddd d000 dddd 0000	0 (0x00000000)
R20246(R0x00004F16)	overlay_char_control0	0000 0000 0000 0000 dddd dddd dddd dddd	0 (0x00000000)
R20248(R0x00004F18)	overlay_char_control1	0000 0000 0000 0000 d000 0000 00dd dddd	0 (0x00000000)
R20250(R0x00004F1A)	overlay_char_descriptor0_1	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20260(R0x00004F24)	overlay_char_descriptor10_11	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20262(R0x00004F26)	overlay_char_descriptor12_13	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20264(R0x00004F28)	overlay_char_descriptor14_15	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20266(R0x00004F2A)	overlay_char_descriptor16_17	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20268(R0x00004F2C)	overlay_char_descriptor18_19	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20270(R0x00004F2E)	overlay_char_descriptor20_21	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20252(R0x00004F1C)	overlay_char_descriptor2_3	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20254(R0x00004F1E)	overlay_char_descriptor4_5	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20256(R0x00004F20)	overlay_char_descriptor6_7	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20258(R0x00004F22)	overlay_char_descriptor8_9	0000 0000 0000 0000 0000 dddd 0000 dddd	0 (0x00000000)
R20280(R0x00004F38)	overlay_char_x_offset	0000 0000 0000 0000 0000 000d dddd dddd	0 (0x00000000)
R20282(R0x00004F3A)	overlay_char_y_offset	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R20226(R0x00004F02)	overlay_control	0000 0000 0000 0000 d000 0000 0000 000d	0 (0x00000000)
R20228(R0x00004F04)	overlay_interrupt_control	0000 0000 0000 0000 0000 0000 0000 0ddd	0 (0x00000000)
R20230(R0x00004F06)	overlay_interrupt_mask	0000 0000 0000 0000 0000 0000 0000 0ddd	7 (0x00000007)
R20232(R0x00004F08)	overlay_layer0_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)

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Table 50: OVERLAY_SS Registers Sorted by Name (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20234(R0x00004F0A)	overlay_layer1_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20236(R0x00004F0C)	overlay_layer2_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20238(R0x00004F0E)	overlay_layer3_control	0000 0000 0000 0000 d000 0000 0000 0ddd	0 (0x00000000)
R20224(R0x00004F00)	overlay_status	0000 0000 0000 0000 ??00 0000 00?? ????	49152 (0x0000C000)
R20242(R0x00004F12)	overlay_testmode	0000 0000 0000 0000 0000 0000 0000 dddd	0 (0x00000000)

Table 51: CALIB_STATS_SS Registers

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R19714(R0x00004D02)	calib_stats_acc0_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19712(R0x00004D00)	calib_stats_acc0_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19718(R0x00004D06)	calib_stats_acc1_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19716(R0x00004D04)	calib_stats_acc1_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19722(R0x00004D0A)	calib_stats_acc2_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19720(R0x00004D08)	calib_stats_acc2_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19726(R0x00004D0E)	calib_stats_acc3_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19724(R0x00004D0C)	calib_stats_acc3_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19730(R0x00004D12)	calib_stats_acc4_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19728(R0x00004D10)	calib_stats_acc4_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19734(R0x00004D16)	calib_stats_acc5_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19732(R0x00004D14)	calib_stats_acc5_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19738(R0x00004D1A)	calib_stats_acc6_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19736(R0x00004D18)	calib_stats_acc6_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19742(R0x00004D1E)	calib_stats_acc7_hi	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19740(R0x00004D1C)	calib_stats_acc7_lo	0000 0000 0000 0000 ???? ???? ???? ????	0 (0x00000000)
R19752(R0x00004D28)	calib_stats_ctrl	0000 0000 0000 0000 0000 0000 0000 0ddd	0 (0x00000000)

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Table 51: CALIB_STATS_SS Registers (continued)

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R19746(R0x00004D22)	calib_stats_x_addr_end	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19744(R0x00004D20)	calib_stats_x_addr_start	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19750(R0x00004D26)	calib_stats_y_addr_end	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)
R19748(R0x00004D24)	calib_stats_y_addr_start	0000 0000 0000 0000 0000 00dd dddd dddd	0 (0x00000000)

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Modes and Timing

This section provides an overview of the typical usage modes and related timing information for the MT9V136.

Composite Video Output

The analog composite video output is enabled by default and is the main usage mode for the MT9V136.

The external pin DOUT_LSB) can be used to configure the device for default NTSC or PAL operation. This and other video configuration settings are available as register settings accessible through the serial interface.

NTSC

Both differential and single-ended connections of the full NTSC format are supported. The differential connection that uses two output lines is used for low noise or long distance applications. The single-ended connection is used for PCB tracks and screened cable where noise is not a concern. The NTSC format has three black lines at the bottom of each image for padding (which most LCDs do not display).

PAL

The PAL format is supported with 576 active image rows.

NTSC or PAL with External Image Processing

The on-chip video encoder and DAC can be used with external data stream input (DIN[7:0] port). Correct NTSC or PAL formatted CCIR656 data is required for correct composite video output.

The on-chip overlay may be put on top of the overlay generated by the external overlay generator.

Single-Ended and Differential Composite Output

The composite output can be operated in a single-ended or differential mode by simply changing the external resistor configuration. For single-ended termination, see Figure 34 on page 98.

For differential mode termination, there are two alternatives. The differential schematic is shown in Figure 34 on page 98. The second differential schematic with floating terminations is shown in Figure 35 on page 98.

Note: The differential schematics have not been tested.

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Figure 34: Single-Ended Termination

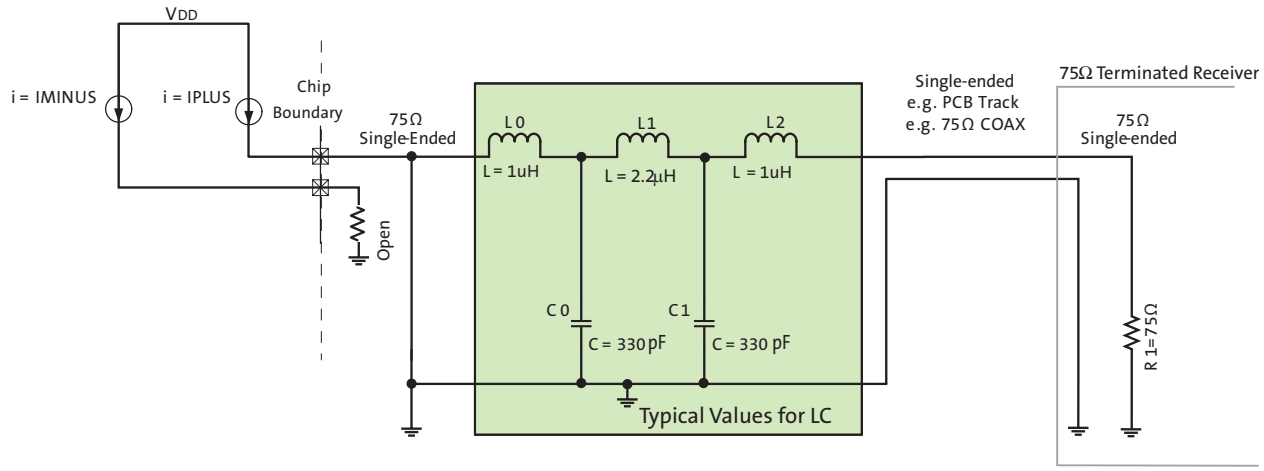
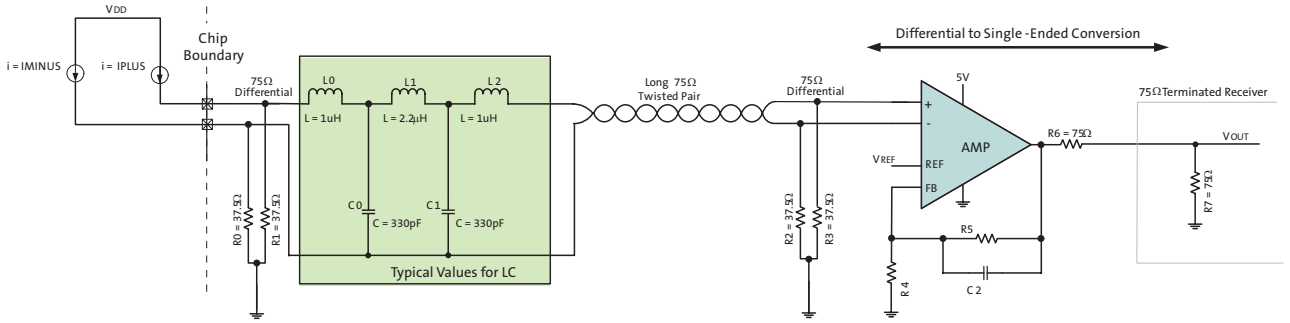


Figure 35: Differential Connection—Grounded Terminations



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Parallel Output (DOUT)

Progressive

The DOUT[7:0] port supports progressive, raw data output. The raw pixel data can also be made available in sensor stand-alone mode.

Figure 36 shows the data that is output on the parallel port for CCIR656. Both NTSC and PAL formats are displayed. The blue values in Figure 36 represent NTSC (525/60). The red values represent PAL (625/50).

Figure 36: CCIR656 8-Bit Parallel Interface Format for 525/60 (625/50) Video Systems

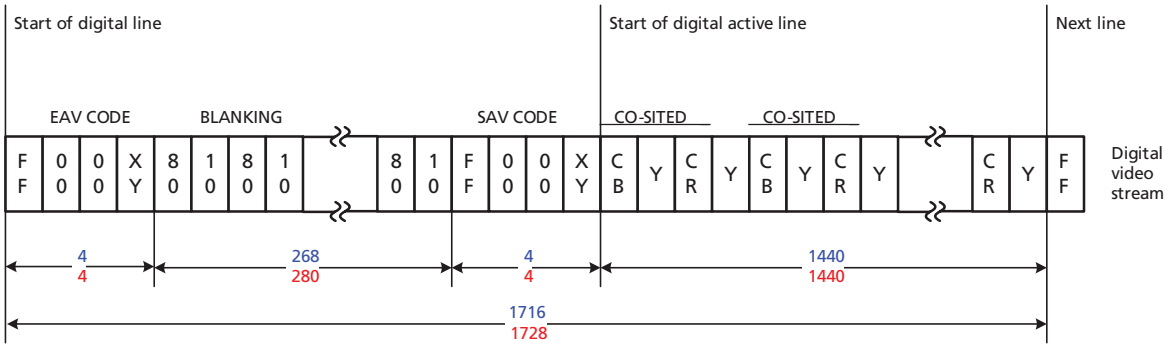

Figure 37 shows detailed vertical blanking information for NTSC timing. See Table 52 on page 100 for data on field, vertical blanking, EAV, and SAV states.

Figure 37: Typical CCIR656 Vertical Blanking Intervals for 525/60 Video System

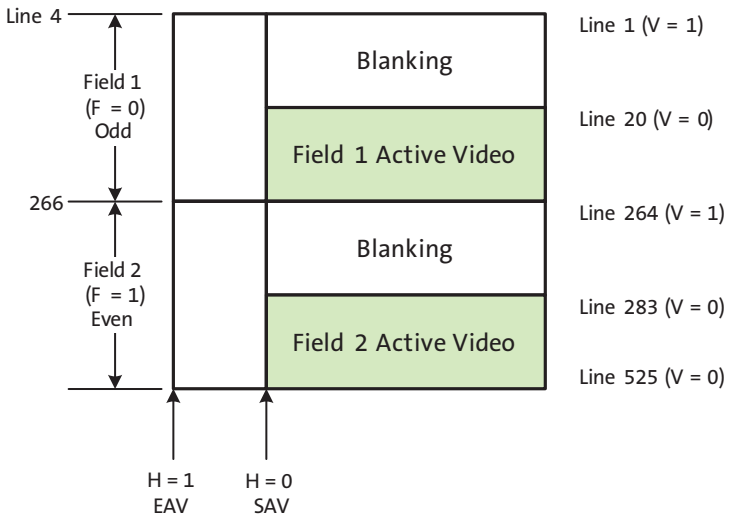

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Table 52: Field, Vertical Blanking, EAV, and SAV States

Line Number	F	V	H (EAV)	H (SAV)
1–3	1	1	1	0
4–9	0	1	1	0
20–263	0	0	1	0
264–265	0	1	1	0
266–282	1	1	1	0
283–525	1	0	1	0

Figure 38 shows detailed vertical blanking information for PAL timing. See Table 53 for data on field, vertical blanking, EAV, and SAV states.

Figure 38: Typical CCIR656 Vertical Blanking Intervals for 625/50 Video System

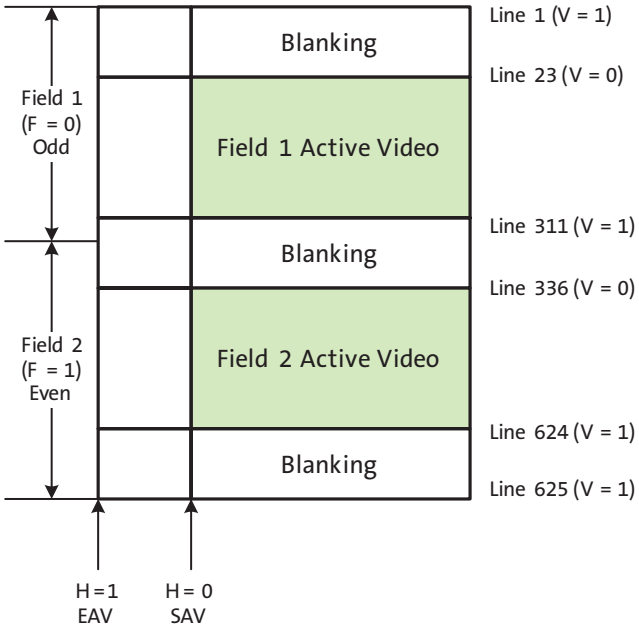

Table 53: Field, Vertical Blanking, EAV, and SAV States

Line Number	F	V	H (EAV)	H (SAV)
1–22	0	1	1	0
23–310	0	0	1	0
311–312	0	1	1	0
313–335	1	1	1	0
336–623	1	0	1	0
624–625	1	1	1	0

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Reset and Clocks

Reset

Power-up reset is asserted or de-asserted with the RESET_N pin, which is active LOW. In the reset state, all control registers are set to default values. See “Device Configuration” on page 32 for more details on Auto, Host, and Flash configurations.

Soft reset is asserted or de-asserted by the two-wire serial interface program. In soft-reset mode, the two-wire serial interface and the register bus are still running. All control registers are reset using default values.

Clocks

The MT9V136 has two primary clocks:

- A master clock coming from the EXTCLK signal.
- A pixel clock (PIXCLK) running at:
  - 2 * EXTCLK when in default mode
  - the same frequency as EXTCLK when in raw Bayer bypass mode

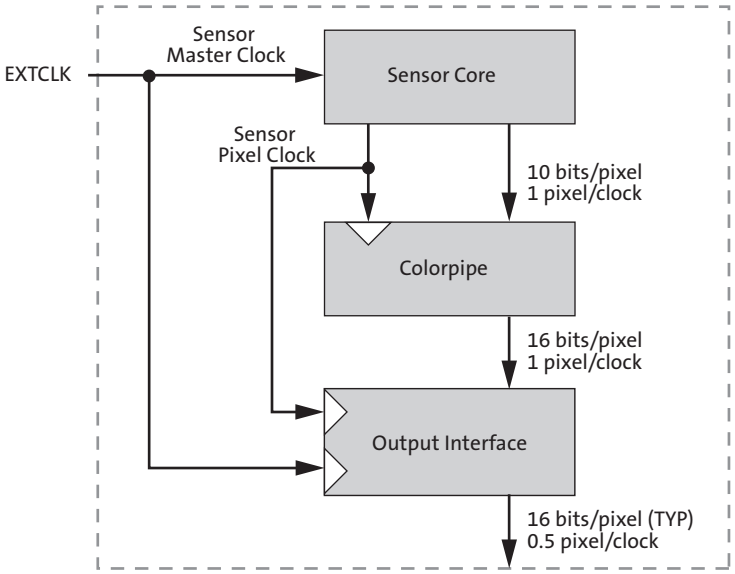
When the MT9V136 operates in sensor stand-alone mode, the image flow pipeline clocks can be shut off to conserve power.

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions. The relationship of the primary clocks is depicted in Figure 39 on page 101.

The image flow pipeline typically generates up to 16 bits per pixel—for example, YCbCr or 565RGB—but has only an 8-bit port through which to communicate this pixel data.

To generate NTSC or PAL format images, the sensor core requires a 27 MHz clock.

Figure 39: Primary Clock Relationships



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Output Data Ordering

Table 54: Output Data Ordering in DOUT RGB Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Note: PIXCLK is 54 MHz when EXTCLK is 27 MHz.

Table 55: Output Data Ordering in Sensor Stand-Alone Mode

Mode	D7	D6	D5	D4	D3	D2	D1	D0	DOUT_LSB1	DOUT_LSB0
10-bit Output	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Note: PIXCLK is 27 MHz when EXTCLK is 27 MHz.

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I/O Circuitry

Figure 40 and Figure 42 on page 105 illustrate typical circuitry used for each input, output or I/O pad.

Figure 40: Typical I/O Equivalent Circuits

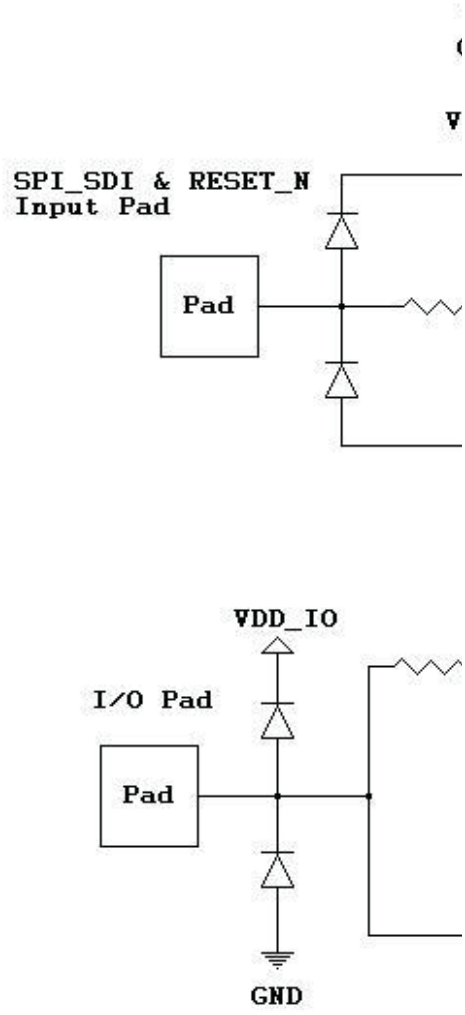

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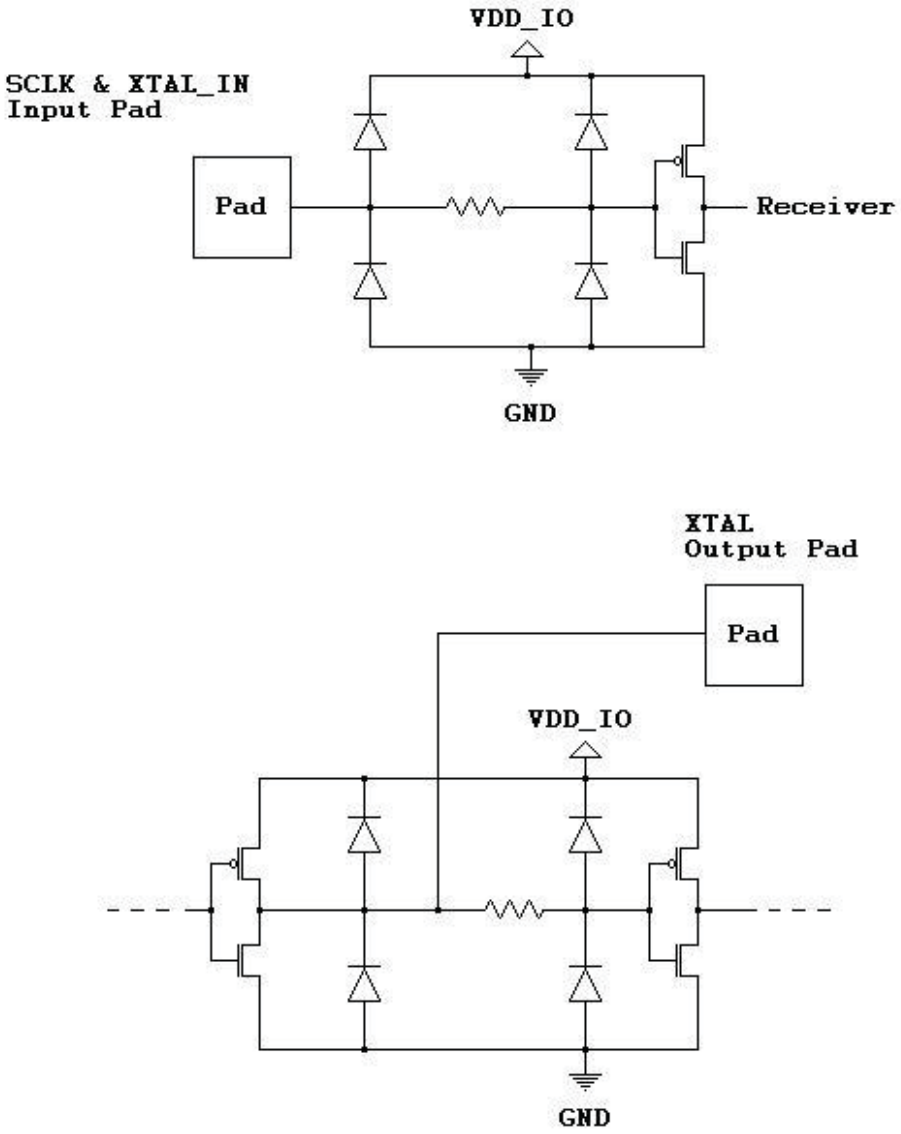
Figure 41: Typical I/O Equivalent Circuits



Note: All I/O circuitry shown above is for reference only. The actual implementation may be different.

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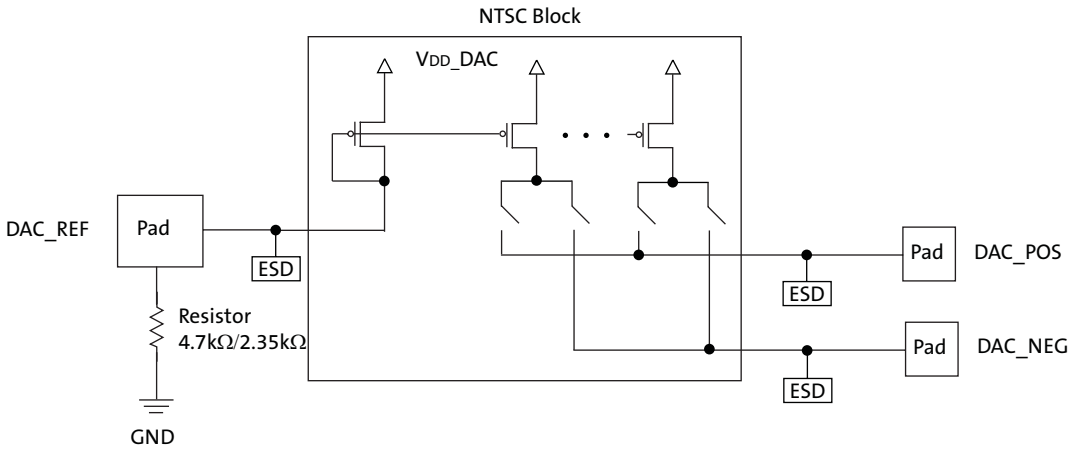
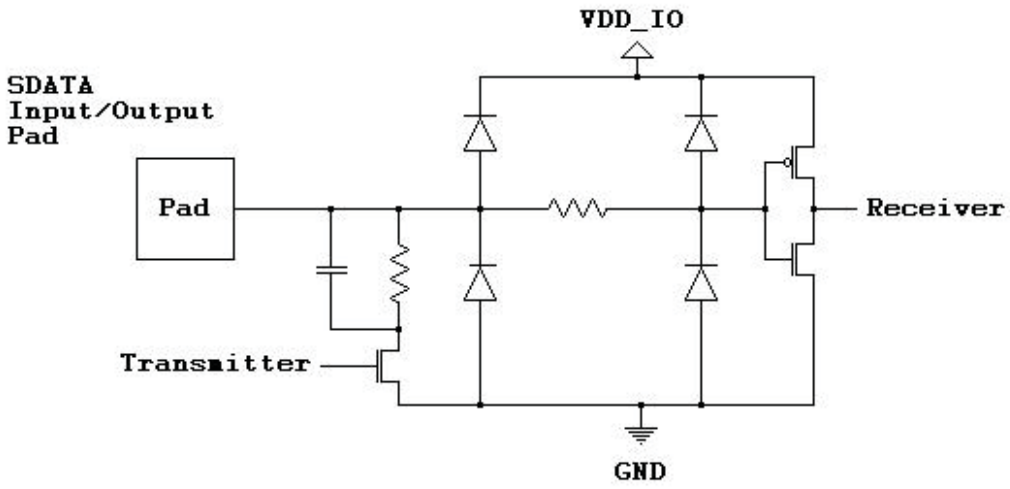
Figure 42: NTSC Block



Note: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 43: Serial Interface



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I/O Timing

Digital Output

By default, the MT9V136 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in Figure 44.

As an option, the polarity of the PIXCLK can be inverted from the default by programming R22[14].

Figure 44: Digital Output I/O Timing

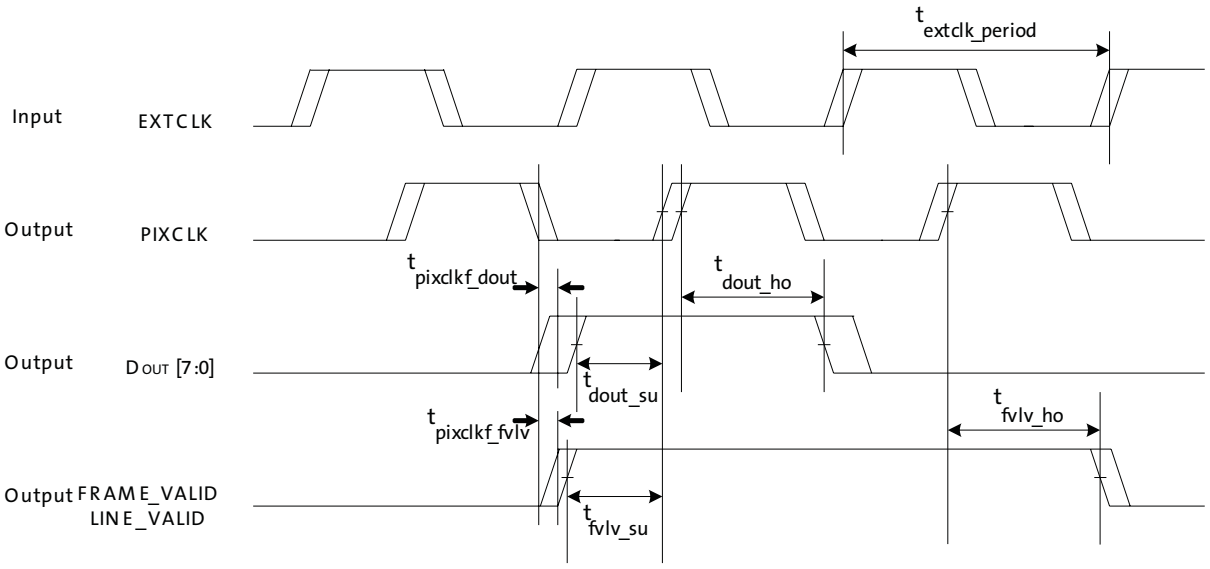

Table 56: Parallel Digital Output I/O Timing

^{f}EXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V; default slew rate

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	^{f}extclk	max +/- 100 ppm	–	27	–	MHz
	^{t}extclk_period		–	27	–	ns
	Duty cycle		45	50	55	%
PIXCLK1	^{f}pixclk		–	27	–	MHz
	^{t}pixclk_period		–	37	–	ns
	Duty cycle		45	50	55	%
DATA[7:0]	^{t}pixclkf_dout		–2	0	2	ns
	^{t}dout_su		8	–	18.5	ns
	^{t}dout_ho		8	–	18.5	ns
FV/LV	^{t}pixclkf_fvlv		–2	0	2	ns
	^{t}fvlv_su		8	–	18.5	ns
	^{t}fvlv_ho		8	–	18.5	ns

Note: PIXCLK can be inverted from the default by programming R22[14].

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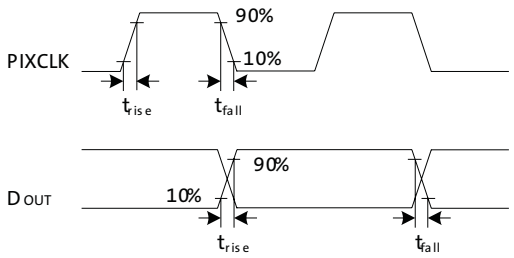
Slew Rate

Table 57: Slew Rate for PIXCLK and DOUT

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V; T = 25°C; C_{LOAD} = 40 pF

PIXCLK			DOUT[7:0]			
R0x30 [10:8]	Typical Rise Time	Typical Fall Time	R0x30 [2:0]	Typical Rise Time	Typical Fall Time	Unit
000	6.5	6.3	000	6.5	6.3	ns
001	4.8	4.6	001	4.8	4.6	ns
010	3.9	3.8	010	3.9	3.8	ns
011	3.7	3.7	011	3.7	3.7	ns
100	3.6	3.6	100	3.6	3.6	ns
101	3.5	3.5	101	3.5	3.5	ns
110	3.4	3.4	110	3.4	3.4	ns
111	3.3	3.3	111	3.3	3.3	ns

Figure 45: Slew Rate Timing



RESET_N Timing

Setup and hold timing for the RESET_N signal with respect to DOUT_LSB[0], LV , and FV are shown in Figure 46 and Table 58. These signals are sampled once by the on chip firmware, which yields a long ^{t}Hold time.

Figure 46: RESET_N Timing

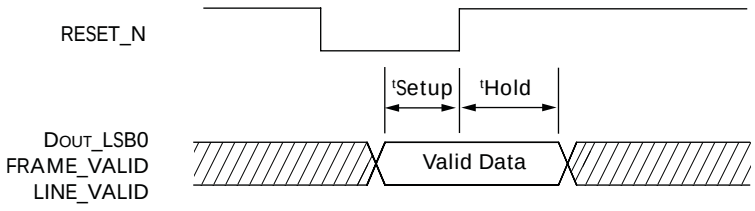


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Table 58: RESET_N Timing

Signal	Parameter	Conditions	Min	Typ	Max	Unit
DOUT_LSB0, FRAME_VALID, LINE_VALID	^{t}Setup		0			µs
	^{t}Hold		50			µs

Figure 47: Power Up Sequence

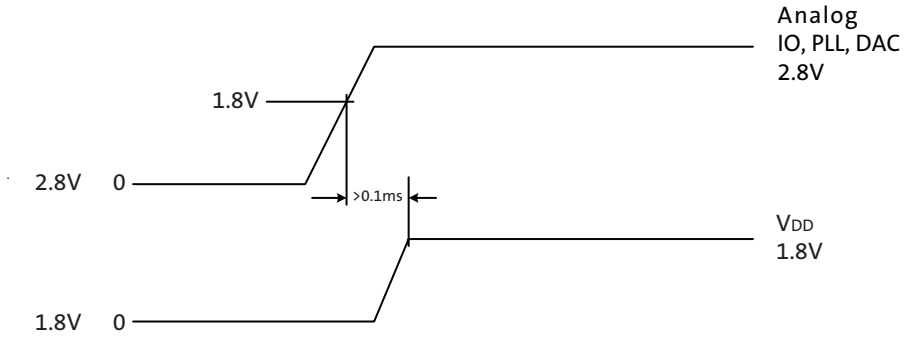

Figure 48: Reset to SPI Access Delay

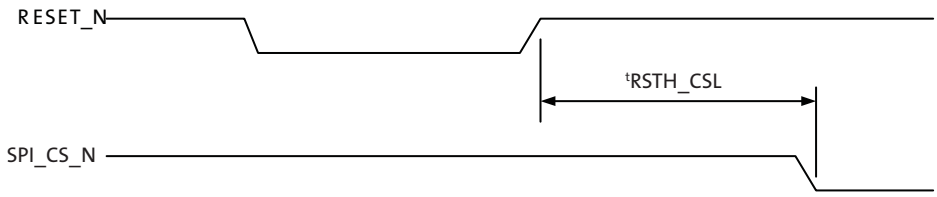

Figure 49: Reset to AE/AWB Image

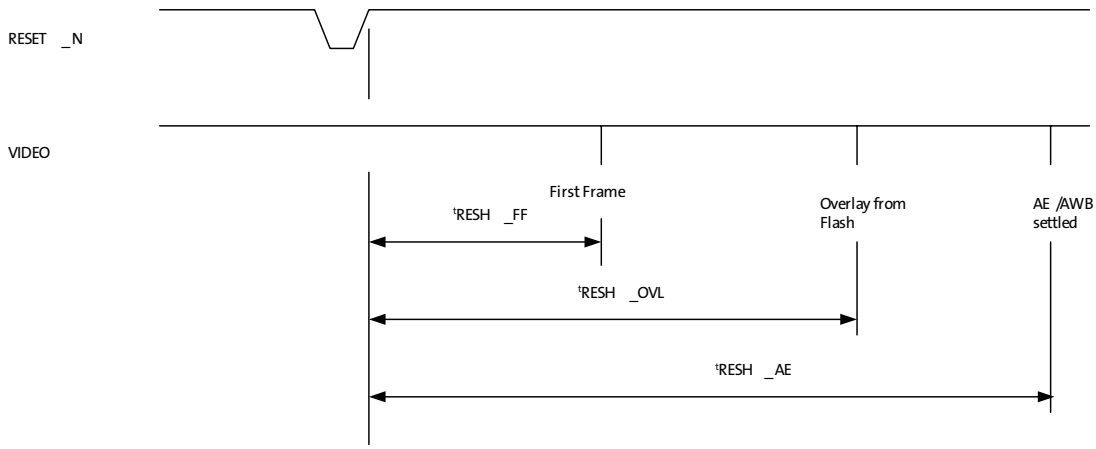

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Table 59: Delay Parameters in NTSC Configuration

Parameter	Name	Condition	Min	Typ	Max	Unit
Power up delay 2.8V to 1.8V			0.1	–	–	ms
RESET_N HIGH to SPI_CS_N LOW	tRSTH_CSL		18	–	–	ms
RESET_N HIGH to SDATA LOW	tRSTH_SDATAL			–	–	ms
RESET_N HIGH to FRAME_VALID	tRSTH_FVH		235	–	–	ms
RESET_N HIGH to first Overlay	tRSTH_OVL		235	–	–	ms
RESET_N HIGH to AE/AWB settled	tRSTH_AEAWB		–	400	–	ms

Electrical Specifications

Signal Specifications

Figure 50: SPI Data Setup and Hold Timing

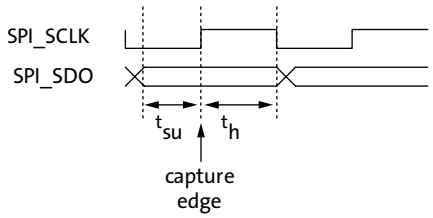

Table 60: SPI Data Setup and Hold Timing

Signal	Conditions	Min	Typ	Max	Units
SPI_SCLK	Frequency	–	4.5	18	MHz
SPI_SDO	Setup time	–	-	110	ns
SPI_SDO	Hold time	–	-	110	ns
SPI_CS_N	Delay from falling edge of SPI_CS_N to rising edge of SPI_SCLK	–	230	–	ns

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Table 61: Electrical Characteristics and Operating Conditions

T_A = Ambient = 25°C

Parameter[1]	Condition	Min	Typ	Max	Unit
Core digital voltage (V_{DD})	–	1.7	1.8	1.9	V
IO digital voltage (V_{DD_IO})	–	2.66	2.8	2.94	V
Video DAC voltage (V_{DD_DAC})	–	2.66	2.8	2.94	V
PLL Voltage (V_{DD_PLL})	–	2.66	2.8	2.94	V
Analog voltage (V_{AA})	–	2.66	2.8	2.94	V
Pixel supply voltage (V_{AA_PIX})	–	2.66	2.8	2.94	V
Leakage current	EXTCLK: HIGH or LOW			10	µA
Imager operating temperature	–	–40		+105	°C
Functional operating temperature[2]		–40		+105	°C
Storage temperature	–	–50		+150	°C

Notes:
1. V_{AA} and V_{AAPIX} must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.
2. Image quality is not guaranteed at temperatures equal to or greater than 85°C.

Table 62: Video DAC Electrical Characteristics–Single-Ended Mode

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V

Parameter	Condition	Min	Typ	Max	Unit
Resolution		–	10	-	bits
DNL		–	0.2	0.4	bits
INL		–	0.7	3.5	bits
Output local load	Output pad (DAC_POS)	–	75	-	Ω
	Unused output (DAC_NEG)	–	0	-	Ω
Output voltage	Single-ended mode, code 000h	–	.02	-	V
	Single-ended mode, code 3FFh	–	1.30	-	V
Output current	Single-ended mode, code 000h	–	0.26	-	mA
	Single-ended mode, code 3FFh	–	17.33	-	mA
Supply current	Estimate	–	-	25.0	mA
DAC_REF	DAC Reference	–	1.15 +/-0.2	-	V
R DAC_REF	DAC Reference	–	4.7	-	KΩ

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Table 63: Video DAC Electrical Characteristics–Differential Mode

[f]EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V

Parameter	Condition	Min	Typ	Max	Unit
DNL		–	0.2	0.25	Bits
INL		–	0.8	2.5	Bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω
Output voltage	Differential mode, code 000h, pad dacp	–	.02	–	V
	Differential mode, code 000h, pad dacn	–	1.30	–	V
	Differential mode, code 3FFh, pad dacp	–	1.30	–	V
	Differential mode, code 3FFH, pad dacn	–	.02	–	V
Output current	Differential mode, code 000h, pad dacp	–	.53	–	mA
	Differential mode, code 000h, pad dacn	–	34.7	–	mA
	Differential mode, code 3FFh, pad dacp	–	34.7	–	mA
	Differential mode, code 3FFH, pad dacn	–	.53	–	mA
Differential output, midlevel		–	0.65	–	V
Supply current	Estimate	–	–	50	mA
DAC_REF	DAC Reference	–	1.15 +/-0.2		V
R DAC_REF	DAC Reference		2.35		KΩ

Table 64: Digital I/O Parameters

T_A = Ambient = 25°C; All supplies at 2.8V

Signal	Parameter	Definitions	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		1	–	30	pF
		Output signal slew	2.8V, 30pF load	–	–	–	V/ns
			2.8V, 5pF load	–	–	–	V/ns
	V_{OH}	Output high voltage		–	V_{DD_IO}	–	V
	V_{OL}	Output low voltage		–0.3	–	–	V
	I_{OH}	Output high current	V_{DD} = 2.8V, V_{OH} = 2.4V	–	–	8	mA
	I_{OL}	Output low current	V_{DD} = 2.8V, V_{OL} = 0.4V	–	–	8	mA
All Inputs	V_{IH}	Input high voltage	V_{DD} = 2.8V	0.7 * V_{DD_IO}	–	V_{DD_IO} + 0.3	V
	V_{IL}	Input low voltage	V_{DD} = 2.8V	–0.3	–	0.3 * V_{DD_IO}	V
	I_{IN}	Input leakage current		–2	–	2	µA
	Signal CAP	Input signal capacitance		–	3.5	–	pF

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Power Consumption, Operating Mode

Table 65: Power Consumption – Condition 1

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD} _IO = 2.8V; V_{AA} =2.8V;V_{AA}_PIX=2.8V; V_{DD} _PLL = 2.8V; V_{DD} _DAC = 2.8V

Power Plane	Supply	Condition 1	Typ Power	Max Power	Unit
V_{DD}	1.8		140.4	162	mW
V_{DD}_IO	2.8	Parallel off	4.2	8.4	mW
V_{AA}	2.8		89.6	112	mW
VAA_PIX	2.8		1.96	5.04	mW
V_{DD}_DAC	2.8	Single 75(1)	39.2	44.8	mW
V_{DD}_PLL	2.8		13.44	16.8	mW
		Total	288.8	349.04	mW

Analog output uses single-ended mode: DAC_Pos = 75Ω, DAC_Neg = open, parallel output is disabled.

Table 66: Power Consumption – Condition 2

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD} _IO = 2.8V; V_{AA} =2.8V;V_{AA}_PIX=2.8V; V_{DD} _PLL = 2.8V; V_{DD} _DAC = 2.8V

Power Plane	Supply	Condition 2	Typ Power	Max Power	Unit
V_{DD}	1.8		140.4	162	mW
V_{DD}_IO	2.8	Parallel on	42	50.4	mW
V_{AA}	2.8		89.6	112	mW
VAA_PIX	2.8		1.96	5.04	mW
V_{DD}_DAC	2.8	Single 75(1)	39.2	44.8	mW
V_{DD}_PLL	2.8		13.44	16.8	mW
		Total	326.6	391.04	mW

Analog output uses single-ended mode: DAC_Pos = 75Ω, DAC_Neg = open, parallel output is enabled.

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NTSC Signal Parameters

Table 67: NTSC Signal Parameters

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD}_IO = 2.8V; V_{AA} = 2.8V; V_{AA}_PIX = 2.8V; V_{DD}_PLL = 2.8V; V_{DD}_DAC = 2.8V

Parameter	Conditions	Min	Typ	Max	Units	Note
Line Frequency		15730	15735	15740	Hz	
Field Frequency		59.00	59.94	60.00	Hz	
Sync Rise Time		120	164	170	ns	
Sync Fall Time		120	167	170	ns	
Sync Width		4.60	4.74	4.80	µS	
Sync Level		37	39.9	43	IRE	2, 4
Burst Level		37	39.7	43	IRE	2, 4

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Table 67: NTSC Signal Parameters

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V

Parameter	Conditions	Min	Typ	Max	Units	Note
Sync to Setup (with pedestal off)		9.10	9.40	9.40	µS	
Sync to Burst Start		5.00	5.31	5.60	µS	
Front Porch		1.40	1.40	1.60	µS	
Burst Width		8.0	8.5	10.0	cycles	
Black Level		6.5	7.5	8.5	IRE	1, 2, 4
White Level		90	100	110	IRE	1, 2, 3, 4

Notes:
1. Black and white levels are referenced to the blanking level.
2. NTSC convention standardized by the IRE (1 IRE = 7.14mV).
3. Encoder contrast setting R0x011 = R0x001 = 0.
4. DAC ref = 2.8kΩ, load = 37.5Ω.

Figure 51: Video Timing

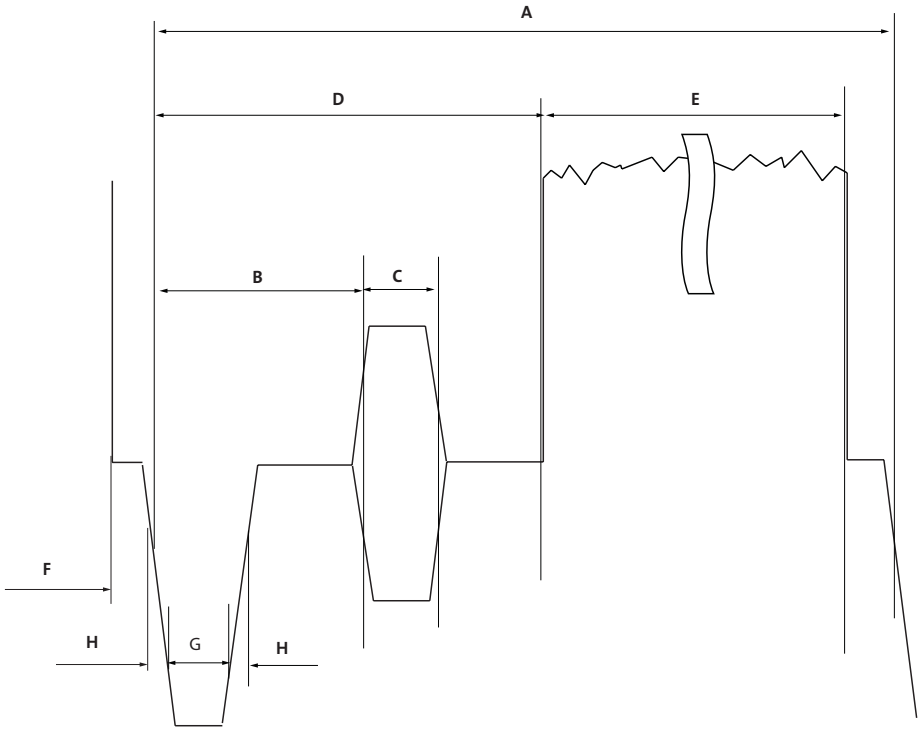

Table 68: Video Timing

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
A	H Period	17161	1728	Clocks
B	Hsync to burst	144	153	Clocks
C	burst	63	66	Clocks
D	Hsync to Signal	255	279	Clocks

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Table 68: Video Timing

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
E	Video Signal	1423	1413	Clocks
F	Front	36	39	Clocks
G	Hsync Period	128	128	Clocks
H	Sync rising/falling edge	4	4	Clocks

Figure 52: Equivalent Pulse

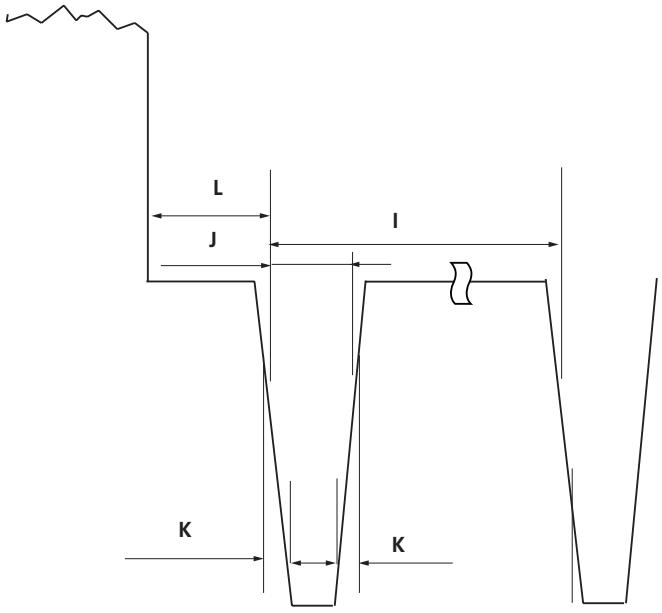

Table 69: Equivalent Pulse

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
I	H/2 Period	858	864	Clocks
J	Pulse width	64	64	Clocks
K	Pulse rising/falling edge	4	4	Clocks
L	Signal to pulse	38	41	Clocks

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Figure 53: V Pulse

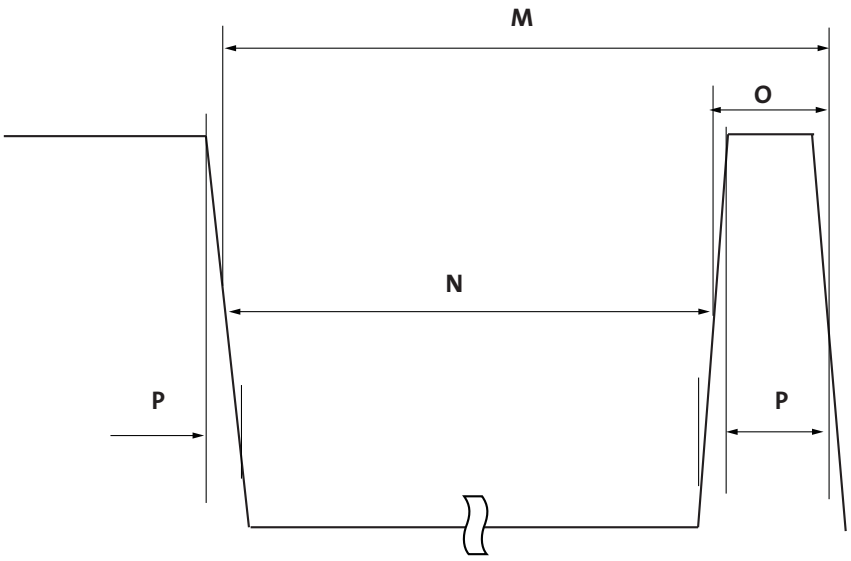

Table 70: V Pulse

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
M	H/2 Period	858	864	Clocks
N	Pulse width	730	736	Clocks
O	V pulse interval	128	128	Clocks
P	Pulse rising/falling edge	4	4	Clocks

Two-Wire Serial Bus Timing

Figure 54 and Table 71 on page 117 describe the timing for the two-wire serial interface.

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Figure 54: Two-Wire Serial Bus Timing Parameters

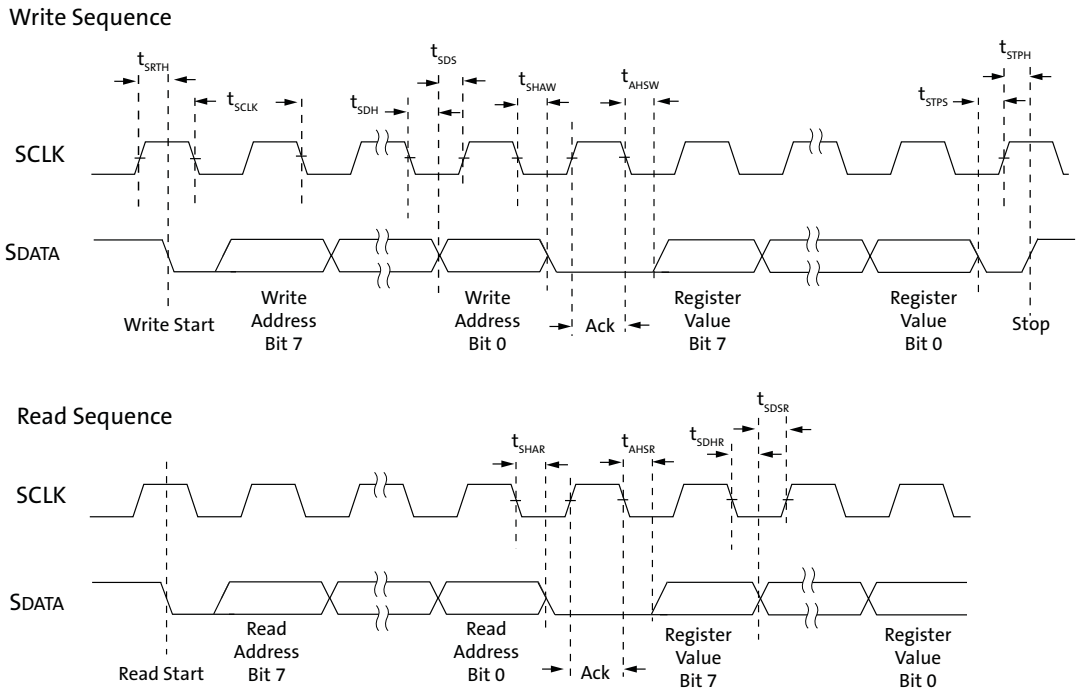

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Table 71: Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
^{f}SCLK	Serial interface input clock frequency		100	–	400	kHz	
^{t}SCLK	Serial interface input clock period		2.5	–	10	µs	Master clock cycle units or PLL cycles if enabled
	SCLK duty cycle		40	50	60	%	
^{t}SRTH	Start hold time	Write/Read	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}SDH	SDATA hold	Write	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}SDS	SDATA setup	Write	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}SHAW	SDATA hold to ack	Write	0.15	–	0.75	µs	Master clock cycle units or PLL cycles if enabled
^{t}AHSW	Ack hold to SDATA	Write	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}STPS	Stop setup time	Write/Read	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}STPH	Stop hold time	Write/Read	0.6	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}SHAR	SDATA hold to ack	Read	0.15	–	0.75	µs	Master clock cycle units or PLL cycles if enabled
^{t}AHSR	Ack hold to SDATA	Read	0.15	–	1	µs	Master clock cycle units or PLL cycles if enabled
^{t}SDHR	SDATA hold	Read	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
^{t}SDSR	SDATA setup	Read	0.3	–	–	µs	Master clock cycle units or PLL cycles if enabled
C_{IN_SI}	Serial interface input pin capacitance		–	–	3.3	pF	
C_{LOAD_SD}	SDATA max load capacitance		–	–	30	pF	
R_{SD}	SDATA pull-up resistor		–	1.5	–	KΩ	

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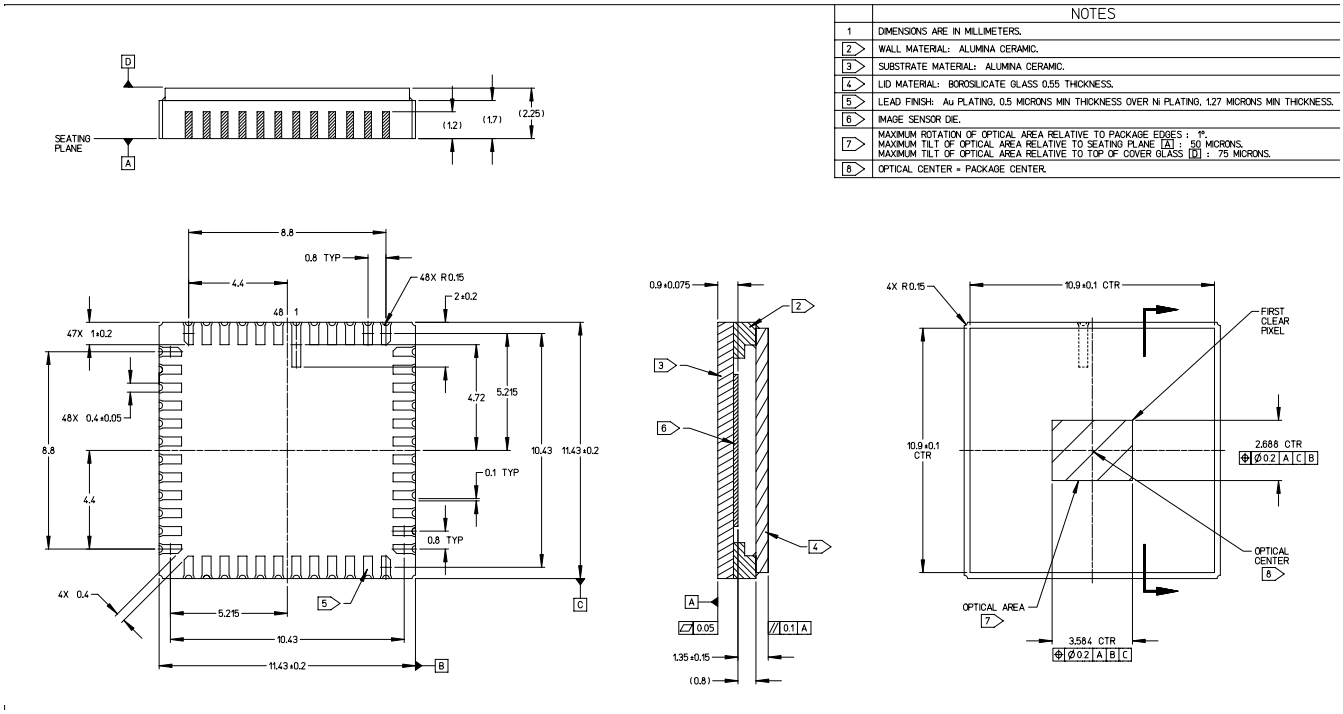
Package and Die Dimensions

Figure 55: CLCC 48–Ball iBGA Package Outline Drawing



Note: All dimensions in millimeters.

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Revision History

Rev. B **1/28/09**

- Updated

Rev. A **10/30/08**

- Initial release

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