1/4-Inch SOC VGA CMOS Digital Image Sensor

MT9V131I29STC (iCSP)
MT9V131C12STC (CLCC)

Features

- Micron® DigitalClarity® CMOS imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra low-power, high fidelity CMOS image sensor
- Superior low-light performance
- Up to 30 fps progressive scan at 27 MHz for high-quality video at VGA resolution
- On-chip image flow processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, 2X fixed zoom
- Automatic exposure, white balance and black compensation, flicker avoidance, color saturation, and defect identification and correction, auto frame rate, back light compensation
- Xenon and LED-type flash support
- Two-wire serial programming interface
- Progressive scan ITU_R BT.656 (YCbCr), YUV, 565RGB, 555RGB, and 444RGB output data formats

Applications

- Security
- Biometrics
- Network cameras
- Toys and other battery-powered products

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/4-inch (4:3)
Active imager size		3.58mm(H) x 2.69mm(V) 4.48mm (diagonal)
Active pixels		640H x 480V (VGA)
Pixel size		5.6µm x 5.6µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		12—13.5 Mp/s/ 24—27 MHz
Frame rate	VGA (640 x 480)	15 fps at 12 MHz (default), programmable up to 30 fps at 27 MHz
	CIF (352 x 288)	Programmable up to 60 fps
	QVGA (320 x 240)	Programmable up to 90 fps
ADC resolution		10-bit, on-chip
Responsivity		1.9 V/lux-sec (550nm)
Dynamic range		60dB
SNR_{MAX}		45dB
Supply voltage		2.8V ±0.25V
Power consumption		<80mW at 2.8V, 15 fps at 12MHz
Operating temperature		–20°C to +60°C
Packaging		44-Ball iCSP, 48-Pin CLCC

The sensor is a complete camera-on-a-chip solution and is designed specifically to meet the demands of battery-powered products such as security cameras, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V131I29STC	44-Ball iCSP
MT9V131C12STC ES	48-Pin CLCC ES (color)
MT9V131C12STCD ES	Demo kit (color)
MT9V131C12STCH ES	Demo kit headboard (color)

General Description

This SOC VGA CMOS image sensor features DigitalClarity—Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The MT9V131 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8-bit port, as shown in Figure 2 on page 3. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. The sensor can be put in an ultra-low power sleep mode by asserting the STANDBY pin. Output pads can also be tri-stated by de-asserting the OE# pin. The MT9V131 internal registers can be configured using a two-wire serial interface.

The MT9V131 can be programmed to output progressive scan images up to 30 fps in an 8-bit ITU_R BT.656 (YCbCr) formerly CCIR656, YUV, 565RGB, 555RGB, or 444RGB formats. The FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Table 3 lists typical values of MT9V131 performance parameters.

Table 3: MT9V131 Detailed Performance Parameters

Parameter		Typ	Unit
Pixel count			
	Active pixel	0.31	Million Pixels
Resolution		640 x 480	H X V
Optical format		1/4	Inches
Power consumption		<80	mW
Dynamic range		60	dB
Shutter type		Rolling	Type
Output gain		28	e-/LSB
Read noise		6	e-RMS at 16X
Dark current		150	e-/pix/sec at 55°C
Responsivity		2.5	V/lux-sec
Operating frequency			
	Master clock	24 to 27	MHz
	Data rate	12 to 13.5	Mp/s
Operating temperature		–20 to +60	°C

Figure 1 illustrates the MT9V131 quantum efficiency in relation to wavelength.

Figure 1: MT9V131 Quantum Efficiency vs. Wavelength

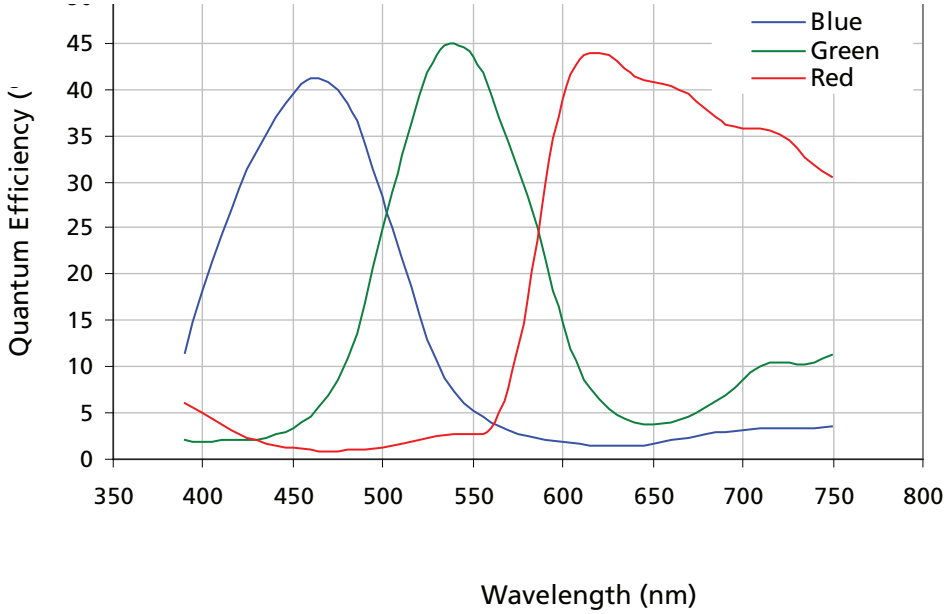
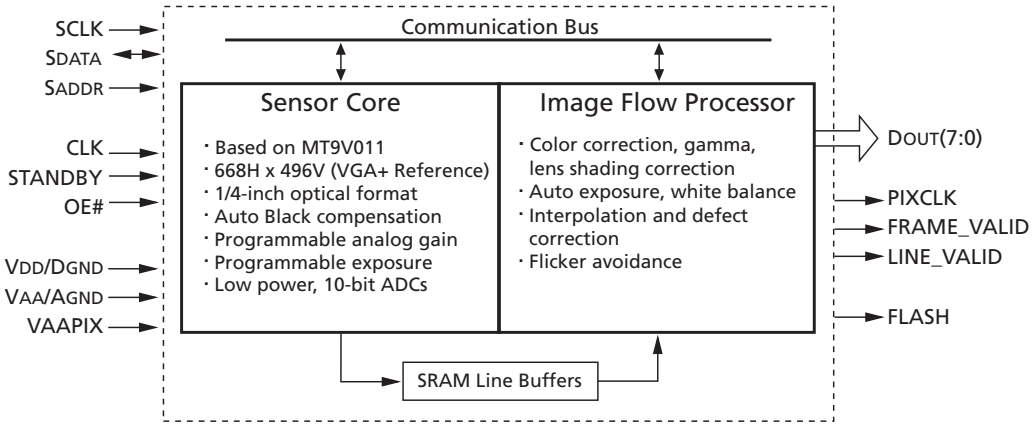


Figure 2: Chip Block Diagram

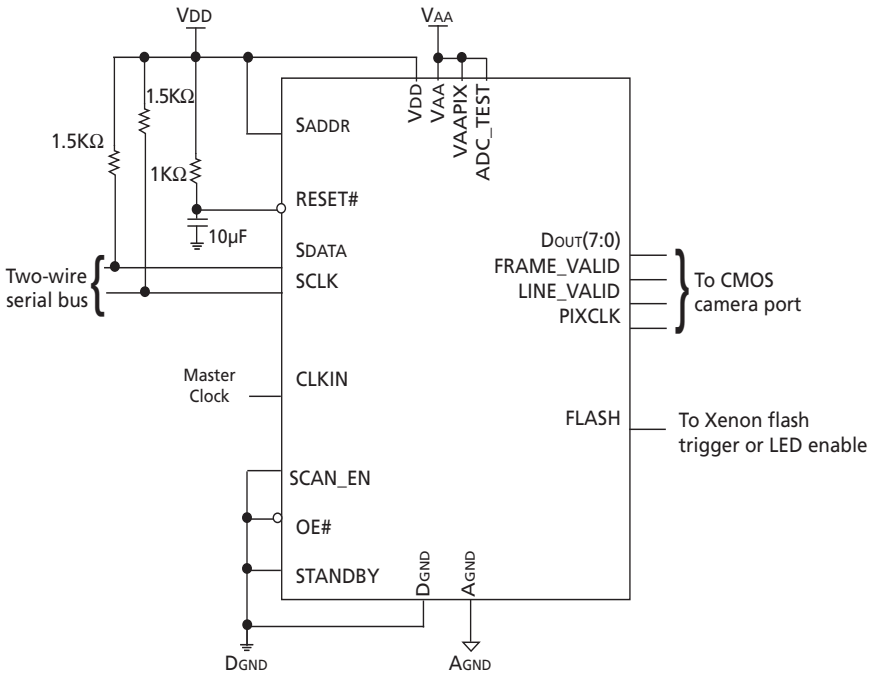


The MT9V131 can accept the input clock of up to 27 MHz, delivering 30 fps. With power-on defaults, the camera is configured to deliver 15 fps at 12 MHz and automatically slows down the frame rate in low-light conditions to achieve longer exposures and better image quality.

Internally, the MT9V131 consists of a sensor core and an image flow processor. The sensor core functions to capture raw Bayer-encoded images that are input into the IFP as shown in Figure 2. The IFP processes the incoming stream to create interpolated, color-corrected output and controls the sensor core to maintain the desirable exposure and color balance.

Figure 3 shows MT9V131 typical connections. For low-noise operation, the MT9V131 requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

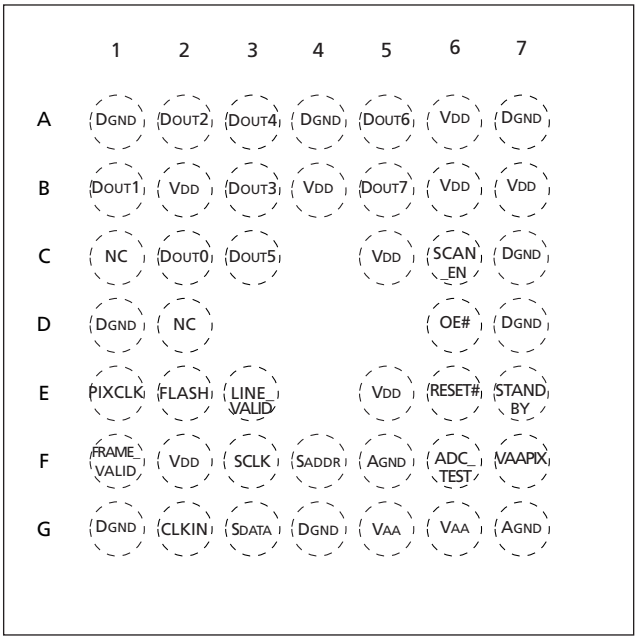
Figure 3: Typical Configuration (Connection)



Note: For two-wire serial interface, a 1.5KΩ resistor is recommended, but may be greater for slower two-wire speed.

Ball Assignment

Figure 4: 44-Ball iCSP Pinout Diagram



Top View
(Ball Down)

Figure 5: 48-Pin CLCC Pinout Diagram

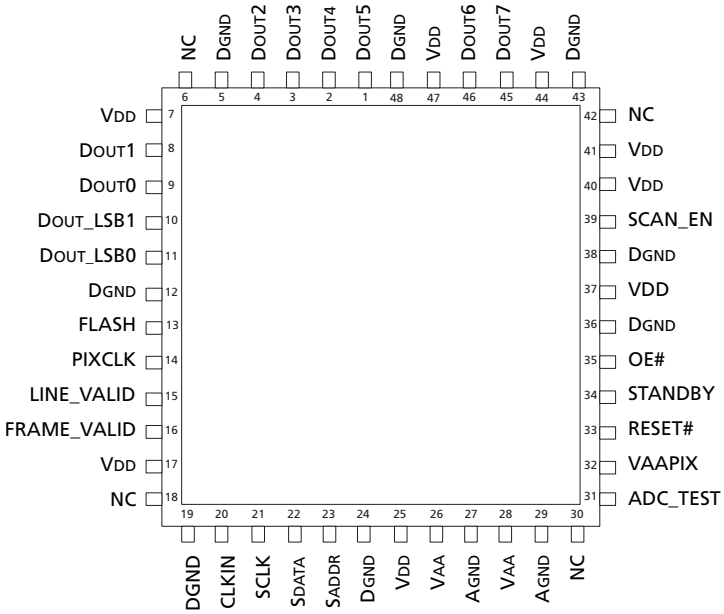


Table 4: Ball and Pin Description

Symbol	CLCC Pin	iCSP Ball	Type	Description
CLKIN	20	G2	Input	Master clock into sensor. Default is 12 MHz (27 MHz maximum).
SCLK	21	F3	Input	Serial clock.
SADDR	23	F4	Input	Serial interface address select: Reg0xB8 when HIGH (default). Reg0x90 when LOW.
ADC_TEST	31	F6	Input	Tie to VAAPIX (factory use only).
RESET#	33	E6	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
STANDBY	34	E7	Input	When HIGH, puts the imager in ultra-low power standby mode.
OE#	35	D6	Input	Output_Enable_Bar pin. When HIGH, tri-state all outputs except SDATA (tie LOW for normal operation).
SCAN_EN	39	C6	Input	Tie to digital ground.
SDATA	22	G3	I/O	Serial data I/O.
FLASH	13	E2	Output	Flash strobe.
PIXCLK	14	E1	Output	Pixel clock out. Pixel data output are valid during rising edge of this clock. IFP Reg0x08 [9] inverts polarity. Frequency = Master clock.
LINE_VALID	15	E3	Output	Active HIGH during line of selectable valid pixel data.
FRAME_VALID	16	F1	Output	Active HIGH during frame of valid pixel data.
DOUT7	45	B5	Output	ITU_R BT.656/RGB data bit 7 (MSB).
DOUT6	46	A5	Output	ITU_R BT.656/RGB data bit 6.
DOUT5	1	C3	Output	ITU_R BT.656/RGB data bit 5.
DOUT4	2	A3	Output	ITU_R BT.656/RGB data bit 4.
DOUT3	3	B3	Output	ITU_R BT.656/RGB data bit 3.
DOUT2	4	A2	Output	ITU_R BT.656/RGB data bit 2.
DOUT1	8	B1	Output	ITU_R BT.656/RGB data bit 1.
DOUT0	9	C2	Output	ITU_R BT.656/RGB data bit 0 (LSB).
VDD	7, 17, 25, 40, 41, 44, 47	A6, B2, B4, B6, B7, C5, E5, F2	Supply	Digital power (2.8V).
VAA	26, 28	G5, G6	Supply	Analog power (2.8V).
VAAPIX	32	F7	Supply	Pixel array power (2.8V).
AGND	27, 29	F5, G7	Supply	Analog ground.
DGND	5, 12, 24, 36, 38, 43, 48	A1, D1, A4, A7, C7, D7, G1, G4	Supply	Digital ground.
NC	6, 18, 30, 42	C1, D2	–	No connect.

Image Flow Processor

Overview of Architecture

The image flow processor consists of a color processing pipeline and a measurement and control logic block, as shown in Figure 6 on page 8. The stream of raw data from the sensor enters the pipeline and undergoes a number of transformations. Image stream processing starts from conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel and defective pixels are corrected. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections and is formatted for final output.

The measurement and control logic continuously accumulates statistics about image brightness and color. Indoor 50/60Hz flicker is detected and automatically updated when possible. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains, which are sent to the sensor core through the communication bus.

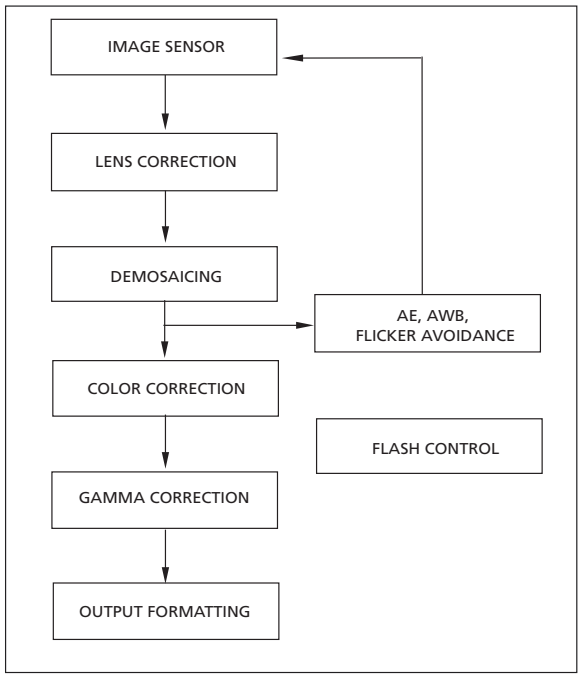
Color correction is achieved through linear transformation of the image with a 3 x 3 color correction matrix. Color saturation can be adjusted in the range from zero (black and white) to 1.25 (125% of full color saturation).

Gamma correction compensates for nonlinear dependence of the display device output versus driving signal (monitor brightness versus CRT voltage).

Output and Formatting

Processed video can be output in the form of a progressive scan ITU_R BT.656 or RGB stream. ITU_R BT.656 (default) stream contains 4:2:2 data with optional embedded synchronization codes. This kind of output is typically suitable for subsequent display by standard video equipment. For JPEG/MPEG compression, YUV/ encoding is suitable. RGB functionality is provided to support LCD devices. The MT9V131 can be configured to output 16-bit RGB (RGB565) and 15-bit RGB (RGB555), as well as two types of 12-bit RGB (RGB444). The user can configure internal registers to swap odd and even bytes, chrominance channels, and luminance and chrominance components to facilitate interface to application processors.

Figure 6: Image Flow Processor Block Diagram



The MT9V131 features smooth, continuous zoom and pan. This functionality is available when the IFP output is downsized in the decimation block. The decimation block can downsize the original VGA image to any integer size, including QVGA, QQVGA, CIF, and QCIF with no loss to the field of view. The user can program the desired size of the output image in terms of horizontal and vertical pixel count. In addition, the user can program the size of a region for downsizing. Continuous zoom is achieved every time the region of interest is less than the entire VGA image. The maximum zoom factor is equal to the ratio of VGA to the size of the region of interest. For example, an image rendered on a 160 x 120 display can be zoomed by 640/160 = 480/120 = 4 times. Continuous pan is achieved by adjusting the starting coordinates of the region of interest.

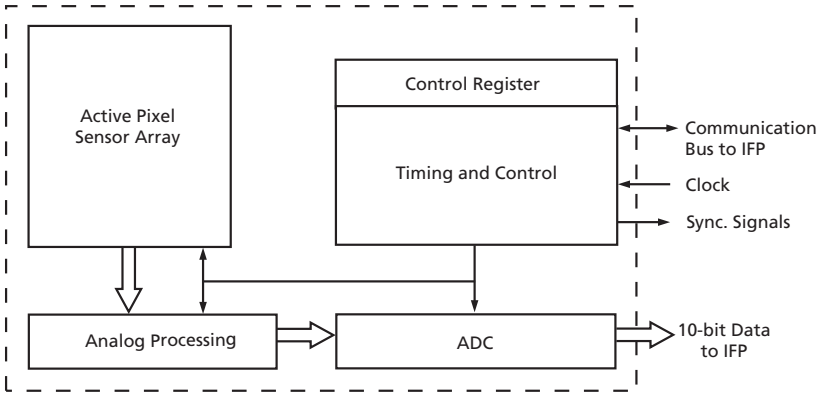
Also, a fixed 2X up-zoom is implemented by means of windowing down the sensor core. In this mode, the IFP receives a QVGA-sized input data and outputs a VGA-size image. The sub-window can be panned both vertically and horizontally by programming sensor core registers.

The MT9V131 supports both LED and Xenon-type flash light sources using a dedicated output pad. For Xenon devices, the pad generates a strobe to fire when the imager's shutter is fully open. For LED, the pad can be asserted or de-asserted asynchronously. Flash modes are configured and engaged over the two-wire serial interface using IFP.

Sensor Core Overview

The sensor consists of a pixel array of 668 x 496 total, analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

Figure 7: Sensor Core Block Diagram



The sensor core image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 8.

Figure 8: Spatial Illustration of Image Readout

$P_{0,0}$ $P_{0,1}$ $P_{0,2}$ ..... $P_{0,n-1}$ $P_{0,n}$ $P_{1,0}$ $P_{1,1}$ $P_{1,2}$ ..... $P_{1,n-1}$ $P_{1,n}$ VALID IMAGE $P_{m-1,0}$ $P_{m-1,1}$ ..... $P_{m-1,n-1}$ $P_{m-1,n}$ $P_{m,0}$ $P_{m,1}$ ..... $P_{m,n-1}$ $P_{m,n}$	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 HORIZONTAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00
00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 VERTICAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 VERTICAL/HORIZONTAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00

Electrical Specifications

The recommended die operating temperature ranges from –20°C to +40°C. The sensor image quality may degrade above +40°C.

Table 5: DC Electrical Characteristics
$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage		V_{DD} - 0.25		V_{DD} + 0.25	V
V_{IL}	Input low voltage		–0.3		0.8	V
I_{IN}	Input leakage current	No pull-up resistor; $V_{IN} = V_{DD}$ or DGND	–5		5.0	µA
V_{OH}	Output high voltage		V_{DD} - 0.2			V
V_{OL}	Output low voltage				0.2	V
I_{OH}	Output high current				15.0	mA
I_{OL}	Output low current				20.0	mA
I_{OZ}	Tri-state output leakage current				5.0	µA
I_{AA}	Analog operating supply current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 10.0 10.0	 20.0 20.0	 25.0 25.0	mA
I_{DD}	Digital operating supply current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 5.0 10.0	 8.0 15.0	 20.0 20.0	mA
I_{AA} Standby	Analog standby supply current	STDBY = V_{DD}	0.0	2.5	5.0	µA
I_{DD} Standby	Digital standby supply current	STDBY = V_{DD}	0.0	2.5	5.0	µA

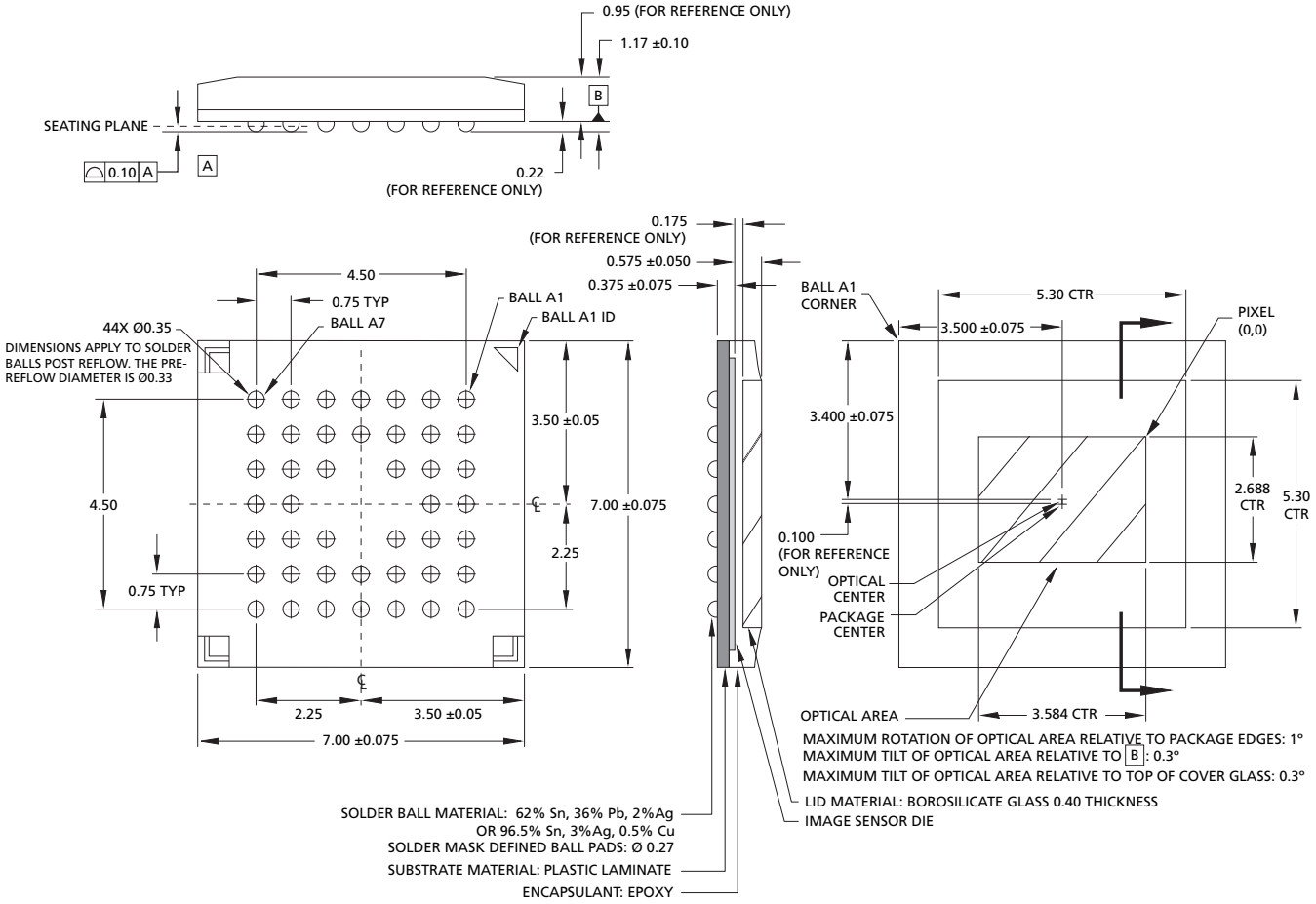
Notes:
1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 6: AC Electrical Characteristics
V_{DD} = V_{AA} = 2.8 ± 0.25V; T_A = 25°C

Definition		Symbol	Condition	Min	Typ	Max	Unit	Notes
Input clock frequency		^tCLKIN		10	12	27	MHz	
Clock duty cycle			50:50	45	50	55	%	1
Input clock rise time		^tR		1	2	5	ns	
Input clock fall time		^tF		1	2	5	ns	
CLKIN to PIXCLK propagation delay	LOW-to-HIGH	$^tPLH_P$	C_{LOAD} = 10pF	6	12	14	ns	3
	HIGH-to-LOW	$^tPHL_P$		6	10	14	ns	
PIXCLK to DOUT[7:0] at 27 MHz	Setup time	^tDSETUP	C_{LOAD} = 10pF	11	18	–	ns	2
	Hold time	^tDHOLD		11	18	–	ns	
PIXCLK to FRAME_VALID and LINE_VALID propagation delay	LOW-to-HIGH	$^tPLH_{F,L}$	C_{LOAD} = 10pF	4	9.0	13	ns	
	HIGH-to-LOW	$^tPHL_{F,L}$		4	7.5	13	ns	
Output rise time		$^tOUT_R$	C_{LOAD} = 10pF	5	7.0	15	ns	
Output fall time		$^tOUT_F$	C_{LOAD} = 10pF	5	9.0	15	ns	

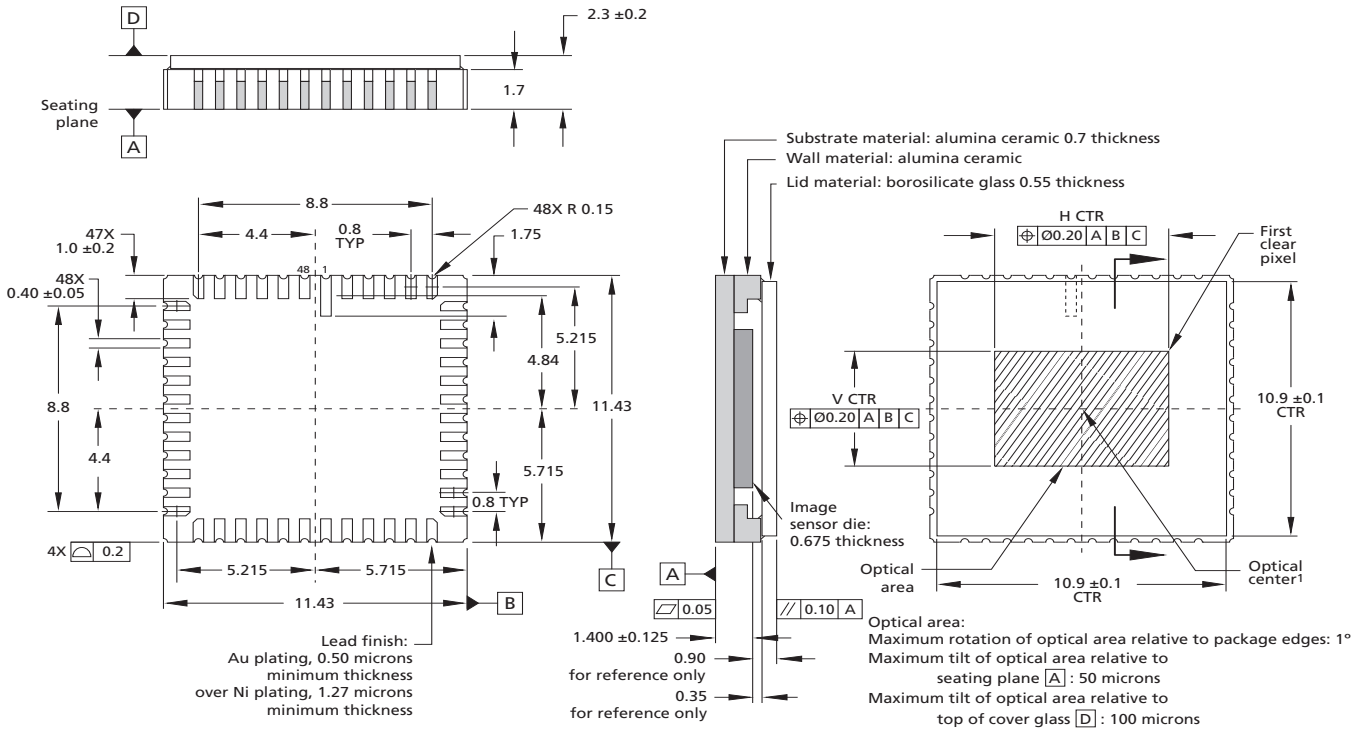
Notes:
1. For 30 fps operation with a 27 MHz clock, the user must have a precise duty cycle equal to 50%. With a slower frame rate and a slower clock, the clock duty cycle can be relaxed.
2. Typical is 1/2 of CLKIN period.
3. PIXCLK can be programmed to be inverted or non-inverted.

Figure 9: 44-Ball iCSP Package Outline



Notes:
1. All dimensions in millimeters.
2. iCSP package information is preliminary.

Figure 10: 48-Pin CLCC Package Outline



Notes:
1. Optical center = package center.
2. All dimensions are in millimeters.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

Rev. B 3/28/2007

- Updated package diagram