1/4-Inch SOC VGA CMOS Digital Image Sensor Die

MT9V125

For the production data sheet, refer to Micron's Web site at www.micron.com

Features

- DigitalClarity® CMOS imaging technology
- System-on-a-chip (SOC)—completely integrated camera system
- NTSC or PAL composite video
- Low-power, interlaced scan CMOS image sensor
- Serial LVDS data output in CCIR656 format
- Supports use of external devices for addition of custom overlay graphics
- Superior low-light performance
- On-die image flow processor (IFP) performs sophisticated processing
- Color recovery and correction, sharpening, gamma, lens shading correction, and on-the-fly defect correction
- Automatic features: auto exposure (AE), auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Two-wire serial programming interface

Data Sheet Applicable to Silicon Revision: Rev 4

General Physical Specifications

- Die thickness: 200µm ±12µm (7.87 mil ±0.5 mil) (*Consult factory for die thickness other than 200µm*)
- Back side wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

2.8V Power Supply

MT9V125D00ATCK12BC1

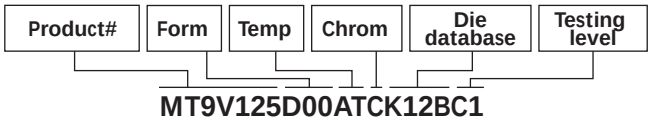
MT9V125D00XTCK12BC1

Die Database K12B

- Die outline, see Figure 2 on page 9
- Singulated die size (nominal dimension): 6,304µm ±25µm x 6,604µm ±25µm
- Bond Pad Location and Identification Tables, see pages 5–8

Options

- Form
  - Die — D
- Testing
  - Standard (level 1) probe — C1



Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Key Performance Parameters

- Optical format: 1/4-inch (4:3)
- Active imager size: 3.58mm(H) x 2.69mm(V), 4.48mm diagonal
- Active pixels: 640H x 480V (VGA)
- NTSC output: 720H x 480V (visible)
- PAL output: 720H x 480V (visible)
- Pixel size: 5.6µm x 5.6µm
- Color filter array: RGB paired Bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Maximum data rate/master clock: 13.5 Mp/s at 27 MHz
- Frame rate: VGA (640H x 480V) 30 fps at 27 MHz
- Integration time: 16µs/33ms (NTSC), 16µs/40ms (PAL)
- ADC resolution: 10-bit, on-die
- Responsivity: 5 V/lux-sec (550nm)
- Pixel dynamic range: 70dB
- SNR MAX: 39dB
- Supply voltage: I/O digital: 2.5–3.1V (2.8V nominal)
  - Core digital: 2.5–3.1V (2.8V nominal)
  - Analog: 2.5–3.1V (2.8V nominal)
- Power consumption: 320mW@2.8V, +25°C
- Operating temperature: –40°C to +85°C

General Description

The Micron® Imaging MT9V125 die is a VGA-format, single-die camera CMOS active-pixel digital image sensor. It captures high-quality color images at VGA resolution with NTSC or PAL interlaced composite video output.

The VGA CMOS image sensor die features DigitalClarity— Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete camera-on-a-die solution. It incorporates sophisticated camera functions on-die and is programmable through a simple two-wire serial interface.

The MT9V125 die outputs interlaced-scan images at 30 or 25 fps, supporting both NTSC and PAL video formats. The image data can be output on any one of four output ports:

- Differential composite analog video
- Single-ended composite analog video
- Low-voltage differential signaling (LVDS)
- Parallel eight-bit digital

The MT9V125 can also be programmed to output progressive scan raw images.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Because the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die analog-to-digital converter (ADC), logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9V125 imager die has 59 bond pads. Refer to Tables 1 and 2 on pages 5–8 for a complete list of bond pads and coordinates.

Figure 1 on page 4 shows the typical die connections for the MT9V125. The die can be powered from a single external voltage supply, provided that the incoming digital and analog conductors are tied together next to the die, and decoupled using capacitors.

Storage Requirements

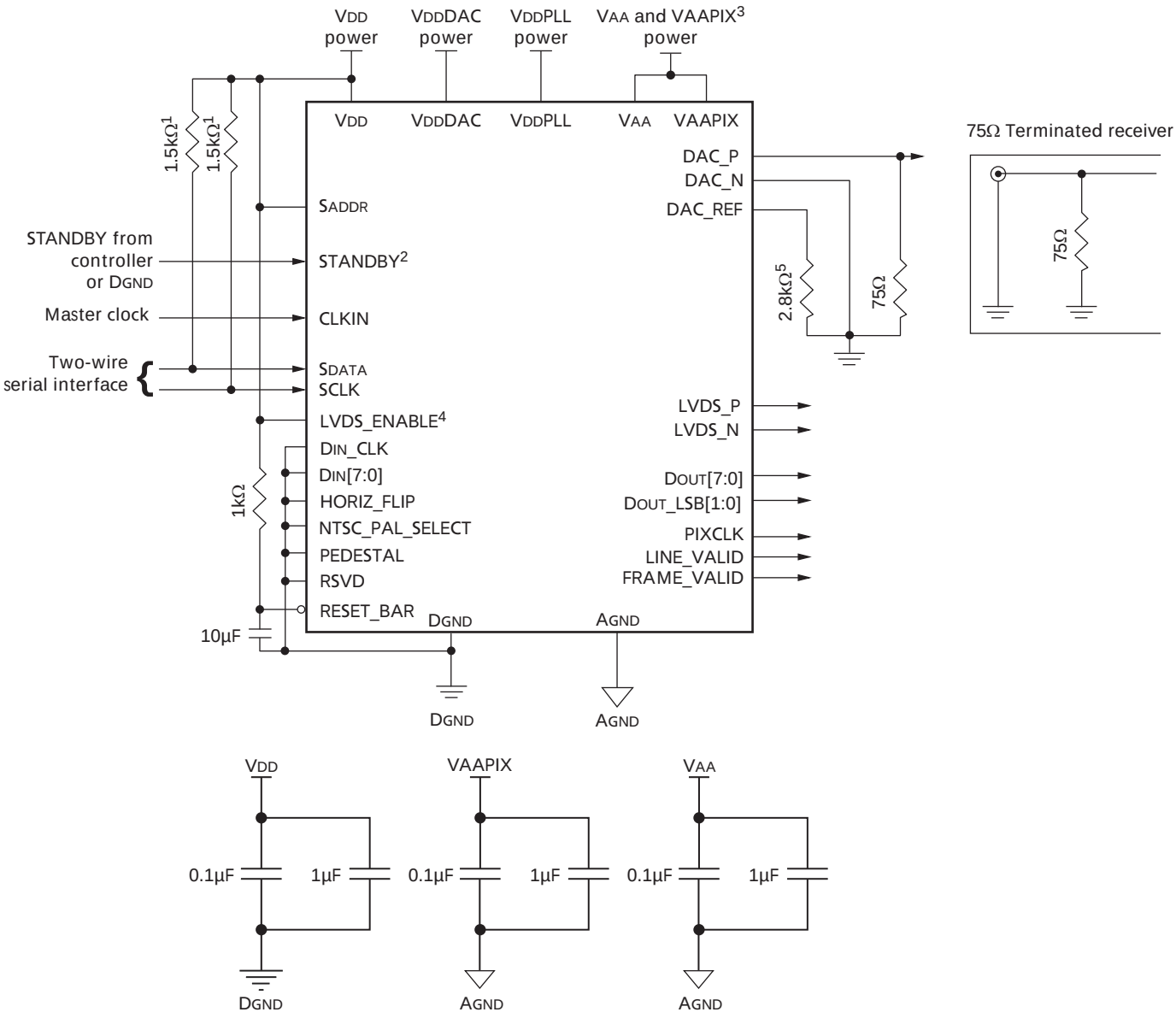
Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Typical Connections

Figure 1: Typical Configuration (without use of overlay)



Notes:
1. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.
2. MT9V125 STANDBY can be connected to the customer's ASIC controller directly or to DGND, depending on the controller's capability.
3. VAA and VAAPIX must be tied to the same potential for proper operation.
4. LVDS_ENABLE must be tied HIGH if LVDS is to be used.
5. Pull down DAC_REF with a 2.4kΩ resistor for 1.4V peak-to-peak video output. For a 1.0V peak-to-peak video output, change the video resistor to 2.8kΩ.

Bond Pad Location and Identification Tables

Table 1: MT9V125 Bond Pad Location and Identification from Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDDPLL	0.00	0.00	0.0000000	0.0000000
2	LVDS_P	638.67	0.00	0.0251445	0.0000000
3	LVDS_N	974.29	0.00	0.0383579	0.0000000
4	DGND5	1105.28	0.00	0.0435150	0.0000000
5	VDD5	1247.12	0.00	0.0490992	0.0000000
6	DAC_P	4458.80	0.00	0.1755433	0.0000000
7	VDDDAC	4600.64	0.00	0.1811276	0.0000000
8	DAC_N	4731.68	0.00	0.1862866	0.0000000
9	DGND6	4862.72	0.00	0.1914457	0.0000000
10	DAC_REF	4993.76	0.00	0.1966047	0.0000000
11	VAAPIX	5467.03	–1021.43	0.2152372	–0.0402136
12	AGND1	5467.03	–1152.47	0.2152372	–0.0453726
13	VAA2	5467.03	–1294.31	0.2152372	–0.0509569
14	VAA1	5467.03	–1436.15	0.2152372	–0.0565411
15	VAA0	5467.03	–3910.79	0.2152372	–0.1539679
16	AGND0	5467.03	–4041.83	0.2152372	–0.1591270
17	PEDESTAL	5467.03	–4502.57	0.2152372	–0.1772665
18	LVDS_ENABLE	5467.03	–4678.36	0.2152372	–0.1841874
19	NTSC_PAL_SELECT	5467.03	–4842.41	0.2152372	–0.1906461
20	HORIZ_FLIP	5467.03	–5018.20	0.2152372	–0.1975669
21	RSVD[2]	5467.03	–5182.25	0.2152372	–0.2040256
22	SADDR	5467.03	–5358.04	0.2152372	–0.2109465
23	SCLK	5467.03	–5522.09	0.2152372	–0.2174051
24	SDATA	5467.03	–5737.27	0.2152372	–0.2258766
25	VDD0	5467.03	–5919.59	0.2152372	–0.2330545
26	DGND0	5467.03	–6050.63	0.2152372	–0.2382136
27	RESET_BAR	4564.03	–6298.21	0.1796860	–0.2479610
28	STANDBY	4160.83	–6298.21	0.1638120	–0.2479610
29	CLKIN	3524.35	–6298.21	0.1387537	–0.2479610
30	VDD1	2582.72	–6298.21	0.1016819	–0.2479610
31	DGND1	2451.68	–6298.21	0.0965228	–0.2479610
32	DIN_CLK	2064.99	–6298.21	0.0812986	–0.2479610
33	DIN0	1661.79	–6298.21	0.0654246	–0.2479610
34	DIN1	1497.74	–6298.21	0.0589659	–0.2479610
35	DIN2	1321.95	–6298.21	0.0520451	–0.2479610
36	DIN3	1157.90	–6298.21	0.0455864	–0.2479610
37	DIN4	748.83	–6298.21	0.0294813	–0.2479610
38	DIN5	584.78	–6298.21	0.0230226	–0.2479610
39	DIN6	408.99	–6298.21	0.0161018	–0.2479610
40	DIN7	244.94	–6298.21	0.0096431	–0.2479610

Table 1: MT9V125 Bond Pad Location and Identification from Center of Pad 1 (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
41	VDD2	–152.56	–6298.21	–0.0060063	–0.2479610
42	DGND2	–283.60	–6298.21	–0.0111654	–0.2479610
43	DGND3	–531.19	–6050.63	–0.0209128	–0.238.2136
44	VDD3	–531.19	–5908.79	–0.0209128	–0.2326293
45	DOUT7	–531.19	–5503.99	–0.0209128	–0.2166923
46	DOUT6	–531.19	–5249.43	–0.0209128	–0.2066703
47	DOUT5	–531.19	–5037.43	–0.0209128	–0.1983238
48	DOUT4	–531.19	–4782.87	–0.0209128	–0.1883018
49	DOUT3	–531.19	–4337.59	–0.0209128	–0.1707711
50	DOUT2	–531.19	–4083.03	–0.0209128	–0.1607490
51	DOUT1	–531.19	–3871.03	–0.0209128	–0.1524026
52	DOUT0	–531.19	–3616.47	–0.0209128	–0.1423805
53	DOUT_LSB1	–531.19	–3171.19	–0.0209128	–0.1248498
54	DOUT_LSB0	–531.19	–2916.63	–0.0209128	–0.1148278
55	PIXCLK	–531.19	–2704.63	–0.0209128	–0.1064813
56	FRAME_VALID	–531.19	–2450.07	–0.0209128	–0.0964593
57	LINE_VALID	–531.19	–2238.07	–0.0209128	–0.0881128
58	VDD4	–531.19	–1801.19	–0.0209128	–0.0709128
59	DGND4	–531.19	–1670.15	–0.0209128	–0.0657537

Notes: 1. Reference to center of each bond pad from center of bond pad 1.
2. RSVD bond pad must be connected to DGND for proper device functionality.

Table 2: MT9V125 Bond Pad Location and Identification from Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDDPLL	–2467.92	3149.11	–0.0971622	0.1239805
2	LVDS_P	–1829.25	3149.11	–0.0720177	0.1239805
3	LVDS_N	–1493.63	3149.11	–0.0588043	0.1239805
4	DGND5	–1362.64	3149.11	–0.0536472	0.1239805
5	VDD5	–1220.80	3149.11	–0.0480630	0.1239805
6	DAC_P	1990.88	3149.11	0.0783811	0.1239805
7	VDDDAC	2132.72	3149.11	0.0839654	0.1239805
8	DAC_N	2263.76	3149.11	0.0891244	0.1239805
9	DGND6	2394.80	3149.11	0.0942835	0.1239805
10	DAC_REF	2525.84	3149.11	0.0994425	0.1239805
11	VAAPIX	2999.11	2127.68	0.1180750	0.0837669
12	AGND1	2999.11	1996.64	0.1180750	0.0786079
13	VAA2	2999.11	1854.80	0.1180750	0.0730236
14	VAA1	2999.11	1712.96	0.1180750	0.0674394
15	VAA0	2999.11	–761.68	0.1180750	–0.0299874
16	AGND0	2999.11	–892.72	0.1180750	–0.0351465
17	PEDESTAL	2999.11	–1353.47	0.1180750	–0.0532860
18	LVDS_ENABLE	2999.11	–1529.26	0.1180750	–0.0602069
19	NTSC_PAL_SELECT	2999.11	–1693.31	0.1180750	–0.0666656
20	HORIZ_FLIP	2999.11	–1869.10	0.1180750	–0.0735864
21	RSVD[2]	2999.11	–2033.15	0.1180750	–0.0800451
22	SADDR	2999.11	–2208.94	0.1180750	–0.0869659
23	SCLK	2999.11	–2372.99	0.1180750	–0.0934246
24	SDATA	2999.11	–2588.16	0.1180750	–0.1018961
25	VDD0	2999.11	–2770.48	0.1180750	–0.1090740
26	DGND0	2999.11	–2901.52	0.1180750	–0.1142331
27	RESET_BAR	2096.11	–3149.11	0.0825238	–0.1239805
28	STANDBY	1692.91	–3149.11	0.0666498	–0.1239805
29	CLKIN	1056.43	–3149.11	0.0415915	–0.1239805
30	VDD1	114.80	–3149.11	0.0045197	–0.1239805
31	DGND1	–16.24	–3149.11	–0.0006394	–0.1239805
32	DIN_CLK	–402.94	–3149.11	–0.0158636	–0.1239805
33	DIN0	–806.14	–3149.11	–0.0317376	–0.1239805
34	DIN1	–970.19	–3149.11	–0.0381963	–0.1239805
35	DIN2	–1145.98	–3149.11	–0.0451171	–0.1239805
36	DIN3	–1310.03	–3149.11	–0.0515758	–0.1239805
37	DIN4	–1719.10	–3149.11	–0.0676809	–0.1239805
38	DIN5	–1883.15	–3149.11	–0.0741396	–0.1239805
39	DIN6	–2058.94	–3149.11	–0.0810604	–0.1239805
40	DIN7	–2222.99	–3149.11	–0.0875191	–0.1239805
41	VDD2	–2620.48	–3149.11	–0.1031685	–0.1239805
42	DGND2	–2751.52	–3149.11	–0.1083276	–0.1239805

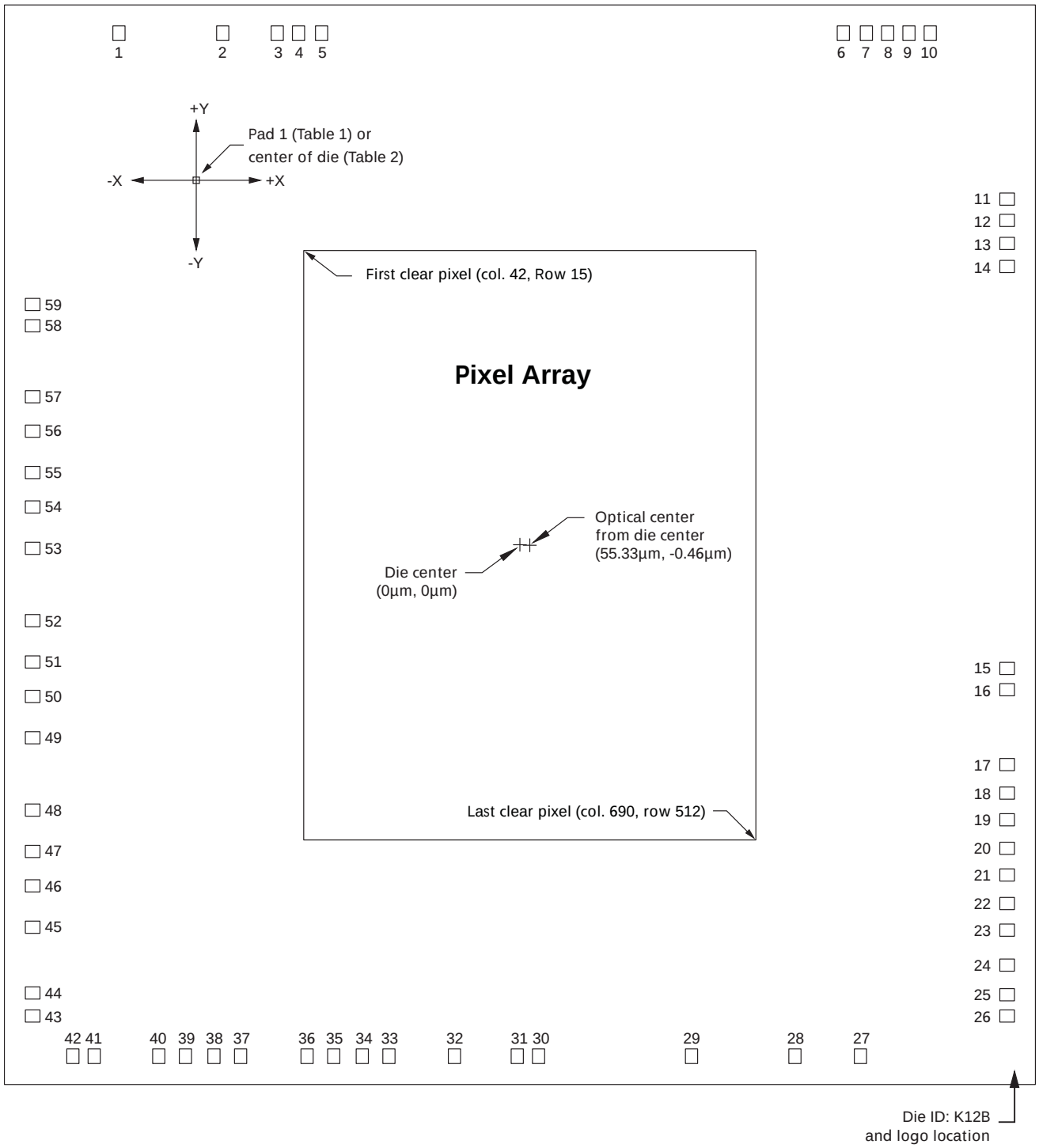
Table 2: MT9V125 Bond Pad Location and Identification from Center of Die (0, 0) (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
43	DGND3	–2999.11	–2901.52	–0.1180750	–0.1142331
44	VDD3	–2999.11	–2759.68	–0.1180750	–0.1086488
45	DOUT7	–2999.11	–2354.88	–0.1180750	–0.0927118
46	DOUT6	–2999.11	–2100.32	–0.1180750	–0.0826898
47	DOUT5	–2999.11	–1888.32	–0.1180750	–0.0743433
48	DOUT4	–2999.11	–1633.76	–0.1180750	–0.0643213
49	DOUT3	–2999.11	–1188.48	–0.1180750	–0.0467906
50	DOUT2	–2999.11	–933.92	–0.1180750	–0.0367685
51	DOUT1	–2999.11	–721.92	–0.1180750	–0.0284220
52	DOUT0	–2999.11	–467.36	–0.1180750	–0.0184000
53	DOUT_LSB1	–2999.11	–22.08	–0.1180750	–0.0008693
54	DOUT_LSB0	–2999.11	232.48	–0.1180750	0.0091528
55	PIXCLK	–2999.11	444.48	–0.1180750	0.0174992
56	FRAME_VALID	–2999.11	699.04	–0.1180750	0.0275213
57	LINE_VALID	–2999.11	911.04	–0.1180750	0.0358677
58	VDD4	–2999.11	1347.92	–0.1180750	0.0530677
59	DGND4	–2999.11	1478.96	–0.1180750	0.0582268

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. RSVD bond pad must be connected to DGND for proper device functionality.

Die Features

Figure 2: Die Outline (Top View)



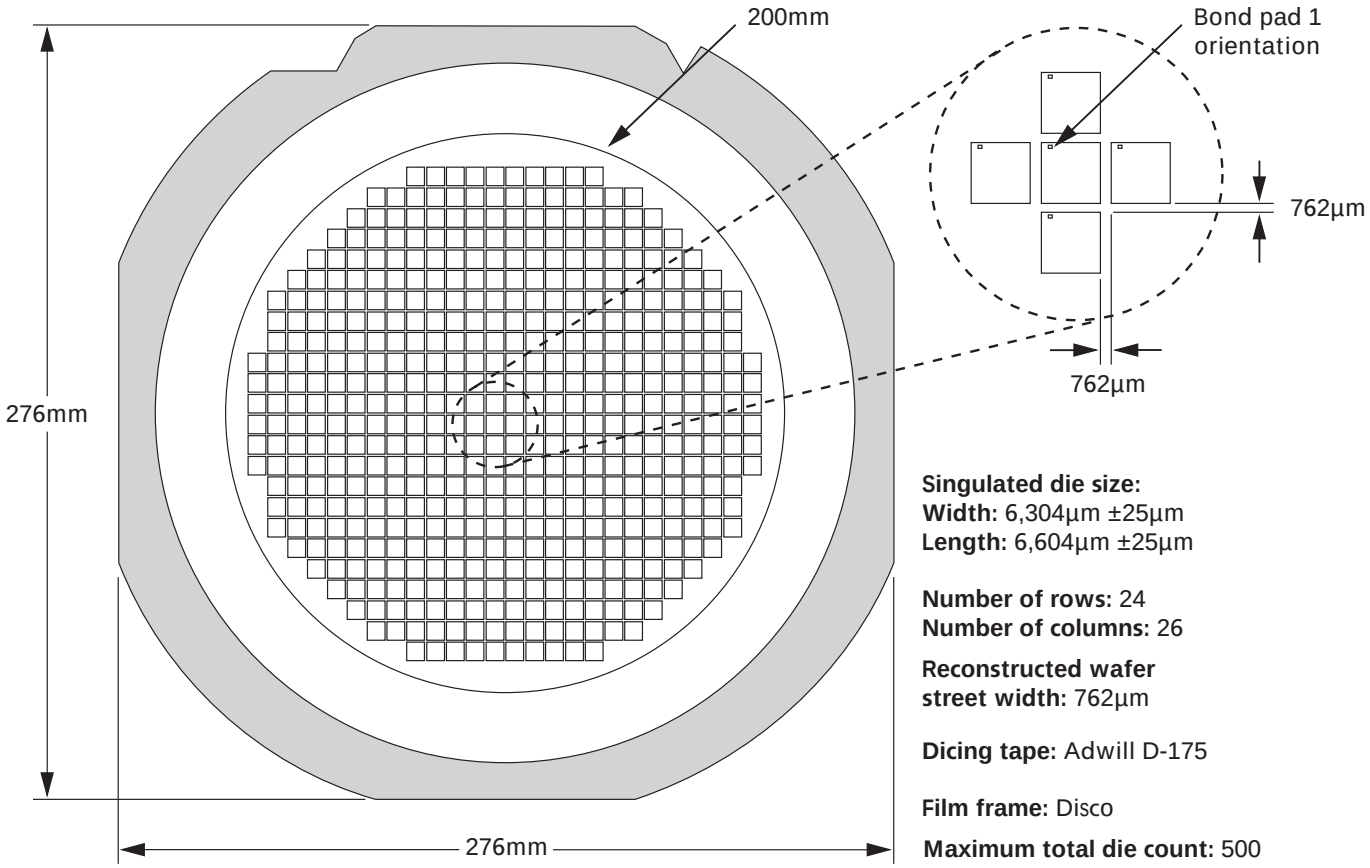
Physical Specifications

Table 3: Die Dimensions

Features	Dimensions
Die thickness	200µm ±12µm (7.87 mil ±0.5 mil)
Singulated die size *Width:* *Length:*	 6,304µm ±25µm 6,604µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	131.04µm (5.159 mil)
Optical array *Optical center from die center:* *Optical center from center of pad 1:*	 X = 55.33µm, Y = –0.46µm X = 2,523.25µm, Y = –3,149.57µm
First clear pixel (col. 42, row 15)[1] *From die center:* *From center of pad 1:*	 X = –1,330.68µm, Y = 1,811.14µm X = 1,137.24µm, Y = –1,337.97µm
Last clear pixel (col. 690, row 512)[1] *From die center:* *From center of pad 1:*	 X = 1,452.53µm, Y = –1,817.66µm X = 3,920.45µm, Y = –4,966.77µm

Notes: 1. Physical coordinates are used for these values. Physical coordinates range from 0 to 515 in the vertical direction. The first two rows and last two rows cannot be accessed using sensor registers. Logical coordinates, which are physical coordinates minus the first and last two rows, are used to describe the sensor array in all other MT9V125 documents. The logical coordinate vertical range is from 0 to 511.

Figure 3: MT9V125 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 6,304µm ±25µm
Length: 6,604µm ±25µm

Number of rows: 24
Number of columns: 26

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 500

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Revision History

Rev. G, Production 12/07

- Updated “Key Performance Parameters” on page 1
- Added “Data Sheet Applicable to Silicon Revision: Rev 4” on page 1
- Added new part number under “Order Information” on page 1
- Changed pull-up resistor from 2.4kΩ to 2.8kΩ in Figure 1 on page 4
- RESET# updated to RESET_BAR throughout the document

Rev. F, Production 8/07

- Updated specifications under “Key Performance Parameters” on page 1
- Updated to latest format
- Added DigitalClarity to trademark logo, last page

Rev. E, Production 7/06

- Updated die thickness and TBDs in “General Physical Specifications” on page 1 and Table 3 on page 10
- Updated Figure 1 on page 4
- Added PDF to Doc ID number

Rev. D, Advance 3/06

- Corrected die center/optical center information in Figure 2 on page 9 and Table 3 on page 10

Rev. C, Advance 2/06

- Updated template

Rev. B, Advance 7/05

- Updated **Figure 1**: added V_{DD}DAC and V_{DD}PLL, tied LVDS_ENABLE above third resistor

Rev. A, Advance 6/05

- Initial release