1/3-Inch 2-Megapixel System-On-A-Chip (SOC) CMOS Digital Image Sensor Die

MT9D111

For functional and parametric specifications, refer to the product data sheet on Micron's Web site: www.micron.com/products/imaging.

Features

- DigitalClarity® CMOS imaging technology
- Ultra low-power, low-cost, progressive scan
- On-die phase lock loop (PLL)
- Integrated auto focus and optical zoom
- Real-time JPEG encoder
- Integrated microcontroller for flexibility
- On-die image flow processor (IFP) for single-die camera module
- Programmable I/O slew rate
- 2 x 2 pixel binning
- Mechanical shutter support
- Automatic image correction and enhancement
- Automatic Xenon- and LED-type flash support with fast exposure adaptation
- Two-wire serial interface
- ITU-R BT.601 (YCbCr), 565RGB, 555RGB, 444RGB, and raw output data formats
- JPEG 4:2:2 and 4:2:0 outputs

General Physical Specifications

- Die thickness: 305µm ±12µm
  (Consult factory for other die thickness)
- Backside die surface of bare silicon
- Typical metal 1 thickness: 3.1KÅ
- Typical metal 2 thickness: 3.1KÅ
- Typical metal 3 thickness: 6.1KÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2KÅ nitride over 6.0KÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Options

- Form
  Die D
- Testing
  Standard (level 1) probe C1

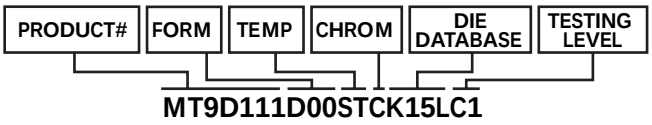
Die Database K15L

- Die outline (see page 8)
- Singulated die size (nominal dimension): 8,199µm ±25µm x 7,845µm ±25µm
- See Tables 1 and 2, "K15L Bond Pad Location and Identification," on pages 4–7.

Order Information

MT9D111D00STCK15LC1

Note: Please consult die distributor or factory before ordering to verify long-term availability of these die products.



Key Performance Parameters

- Optical format: 1/3-inch (4:3)
- Full resolution: 1,600 x 1,200 (UXGA) pixels
- Pixel size: 2.8µm x 2.8µm
- Active pixel array area: 4.73mm x 3.52mm
- Shutter type: Electronic rolling shutter (ERS) with global reset
- Maximum frame rate: 15 frames per second (fps) at full resolution, 30 fps in preview mode (800 x 600)
- Maximum data rate/master clock: 80 MB/s/ 6 MHz to 80 MHz
- ADC resolution: 10-bit, on-die
- Responsivity: 1.0V/lux-sec at 550nm
- Dynamic range: 71dB
- SNRmax: 42.3dB
- Supply voltage: Analog, 2.5V–3.1V; Digital, 1.7V–1.95V; I/O, 1.7V–3.1V; PLL, 2.5V–3.1V
- Power consumption: 348mW at 15 fps, full resolution; 223mW at 30 fps, preview mode
- Operating temperature: –30°C to +70°C

General Description

The Micron® Imaging MT9D111 die is a 1/3-inch 2-megapixel CMOS image sensor with an integrated advanced camera system. The camera system includes a sophisticated image flow processor (IFP), a real-time JPEG encoder, and a microcontroller. Also included are support for flash, auto focus, optical zoom, and mechanical shutter. The system-on-chip (SOC) device has ultra-low-power requirements and superior low-light performance that is particularly suitable for mobile applications.

The sensor consists of an active-pixel array and an IFP managed by a microcontroller with a maximum output image resolution of 1,600 x 1,200 pixels

This 2-megapixel CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die analog-to-digital converter (ADC), logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications in this document are provided for reference only. Please refer to the packaged product data sheets found on Micron's Web site (www.micron.com) for functional and parametric specifications.

Bonding Instructions

The MT9D111 die has 85 bond pads. Refer to Tables 1 and 2, on pages 4–7, for a complete list of bond pads and coordinates.

The MT9D111 die does not require the user to determine bond option features.

The die also has several pads defined as "Do Not Use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

To ensure proper device operation, all power supply bond pads must be bonded.

Figure 1 on page 3, shows the MT9D111 typical die connections. For low-noise operation the MT9D111 die requires separate supplies for analog and digital power. Both power supply rails should be decoupled to ground using ceramic capacitors. Use of inductance filters is not recommended.

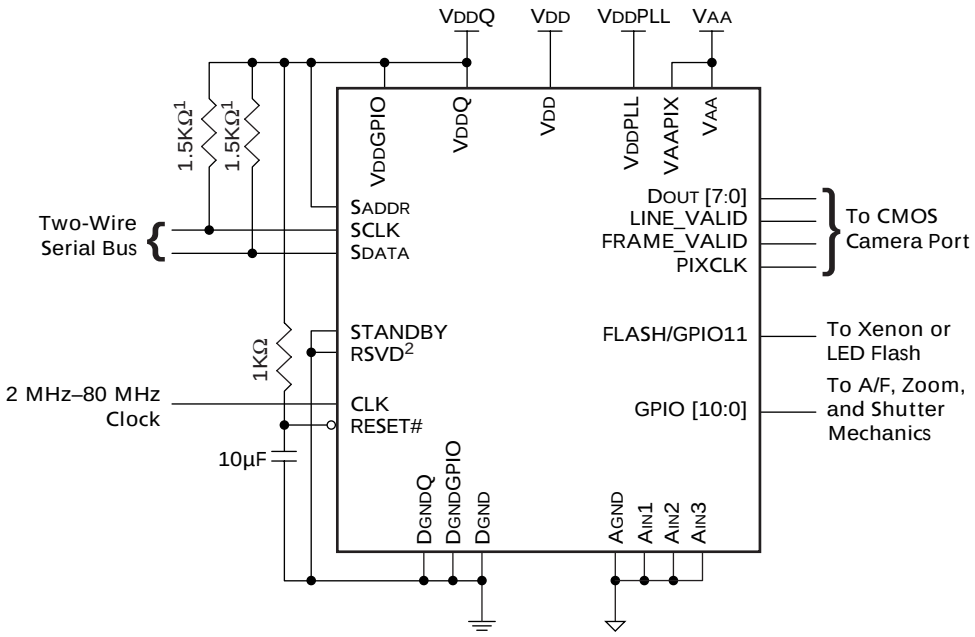
Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Figure 1: Typical Configuration (Connection)



Notes:
1. Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.
2. RSVD must be connected to digital ground for normal device operation.

Bond Pad Location and Identification

Table 1: K15L Bond Pad Location From Center of Pad 1

Pad	MT9D111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDDQ5	0.00	0.00	0.0000000	0.0000000
2	DOUT7	192.80	0.00	0.0075906	0.0000000
3	DOUT6	404.80	0.00	0.0159370	0.0000000
4	DOUT5	659.36	0.00	0.0259591	0.0000000
5	DOUT4	871.36	0.00	0.0343055	0.0000000
6	DGNDQ4	1064.16	0.00	0.0418961	0.0000000
7	VDDQ4	1206.00	0.00	0.0474803	0.0000000
8	DGND9	1337.04	0.00	0.0526394	0.0000000
9	VDD9	1478.88	0.00	0.0582236	0.0000000
10	DOUT3	1671.68	0.00	0.0658142	0.0000000
11	DOUT2	1883.68	0.00	0.0741606	0.0000000
12	DOUT1	2138.24	0.00	0.0841827	0.0000000
13	DOUT0	2350.24	0.00	0.0925291	0.0000000
14	DGNDQ3	2543.04	0.00	0.1001197	0.0000000
15	VDDQ3	2684.88	0.00	0.1057039	0.0000000
16	DGND8	2815.92	0.00	0.1108630	0.0000000
17	VDD8	2957.76	0.00	0.1164472	0.0000000
18	FRAME_VALID	3150.56	0.00	0.1240378	0.0000000
19	LINE_VALID	3362.56	0.00	0.1323843	0.0000000
20	PIXCLK	3617.12	0.00	0.1424063	0.0000000
21	SDATA	3829.12	0.00	0.1507528	0.0000000
22	DGNDQ2	4021.92	0.00	0.1583433	0.0000000
23	VDDQ2	4163.76	0.00	0.1639276	0.0000000
24	SCLK	4317.18	0.00	0.1699675	0.0000000
25	SADDR	4487.10	0.00	0.1766573	0.0000000
26	STANDBY	4657.02	0.00	0.1833470	0.0000000
27	RESET#	4826.94	0.00	0.1900368	0.0000000
28	DGNDQ1	4974.48	0.00	0.1958457	0.0000000
29	VDDQ1	5116.32	0.00	0.2014299	0.0000000
30	DNU[2]	5287.76	0.00	0.2081795	0.0000000
31	DNU	5577.76	0.00	0.2195969	0.0000000
32	DNU	5883.20	0.00	0.2316220	0.0000000
33	DNU	6173.20	0.00	0.2430394	0.0000000
34	DGNDQ0	6305.04	0.00	0.2482299	0.0000000
35	VDDQ0	6446.88	0.00	0.2538142	0.0000000
36	DGND7	6577.92	0.00	0.2589732	0.0000000
37	VDD7	6719.76	0.00	0.2645575	0.0000000
38	CLK	6873.18	0.00	0.2705974	0.0000000
39	VDDPLL0	7251.84	0.00	0.2855055	0.0000000
40	DGND6	7634.07	-3239.91	0.3005537	-0.1275553
41	VDD6	7634.07	-3381.75	0.3005537	-0.1331396
42	AGND2	7187.76	-7538.21	0.2829827	-0.2967799
43	AGND1	7056.72	-7538.21	0.2778236	-0.2967799

Table 1: K15L Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9D111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	AGND0	6925.68	-7538.21	0.2726646	-0.2967799
45	VAA2	6783.84	-7538.21	0.2670803	-0.2967799
46	VAA1	6642.00	-7538.21	0.2614961	-0.2967799
47	VAA0	6500.16	-7538.21	0.2559118	-0.2967799
48	AIN3	6369.12	-7538.21	0.2507528	-0.2967799
49	AIN2	6238.08	-7538.21	0.2455937	-0.2967799
50	AIN1	6107.04	-7538.21	0.2404346	-0.2967799
51	VAAPIX2	5744.88	-7538.21	0.2261764	-0.2967799
52	VAAPIX1	5603.04	-7538.21	0.2205921	-0.2967799
53	VAAPIX0	5461.20	-7538.21	0.2150079	-0.2967799
54	DGNDGPIO2	4307.76	-7538.21	0.1695969	-0.2967799
55	VDDGPIO2	4165.92	-7538.21	0.1640126	-0.2967799
56	GPIO0	3994.40	-7538.21	0.1572598	-0.2967799
57	GPIO1	3739.84	-7538.21	0.1472378	-0.2967799
58	GPIO2	3527.84	-7538.21	0.1388913	-0.2967799
59	GPIO3	3273.28	-7538.21	0.1288693	-0.2967799
60	GPIO4	3061.28	-7538.21	0.1205228	-0.2967799
61	DGNDGPIO1	2868.48	-7538.21	0.1129323	-0.2967799
62	VDDGPIO1	2726.64	-7538.21	0.1073480	-0.2967799
63	DGND5	2595.60	-7538.21	0.1021890	-0.2967799
64	VDD5	2453.76	-7538.21	0.0966047	-0.2967799
65	GPIO5	2260.96	-7538.21	0.0890142	-0.2967799
66	GPIO6	2048.96	-7538.21	0.0806677	-0.2967799
67	GPIO7	1794.40	-7538.21	0.0706457	-0.2967799
68	GPIO8	1582.40	-7538.21	0.0622992	-0.2967799
69	GPIO9	1327.84	-7538.21	0.0522772	-0.2967799
70	VDD4	1145.52	-7538.21	0.0450992	-0.2967799
71	DGND4	1014.48	-7538.21	0.0399402	-0.2967799
72	DGNDGPIO0	883.44	-7538.21	0.0347811	-0.2967799
73	VDDGPIO0	741.60	-7538.21	0.0291699	-0.2967799
74	GPIO10	570.08	-7538.21	0.0224441	-0.2967799
75	FLASH	315.52	-7538.21	0.0124220	-0.2967799
76	RSVD[3]	121.63	-7538.21	0.0047884	-0.2967799
77	VDD3	-36.72	-7538.21	-0.0014457	-0.2967799
78	DGND3	-167.76	-7538.21	-0.0066047	-0.2967799
79	DGND2	-258.39	-3822.39	-0.0101726	-0.1504876
80	VDD2	-258.39	-3680.55	-0.0101726	-0.1449033
81	DGND1	-258.39	-3329.19	-0.0101726	-0.1310703
82	VDD1	-258.39	-3187.35	-0.0101726	-0.1254860
83	VDD0	-258.39	-378.63	-0.0101726	-0.0149065
84	DGND0	-258.39	-247.59	-0.0101726	-0.0097474
85	DGNDQ5	-258.39	-116.55	-0.0101726	-0.0045884

Notes:
1. Reference to center of each bond pad from center of bond pad number 1.
2. DNU = "Do Not Use."
3. RSVD must be connected to digital ground for normal device operation.

Table 2: K15L Bond Pad Location From Center of Die (0, 0)

Pad	MT9D111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDDQ5	-3687.84	3769.11	-0.1451906	0.1483900
2	DOUT7	-3495.04	3769.11	-0.1376000	0.1483900
3	DOUT6	-3283.04	3769.11	-0.1292535	0.1483900
4	DOUT5	-3028.48	3769.11	-0.1192315	0.1483900
5	DOUT4	-2816.48	3769.11	-0.1108850	0.1483900
6	DGNDQ4	-2623.68	3769.11	-0.1032945	0.1483900
7	VDDQ4	-2481.84	3769.11	-0.0977102	0.1483900
8	DGND9	-2350.80	3769.11	-0.0925512	0.1483900
9	VDD9	-2208.96	3769.11	-0.0869669	0.1483900
10	DOUT3	-2016.16	3769.11	-0.0793764	0.1483900
11	DOUT2	-1804.16	3769.11	-0.0710299	0.1483900
12	DOUT1	-1549.60	3769.11	-0.0610079	0.1483900
13	DOUT0	-1337.60	3769.11	-0.0526614	0.1483900
14	DGNDQ3	-1144.80	3769.11	-0.0450709	0.1483900
15	VDDQ3	-1002.96	3769.11	-0.0394866	0.1483900
16	DGND8	-871.92	3769.11	-0.0343276	0.1483900
17	VDD8	-730.08	3769.11	-0.0287433	0.1483900
18	FRAME_VALID	-537.28	3769.11	-0.0211528	0.1483900
19	LINE_VALID	-325.28	3769.11	-0.0128063	0.1483900
20	PIXCLK	-70.72	3769.11	-0.0027843	0.1483900
21	SDATA	141.28	3769.11	0.0055622	0.1483900
22	DGNDQ2	334.08	3769.11	0.0131528	0.1483900
23	VDDQ2	475.92	3769.11	0.0187370	0.1483900
24	SCLK	629.34	3769.11	0.0247770	0.1483900
25	SADDR	799.26	3769.11	0.0314667	0.1483900
26	STANDBY	969.18	3769.11	0.0381565	0.1483900
27	RESET#	1139.10	3769.11	0.0448463	0.1483900
28	DGNDQ1	1286.64	3769.11	0.0506551	0.1483900
29	VDDQ1	1428.48	3769.11	0.0562394	0.1483900
30	DNU[2]	1599.92	3769.11	0.0629890	0.1483900
31	DNU	1889.92	3769.11	0.0744063	0.1483900
32	DNU	2195.36	3769.11	0.0864315	0.1483900
33	DNU	2485.36	3769.11	0.0978488	0.1483900
34	DGNDQ0	2617.20	3769.11	0.1030394	0.1483900
35	VDDQ0	2759.04	3769.11	0.1086236	0.1483900
36	DGND7	2890.08	3769.11	0.1137827	0.1483900
37	VDD7	3031.92	3769.11	0.1193669	0.1483900
38	CLK	3185.34	3769.11	0.1254069	0.1483900
39	VDDPLL0	3564.00	3769.11	0.1403150	0.1483900
40	DGND6	3946.23	529.20	0.1553632	0.0208346
41	VDD6	3946.23	387.36	0.1553632	0.0152504
42	AGND2	3499.92	-3769.11	0.1377921	-0.1483900
43	AGND1	3368.88	-3769.11	0.1326331	-0.1483900
44	AGND0	3237.84	-3769.11	0.1274740	-0.1483900

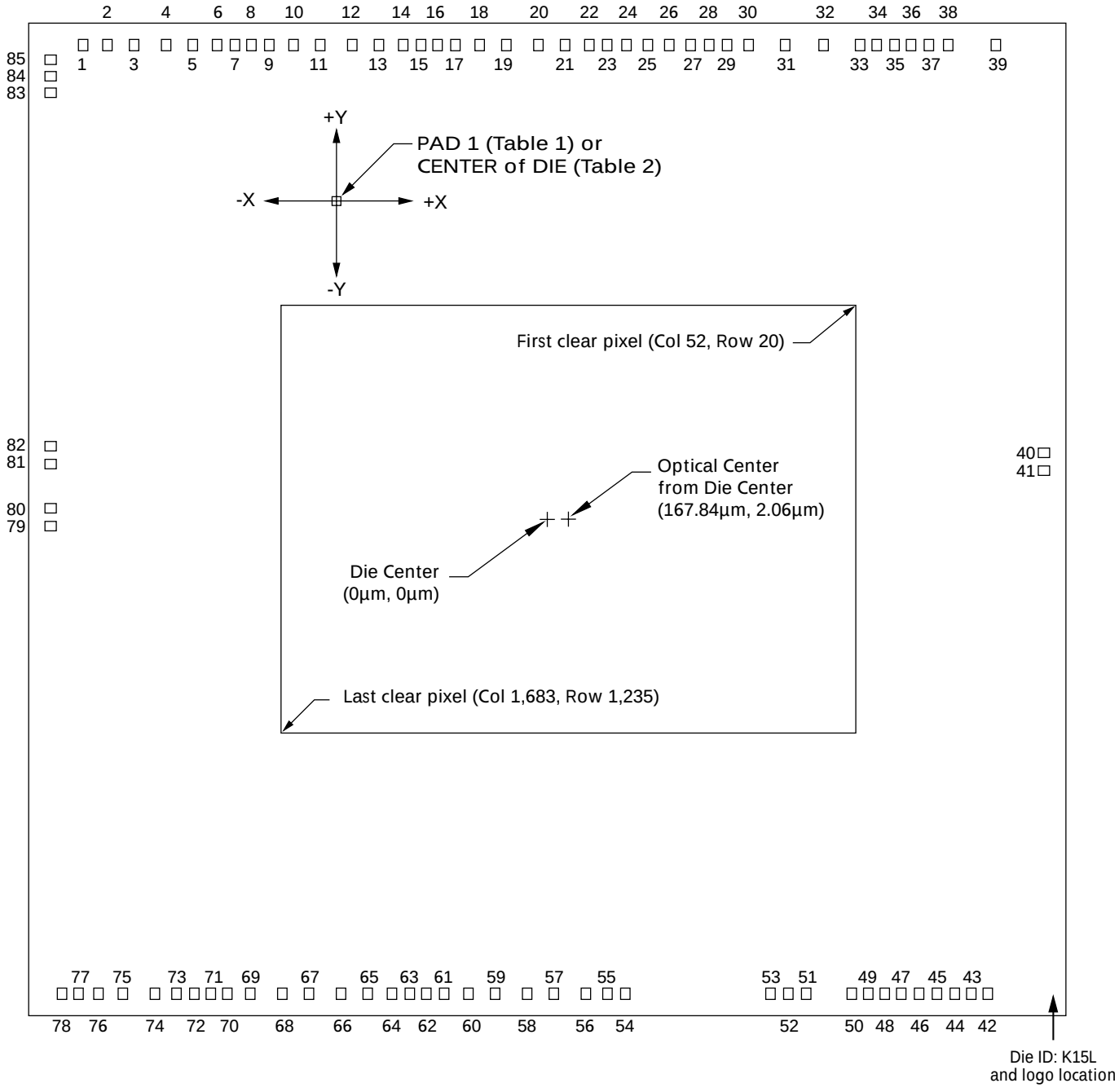
Table 2: K15L Bond Pad Location From Center of Die (0, 0) (continued)

Pad	MT9D111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
45	VAA2	3096.00	-3769.11	0.1218898	-0.1483900
46	VAA1	2954.16	-3769.11	0.1163055	-0.1483900
47	VAA0	2812.32	-3769.11	0.1107213	-0.1483900
48	AIN3	2681.28	-3769.11	0.1055622	-0.1483900
49	AIN2	2550.24	-3769.11	0.1004031	-0.1483900
50	AIN1	2419.20	-3769.11	0.0952441	-0.1483900
51	VAAPIX2	2057.04	-3769.11	0.0809858	-0.1483900
52	VAAPIX1	1915.20	-3769.11	0.0754016	-0.1483900
53	VAAPIX0	1773.36	-3769.11	0.0698173	-0.1483900
54	DGNDGPIO2	619.92	-3769.11	0.0244063	-0.1483900
55	VDDGPIO2	478.08	-3769.11	0.0188220	-0.1483900
56	GPIO0	306.56	-3769.11	0.0120693	-0.1483900
57	GPIO1	52.00	-3769.11	0.0020472	-0.1483900
58	GPIO2	-160.00	-3769.11	-0.0062992	-0.1483900
59	GPIO3	-414.56	-3769.11	-0.0163213	-0.1483900
60	GPIO4	-626.56	-3769.11	-0.0246677	-0.1483900
61	DGNDGPIO1	-819.36	-3769.11	-0.0322583	-0.1483900
62	VDDGPIO1	-961.20	-3769.11	-0.0378425	-0.1483900
63	DGND5	-1092.24	-3769.11	-0.0430016	-0.1483900
64	VDD5	-1234.08	-3769.11	-0.0485858	-0.1483900
65	GPIO5	-1426.88	-3769.11	-0.0561764	-0.1483900
66	GPIO6	-1638.88	-3769.11	-0.0645228	-0.1483900
67	GPIO7	-1893.44	-3769.11	-0.0745449	-0.1483900
68	GPIO8	-2105.44	-3769.11	-0.0828913	-0.1483900
69	GPIO9	-2360.00	-3769.11	-0.0929134	-0.1483900
70	VDD4	-2542.32	-3769.11	-0.1000913	-0.1483900
71	DGND4	-2673.36	-3769.11	-0.1052504	-0.1483900
72	DGNDGPIO0	-2804.40	-3769.11	-0.1104094	-0.1483900
73	VDDGPIO0	-2946.24	-3769.11	-0.1159937	-0.1483900
74	GPIO10	-3117.76	-3769.11	-0.1227465	-0.1483900
75	FLASH	-3372.32	-3769.11	-0.1327685	-0.1483900
76	RSVD[3]	-3566.22	-3769.11	-0.1404022	-0.1483900
77	VDD3	-3724.56	-3769.11	-0.1466362	-0.1483900
78	DGND3	-3855.60	-3769.11	-0.1517953	-0.1483900
79	DGND2	-3946.23	-53.28	-0.1553632	-0.0020976
80	VDD2	-3946.23	88.56	-0.1553632	0.0034866
81	DGND1	-3946.23	439.92	-0.1553632	0.0173197
82	VDD1	-3946.23	581.76	-0.1553632	0.0229039
83	VDD0	-3946.23	3390.48	-0.1553632	0.1334835
84	DGND0	-3946.23	3521.52	-0.1553632	0.1386425
85	DGNDQ5	-3946.23	3652.56	-0.1553632	0.1438016

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = "Do Not Use."
3. RSVD must be connected to digital ground for normal device operation.

Die Features

Figure 2: Die Outline (Top View)

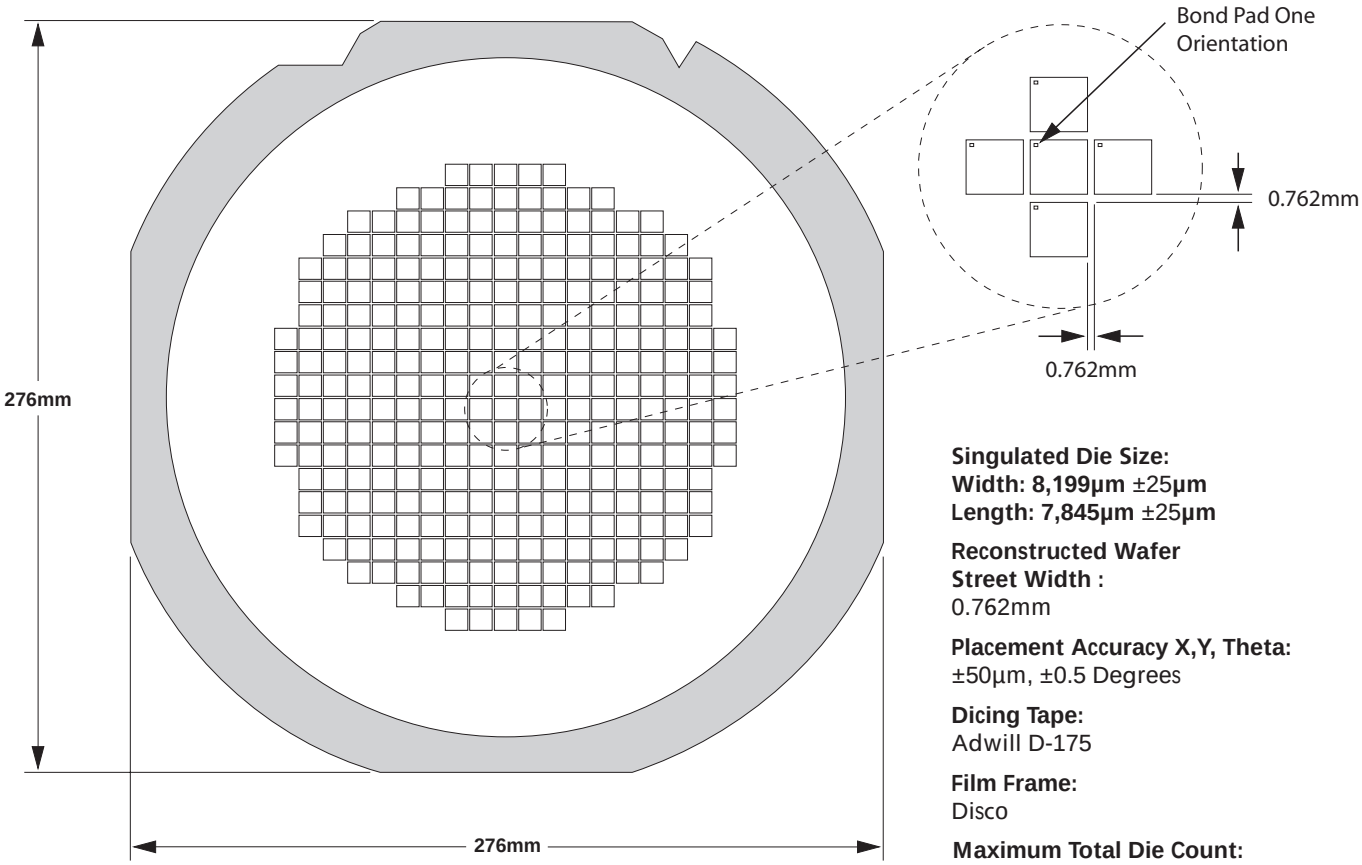


Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	305µm ±12µm (12.0 mil ±0.5 mil)
Singulated die size *Width:* *Length:*	 8,199µm ±25µm 7,845µm ±25µm
Bond pad size (MIN)	85.0µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75.0µm x 90.0µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	131.04µm (5.159 mil)
Optical array *Optical center from die center:* *Optical center from center of pad 1:*	 X = 167.84µm, Y = 2.06µm X = 3,855.68µm, Y = –3,767.05µm
First clear pixel (col 52, row 20) *From die center:* *From center of pad 1:*	 X = 2,451.24µm, Y = 1,702.95µm X = 6,139.08µm, Y = –2,066.16µm
Last clear pixel (col 1,683, row 1,235) *From die center:* *From center of pad 1:*	 X = –2,115.56µm, Y = –1,698.83µm X = 1,572.28µm, Y = –5,467.93µm

Figure 3: K15L Die Orientation in Reconstructed Wafer



Singulated Die Size:
Width: 8,199µm ±25**µm**
Length: 7,845µm ±25**µm**

Reconstructed Wafer Street Width :
0.762mm

Placement Accuracy X,Y, Theta:
±50µm, ±0.5 Degrees

Dicing Tape:
Adwill D-175

Film Frame:
Disco

Maximum Total Die Count:
300

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Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

Revision History

Rev. C, Preliminary **2/06**
- Updated template

Rev. B, Preliminary **8/05**
- Updated template

Rev. A, Preliminary **3/05**
- Initial release