# 1/11-Inch System-on-a-Chip (SOC) CMOS Digital Image Sensor Die

## MT9V113

For the product data sheet, refer to Micron's Web site at www.micron.com

## Features

- DigitalClarity® CMOS imaging technology
- Superior low-light performance
- Ultra low power, low cost
- Internal master clock generated by on-die phase-lock-loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement, including four-channel lens shading correction
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, 565RGB, 555RGB, 444RGB, processed Bayer, RAW8- and RAW10-bit
- Programmable I/O slew rate
- Parallel and serial MIPI data output
- Xenon and LED flash support with fast exposure adaptation
- Independently configurable gamma correction

## General Physical Specifications

- Die thickness: 200µm ±12µm
  *(Consult factory for other thickness)*
- Back side die surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.2kÅ
- Typical metal 3 thickness: 3.2kÅ
- Typical metal 4 thickness: 4.0kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

## Order Information

MT9V113D00STCK22AC1

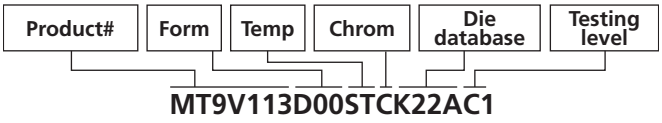
Notes: 1. Consult die distributor or factory before ordering to verify long-term availability of these die products.

## Die Database K22A

- Die outline, see Figure 2 on page 9
- Singulated die size (nominal dimension): 3,485µm ±25µm x 3,729µm ±25µm
- Bond Pad Location and Identification Tables, see pages 5–8

## Options

- Form
  - Die D
- Testing
  - Standard (level 1) probe C1




## Key Performance Parameters

- Optical format: 1/11-inch (4:3)
- Full resolution: 648 x 488 pixels (VGA)
- Pixel size: 2.2µm x 2.2µm
- Dynamic range: 63.5dB
- Responsivity: 1.15 V/lux-sec
- Chief ray angle: 27.12° MAX at 100% image height
- Color filter array: RGB Bayer pattern
- Active pixel array area: 1.43mm x 1.07mm
- Shutter type: electronic rolling shutter (ERS)
- Input clock frequency: 6–48 MHz (PLL-enabled)
- Maximum frame rate: 30 fps at full resolution
- Maximum pixel data output: 14 Mp/s
- Maximum pixel clock frequency: 28 MHz
- Supply voltage: analog: 2.5–3.1V
  - Digital: 1.70–1.95V
  - I/O: 1.70–1.95V or 2.5–3.1V
  - PLL: 2.5–3.1V
  - PHY: 1.70–1.95V (MIPI physical layer)
- ADC resolution: 10-bit, on-die
- Typical power consumption: 80mW at 30 fps, full resolution; 30µW, standby
- Operating temperature: –30°C to +70°C



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## General Description

Micron's MT9V113 die is a 1/11-inch VGA CMOS digital image sensor with an integrated advanced camera system. The camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), and both parallel and serial mobile industry processor interface (MIPI) ports. The microcontroller manages all functions of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 648 x 488 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has an ultra-low power operational mode and a superior low-light performance that is particularly suitable for mobile applications. The MT9V113 die features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

## Die Testing Procedures

Micron® imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Because the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

## Functional Specifications

The specifications provided here are for reference only. For target functional and parametric specifications, refer to the packaged product data sheet found on Micron's Web site.

## Bonding Instructions

The MT9V113 die has 48 bond pads. Refer to Tables 1 and 2 on pages 5–8 for a complete list of bond pads and coordinates.

The MT9V113 die does not require the user to determine bond option features.



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The die also has several pads defined as “do not use.” These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

To ensure proper device operation, all power supply bond pads must be bonded.

Figure 1 on page 4 shows typical MT9V113 device connections. For low-noise operation, the MT9V113 requires separate supplies for analog and digital sections of the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9V113 provides dedicated signals for digital core, PHY, and I/O power domains that can be at different voltages. The PLL and analog circuitry require clean power sources.

## Storage Requirements

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

## Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron’s QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the “Accelerated Life” and “Environmental Stress” tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.



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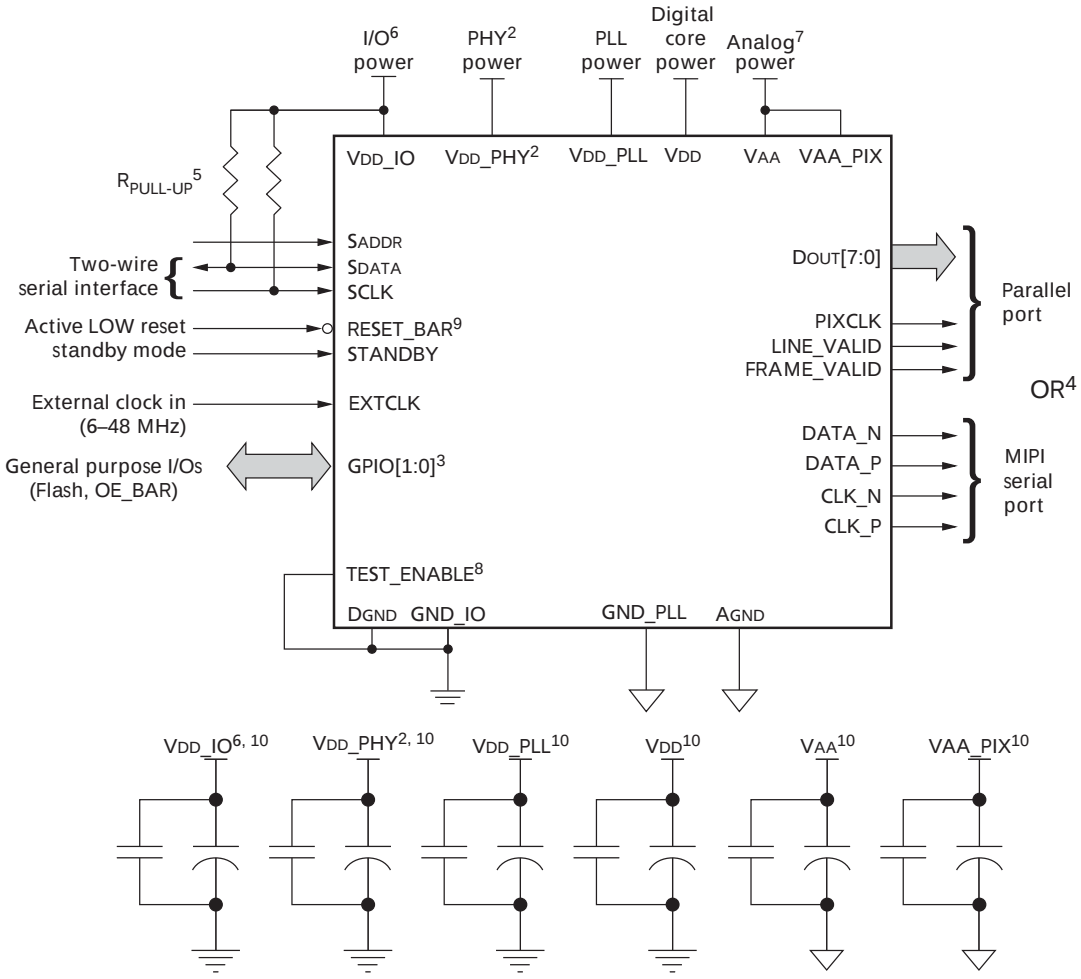
# Typical Connection

**Figure 1: Typical Configuration (Connection)**




Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI interface is not required, the following pads must be left floating: DATA_P, DATA_N, CLK_P, and CLK_N. The VDD_PHY pad must always be connected to 1.8V supply.
3. The GPIO pads have multiple features that can be reconfigured. The function and direction will vary by application. No internal pull-up or pull-down resistors are provided for GPIO pins. An external source needs to drive GPIO pins when GPIO pins are configured as inputs.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. Micron recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
6. All inputs must be configured with VDD_IO.
7. VAA and VAA_PIX must be tied together.
8. TEST_ENABLE has an internal pull-down resistor.
9. RESET_BAR has an internal pull-up resistor.
10. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and numbers may vary depending on layout and design considerations.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# Bond Pad Location and Identification Tables

**Table 1: Bond Pad Location From Center of Pad 1**

| Pad | Pad Name | "X"[1] Microns | "Y"[1] Microns | "X"[1] Inches | "Y"[1] Inches |
|---|---|---|---|---|---|
| 1 | GND_PLL | 0.00 | 0.00 | 0.0000000 | 0.0000000 |
| 2 | VDD_PLL | 141.10 | 0.00 | 0.0055551 | 0.0000000 |
| 3 | DATA_P | 369.20 | 0.00 | 0.0145354 | 0.0000000 |
| 4 | DATA_N | 599.20 | 0.00 | 0.0235906 | 0.0000000 |
| 5 | CLK_P | 829.21 | 0.00 | 0.0326459 | 0.0000000 |
| 6 | CLK_N | 1059.21 | 0.00 | 0.0417010 | 0.0000000 |
| 7 | VDD_PHY | 1320.82 | 0.00 | 0.0520008 | 0.0000000 |
| 8 | VDD1 | 1461.92 | 0.00 | 0.0575559 | 0.0000000 |
| 9 | DGND1 | 1603.02 | 0.00 | 0.0631110 | 0.0000000 |
| 10 | EXTCLK | 1744.12 | 0.00 | 0.0686661 | 0.0000000 |
| 11 | VDD_IO1 | 1885.82 | 0.00 | 0.0742449 | 0.0000000 |
| 12 | DOUT0 | 2026.35 | 0.00 | 0.0797774 | 0.0000000 |
| 13 | GND_IO1 | 2169.45 | 0.00 | 0.0854114 | 0.0000000 |
| 14 | DOUT1 | 2316.37 | 0.00 | 0.0911955 | 0.0000000 |
| 15 | DGND2 | 2459.46 | 0.00 | 0.0968291 | 0.0000000 |
| 16 | VDD2 | 2594.76 | 0.00 | 0.1021559 | 0.0000000 |
| 17 | VDD_IO2 | 2735.83 | 0.00 | 0.1077098 | 0.0000000 |
| 18 | GND_IO2 | 3003.21 | –230.83 | 0.1182366 | –0.0090878 |
| 19 | DOUT2 | 3003.21 | –400.84 | 0.1182366 | –0.0157809 |
| 20 | DOUT3 | 3003.21 | –574.26 | 0.1182366 | –0.0226085 |
| 21 | DOUT4 | 3003.21 | –747.68 | 0.1182366 | –0.0294360 |
| 22 | VAA_PIX | 3003.21 | –982.39 | 0.1182366 | –0.0386768 |
| 23 | VAA | 3003.21 | –1092.59 | 0.1182366 | –0.0430154 |
| 24 | DNU[2] | 3003.21 | –1202.79 | 0.1182366 | –0.0473539 |
| 25 | DNU | 3003.21 | –1312.99 | 0.1182366 | –0.0516925 |
| 26 | AGND | 3003.21 | –1423.19 | 0.1182366 | –0.0560311 |
| 27 | TEST_EN[3] | 3003.21 | –2691.92 | 0.1182366 | –0.1059811 |
| 28 | RESET_BAR | 3003.21 | –2841.56 | 0.1182366 | –0.1118724 |
| 29 | SCLK | 3003.21 | –2991.20 | 0.1182366 | –0.1177638 |
| 30 | STANDBY | 3003.21 | –3140.84 | 0.1182366 | –0.1236551 |
| 31 | GND_IO4 | 3003.21 | –3285.77 | 0.1182366 | –0.1293610 |
| 32 | VDD4 | 2735.76 | –3516.60 | 0.1077071 | –0.1384488 |
| 33 | DGND4 | 2560.95 | –3516.60 | 0.1008248 | –0.1384488 |
| 34 | SDATA | 2386.14 | –3516.60 | 0.0939425 | –0.1384488 |
| 35 | GPIO_1 | 2205.02 | –3516.60 | 0.0868116 | –0.1384488 |
| 36 | PIXCLK | 2031.60 | –3516.60 | 0.0799841 | –0.1384488 |
| 37 | SADDR | 1855.40 | –3516.60 | 0.0730472 | –0.1384488 |
| 38 | GPIO_0 | 1680.59 | –3516.60 | 0.0661648 | –0.1384488 |
| 39 | VDD_IO4 | 1505.78 | –3516.60 | 0.0592827 | –0.1384488 |
| 40 | GND_IO3 | 1192.57 | –3516.60 | 0.0469516 | –0.1384488 |
| 41 | FRAME_VALID | 1017.76 | –3516.60 | 0.0400691 | –0.1384488 |
| 42 | LINE_VALID | 844.34 | –3516.60 | 0.0332415 | –0.1384488 |
| 43 | DGND3 | 668.14 | –3516.60 | 0.0263047 | –0.1384488 |



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**Table 1: Bond Pad Location From Center of Pad 1 (continued)**

| Pad | Pad Name | "X"[1] Microns | "Y"[1] Microns | "X"[1] Inches | "Y"[1] Inches |
|---|---|---|---|---|---|
| 44 | DOUT7 | 493.33 | –3516.60 | 0.0194222 | –0.1384488 |
| 45 | VDD3 | 318.52 | –3516.60 | 0.0125402 | –0.1384488 |
| 46 | DOUT6 | 143.71 | –3516.60 | 0.0056577 | –0.1384488 |
| 47 | DOUT5 | –29.72 | –3516.60 | –0.0011699 | –0.1384488 |
| 48 | VDD_IO3 | –205.91 | –3516.60 | –0.0081067 | –0.1384488 |

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = "do not use."
3. Connect to DGND or leave floating for normal operation.
4. To ensure proper device operation, all power supply bond pads must be bonded.



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**Table 2: Bond Pad Location From Center of Die (0, 0)**

| Pad | Pad Name | "X"[1] Microns | "Y"[1] Microns | "X"[1] Inches | "Y"[1] Inches |
|---|---|---|---|---|---|
| 1 | GND_PLL | –1367.91 | 1758.30 | –0.0538547 | 0.0692244 |
| 2 | VDD_PLL | –1226.81 | 1758.30 | –0.0482996 | 0.0692244 |
| 3 | DATA_P | –998.71 | 1758.30 | –0.0393193 | 0.0692244 |
| 4 | DATA_N | –768.71 | 1758.30 | –0.0302642 | 0.0692244 |
| 5 | CLK_P | –538.71 | 1758.30 | –0.0212089 | 0.0692244 |
| 6 | CLK_N | –308.71 | 1758.30 | –0.0121537 | 0.0692244 |
| 7 | VDD_PHY | –47.09 | 1758.30 | –0.0018539 | 0.0692244 |
| 8 | VDD1 | 94.01 | 1758.30 | 0.0037012 | 0.0692244 |
| 9 | DGND1 | 235.11 | 1758.30 | 0.0092563 | 0.0692244 |
| 10 | EXTCLK | 376.21 | 1758.30 | 0.0148114 | 0.0692244 |
| 11 | VDD_IO1 | 517.91 | 1758.30 | 0.0203902 | 0.0692244 |
| 12 | DOUT0 | 658.44 | 1758.30 | 0.0259226 | 0.0692244 |
| 13 | GND_IO1 | 801.54 | 1758.30 | 0.0315567 | 0.0692244 |
| 14 | DOUT1 | 948.46 | 1758.30 | 0.0373407 | 0.0692244 |
| 15 | DGND2 | 1091.55 | 1758.30 | 0.0429744 | 0.0692244 |
| 16 | VDD2 | 1226.85 | 1758.30 | 0.0483012 | 0.0692244 |
| 17 | VDD_IO2 | 1367.92 | 1758.30 | 0.0538551 | 0.0692244 |
| 18 | GND_IO2 | 1635.30 | 1527.47 | 0.0643819 | 0.0601366 |
| 19 | DOUT2 | 1635.30 | 1357.47 | 0.0643819 | 0.0534435 |
| 20 | DOUT3 | 1635.30 | 1184.05 | 0.0643819 | 0.0466159 |
| 21 | DOUT4 | 1635.30 | 1010.63 | 0.0643819 | 0.0397884 |
| 22 | VAA_PIX | 1635.30 | 775.91 | 0.0643819 | 0.0305476 |
| 23 | VAA | 1635.30 | 665.71 | 0.0643819 | 0.0262091 |
| 24 | DNU[2] | 1635.30 | 555.51 | 0.0643819 | 0.0218705 |
| 25 | DNU | 1635.30 | 445.31 | 0.0643819 | 0.0175319 |
| 26 | AGND | 1635.30 | 335.11 | 0.0643819 | 0.0131933 |
| 27 | TEST_EN[3] | 1635.30 | –933.62 | 0.0643819 | –0.0367567 |
| 28 | RESET_BAR | 1635.30 | –1083.26 | 0.0643819 | –0.0426480 |
| 29 | SCLK | 1635.30 | –1232.90 | 0.0643819 | –0.0485394 |
| 30 | STANDBY | 1635.30 | –1382.54 | 0.0643819 | –0.0544307 |
| 31 | GND_IO4 | 1635.30 | –1527.47 | 0.0643819 | –0.0601366 |
| 32 | VDD4 | 1367.85 | –1758.30 | 0.0538524 | –0.0692244 |
| 33 | DGND4 | 1193.04 | –1758.30 | 0.0469701 | –0.0692244 |
| 34 | SDATA | 1018.23 | –1758.30 | 0.0400878 | –0.0692244 |
| 35 | GPIO_1 | 837.11 | –1758.30 | 0.0329569 | –0.0692244 |
| 36 | PIXCLK | 663.69 | –1758.30 | 0.0261293 | –0.0692244 |
| 37 | SADDR | 487.49 | –1758.30 | 0.0191925 | –0.0692244 |
| 38 | GPIO_0 | 312.68 | –1758.30 | 0.0123100 | –0.0692244 |
| 39 | VDD_IO4 | 137.87 | –1758.30 | 0.0054280 | –0.0692244 |
| 40 | GND_IO3 | –175.34 | –1758.30 | –0.0069031 | –0.0692244 |
| 41 | FRAME_VALID | –350.16 | –1758.30 | –0.0137856 | –0.0692244 |
| 42 | LINE_VALID | –523.58 | –1758.30 | –0.0206132 | –0.0692244 |



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**Table 2: Bond Pad Location From Center of Die (0, 0) (continued)**

| Pad | Pad Name | "X"[1] Microns | "Y"[1] Microns | "X"[1] Inches | "Y"[1] Inches |
|---|---|---|---|---|---|
| 43 | DGND3 | –699.77 | –1758.30 | –0.0275500 | –0.0692244 |
| 44 | DOUT7 | –874.59 | –1758.30 | –0.0344325 | –0.0692244 |
| 45 | VDD3 | –1049.39 | –1758.30 | –0.0413146 | –0.0692244 |
| 46 | DOUT6 | –1224.21 | –1758.30 | –0.0481970 | –0.0692244 |
| 47 | DOUT5 | –1397.63 | –1758.30 | –0.0550246 | –0.0692244 |
| 48 | VDD_IO3 | –1573.82 | –1758.30 | –0.0619614 | –0.0692244 |

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = "do not use."
3. Connect to DGND or leave floating for normal operation.
4. To ensure proper device operation, all power supply bond pads must be bonded.



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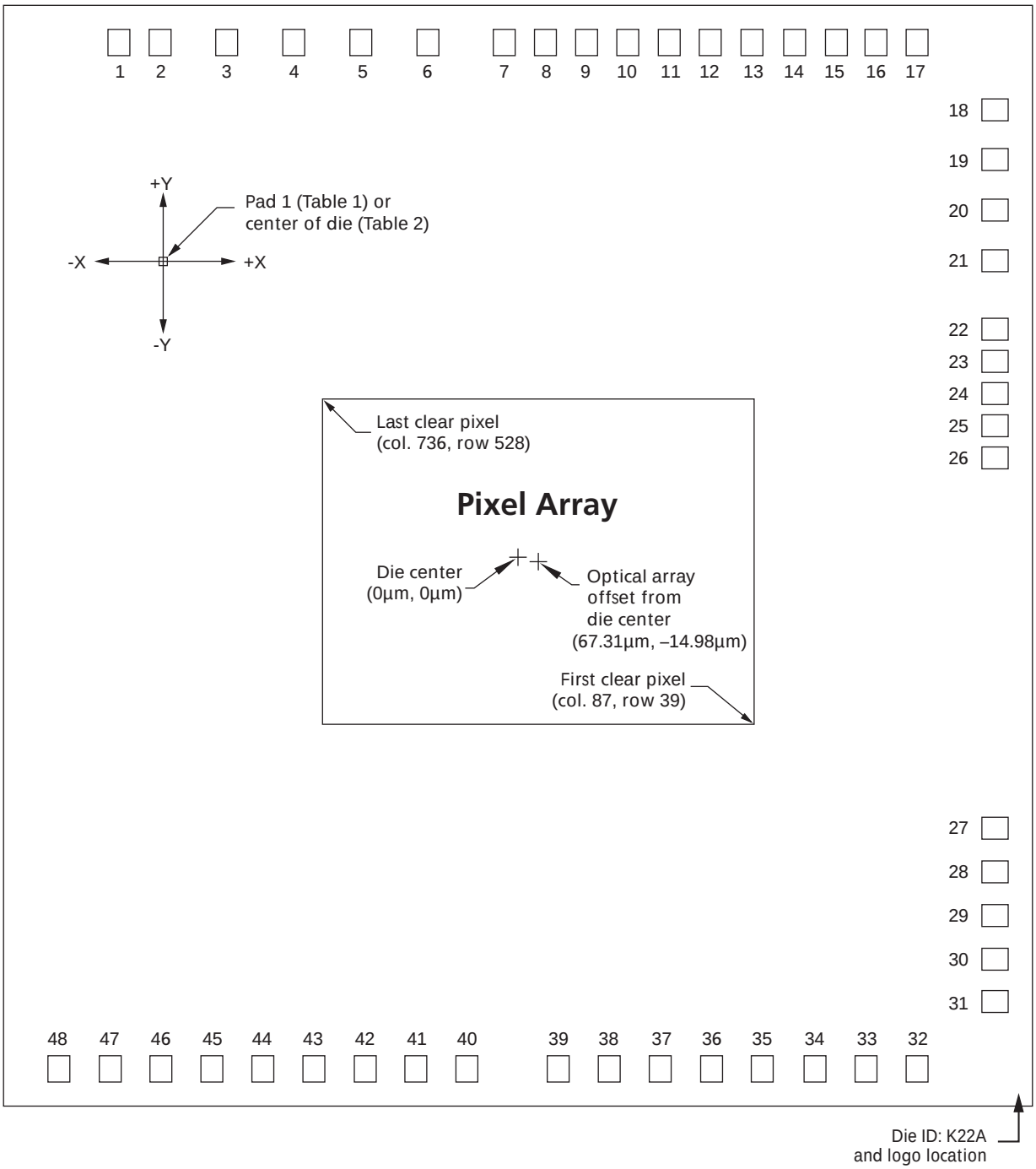
# Die Features

**Figure 2: Die Outline (Top View)**



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# Physical Specifications

**Table 3: Physical Dimensions**

| Feature | Dimensions |
|---|---|
| Wafer diameter | 200mm (8in) |
| Die thickness | 200µm ±12µm |
| Singulated die size<br>*Width:*<br>*Length:* | <br>3,485µm ±25µm<br>3,729µm ±25µm |
| Bond pad size (MIN) | 85µm x 100µm |
| Passivation openings (MIN) | 75µm x 90µm |
| Minimum bond pad pitch | 110.2µm |
| Optical array<br>*Optical center from die center:*<br>*Optical center from center of pad 1:* | <br>X = 67.31µm, Y = –14.98µm<br>X = 1,435.22µm, Y = –1,773.28µm |
| First clear pixel (col. 87, row 39)<br>*From die center:*<br>*From center of pad 1:* | <br>X = 781.28µm, Y = –552.87µm<br>X = 2,149.19µm, Y = –2,311.17µm |
| Last clear pixel (col. 736, row 528)<br>*From die center:*<br>*From center of pad 1:* | <br>X = –646.61µm, Y = 522.99µm<br>X = 721.30µm, Y = –1,235.32µm |



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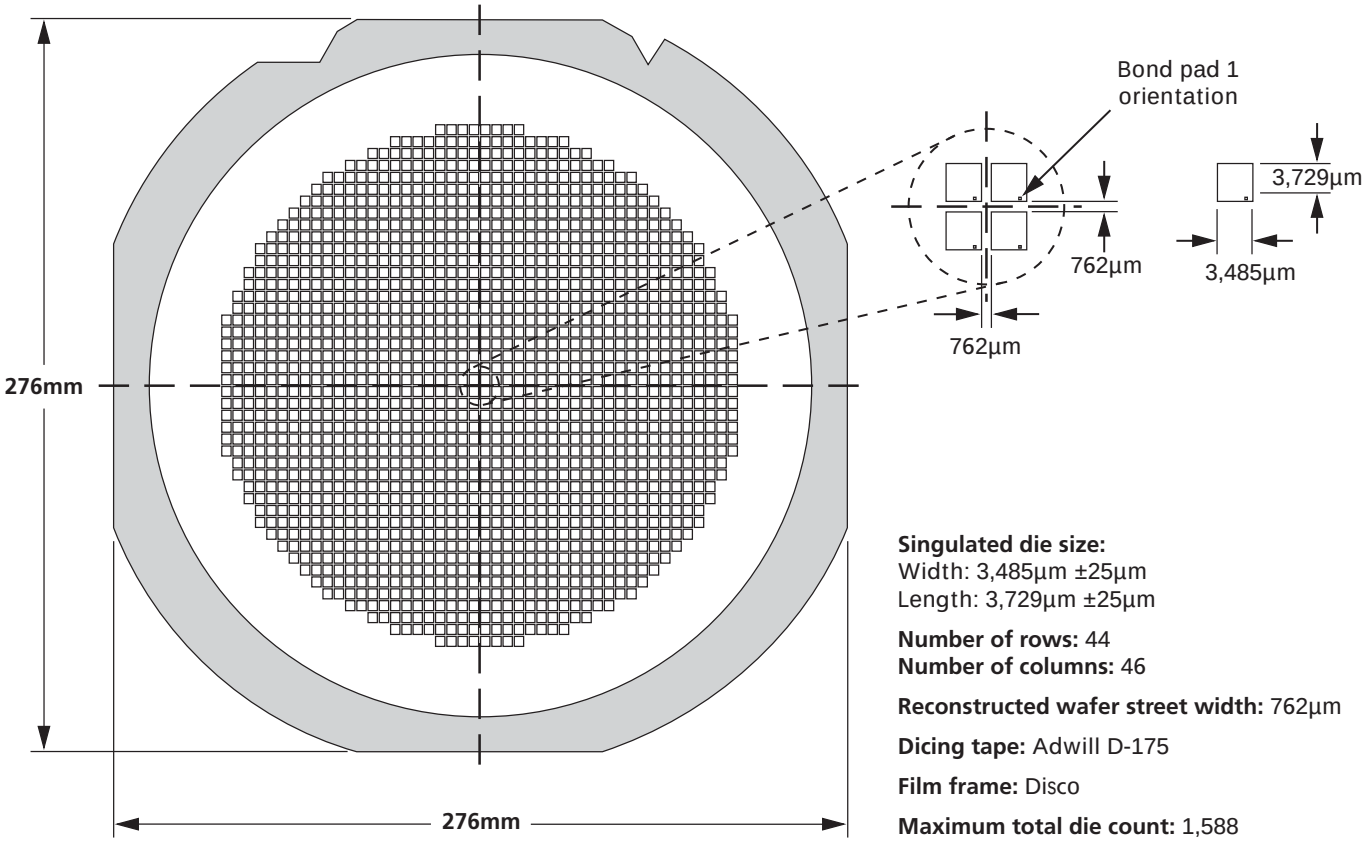
**Figure 3: Die Orientation in Reconstructed Wafer**




**Singulated die size:**
Width: 3,485µm ±25µm
Length: 3,729µm ±25µm

**Number of rows:** 44
**Number of columns:** 46

**Reconstructed wafer street width:** 762µm

**Dicing tape:** Adwill D-175

**Film frame:** Disco

**Maximum total die count:** 1,588

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Advance: This data sheet contains initial descriptions of products still under development.



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# Revision History

**Rev. C, Advance . . . . . 11/07**

- Changed dynamic range from 70 to 63.5dB.
- Changed responsivity from 1.4 to 1.15 V/lux-sec.
- Changed CRA from 25.48° MAX at 90% image height to 27.12° MAX at 100% image height.
- Added “Typical metal 1 thickness: 3.1kÅ” on page 1.
- Changed typical metal 2 and typical metal 3 thickness from 3.1kÅ to 3.2kÅ.
- Changed typical metal 4 thickness from 4.15kÅ to 4.0kÅ .
- Changed typical power consumption on page 1 from “80mW at 30 fps, full resolution; 30µW, standby” to “70mW at 30 fps, full resolution; 35µW, standby”
- Updated formats

**Rev. B, Advance . . . . . 3/07**

- Added die ID and logo location to Figure 2 on page 9
- Corrected die thickness from 305µm to 200µm

**Rev. A, Advance . . . . . 3/07**

- Initial release



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