1/4-Inch System-on-a-Chip (SOC) CMOS Digital Image Sensor Die

MT9T111

For the product data sheets, refer to Micron's Web site: www.micron.com

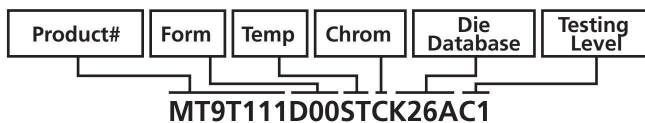
Features

- Micron® DigitalClarity® CMOS imaging technology
- Superior low-light performance
- Ultra low-power, low-cost sensor
- Dual camera bridging support with MT9V013
- Motion adaptive exposure
- One-time programmable (OTP) memory
- Parallel data output and serial mobile industry processor interface (MIPI) data output
- Integrated real-time JPEG encoder
- Flexible support for external auto focus, optical zoom, and mechanical shutter
- Internal master clock generated by on-die phase-lock loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement
- Selectable output data format: YCbCr, 565RGB, 555RGB, 444RGB, JPEG 4:2:2, processed Bayer, RAW8- and RAW10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate
- Xenon and LED flash support with fast exposure adaptation
- Configurable gamma correction based on scene brightness
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory

Ordering Information

MT9T111D00STCK26AC1

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.



Die Database K26A

- Die outline, see Figure 2 on page 13
- Singulated die size (nominal dimension): 6,975µm ±25µm x 6,981µm ±25µm
- Bond Pad Location and Identification Tables, see pages 7–12

Options

- Form
  - Die — D
- Testing
  - Standard (level 1) probe — C1

General Physical Specifications

- Die thickness: 200µm ±12µm
  (Consult factory for other die thickness)
- Backside die surface of bare silicon
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 3.1kÅ
- Typical metal 4 thickness: 4.15kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Key Performance Parameters

- Optical format: 1/4-inch (4:3)
- Full resolution: 2048 x 1536 pixels (QXGA)
- Pixel size: 1.75µm x 1.75µm
- Dynamic range: 67.4dB (preliminary)
- SNR MAX: 38dB (preliminary)
- Responsivity: 0.44 V/lux-sec (preliminary)
- Chief ray angle: 24.99° maximum at 80 percent image height
- Color filter array: RGB Bayer pattern

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Key Performance Parameters (continued)

- Active pixel array area: 3.62mm x 2.72mm, 4.53mm diagonal
- Shutter type: electronic rolling shutter (ERS)
- Input clock frequency: 6–54 MHz
- Maximum frame rate: 15 fps at full resolution (JPEG), 30 fps in preview mode
- Maximum pixel data output: 48Mp/s
- Maximum pixel clock frequency: 96 MHz
- Supply voltage
  - Analog: 2.5–3.1V
  - Digital: 1.7–1.95V
  - I/O: 1.7–3.1V
  - PLL: 2.5–3.1V
  - MIPI: 1.7–1.95V
- ADC resolution: 10-bit, on-die
- Power consumption
  - TBD at 15 fps, full resolution
  - TBD at 30 fps, preview mode
  - 20µA, standby at +70°C
- Operating temperature: –30°C to +70°C (at junction)

General Description

The MT9T111 has a color image sensor with a Bayer color filter arrangement and a 3.1Mp active-pixel array with electronic rolling shutter (ERS). The sensor core readout is 10-bit, supports skipping and binning, and can be flipped and/or mirrored. The sensor core also supports separate analog and digital gain for all four color channels (R, Gr, Gb, and B).

The MT9T111 also has an embedded phase-lock loop (PLL) oscillator that can generate the internal sensor clock from the common clock signals available in typical mobile phone systems. When in use, the PLL adjusts the incoming clock frequency up, allowing the MT9T111 to run at almost any desired resolution and frame rate within the sensor's capabilities. The PLL can be bypassed and powered down to reduce power consumption.

The MT9T111 has numerous power-conserving features including soft standby mode and hard standby mode. The soft standby mode consumes less power than normal operation while retaining the internal registers and variables states. The hard standby mode allows the internal power bus to be disabled.

The MT9T111 can be used with either a serial MIPI interface or the parallel data output interface, which has a programmable I/O slew rate to minimize EMI and an output FIFO to eliminate output data bursts. JPEG format can be outputted in both the MIPI and the parallel data output interfaces. In addition to the MIPI output interface, the MT9T111 also contains a MIPI input interface to enable dual camera configuration with the MT9V013. This allows the MT9V013 to use the image pipeline of the MT9T111 for processing.

The advanced image flow processor (IFP) and flexible programmability of the MT9T111 provide a variety of ways to enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9T111 to operate at factory settings as a fully automatic, highly adaptable camera; however, most of its settings are user-programmable.

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These algorithms include black level conditioning, shading correction, defect correction, noise reduction, color interpolation, color correction, aperture correction, and image formatting such as cropping and scaling.

The MT9T111 also includes a sequencer that coordinates all events triggered by the user. The sequencer manages auto focus, auto white balance, flicker detection, motion adaptive exposure and auto exposure for the different operating modes, which include preview, still capture, video, and snapshot with flash.

All modes of operation are individually configurable and are organized as two contexts. A context is defined by sensor image size, frame rate, resolution, and other associated parameters. The user can switch between the two contexts by sending a command through the two-wire serial interface.

A two wire serial register interface bus enables read/write access to control registers, variables, and special function registers within the MT9T111. The hardware registers include sensor core controls, color pipeline controls, and output controls.

The general purpose I/Os can be configured to allow extended platform functionality or to achieve a 10-bit parallel output.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Micron's characterization package. Because the package environment is not within Micron's control, the user must determine the necessary heat-sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9T111 die has 85 bond pads. Refer to Tables 1 and 2 on pages 7–12 for a complete list of bond pads and coordinates.

The MT9T111 die does not require the user to determine bond option features. The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

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All DGND pads must be tied together, as must all AGND pads, all GND_IO pads, all VDD pads, all VDD_IO pads, all VAA pads, and all VAA_PIX pads.

Storage Requirements

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Typical Connections

Figure 1 on page 5 shows typical MT9T111 device connections. For low-noise operation, the MT9T111 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9T111 also supports different digital core power (VDD/DGND), MIPI output power (VDDIO_TX/GNDIO_TX), MIPI input power VDD IO_ RX/GNDIO_RX), and I/O power (VDD_IO/GND_IO) power domains that can be at different voltages. The PLL requires a clean power source (VDD_PLL).

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Figure 1: Typical Configuration (Connection)

I/O power
MIPI power RX
MIPI power TX
PLL power
Digital core power
Analog power
RPULL-UP[5]
VDD_IO
VDD_VGPIO[9]
VDDIO_RX
VDDIO_TX[2]
VDD_PLL
VDD
VAA[6]
VAA_PIX[6]
Slave two-wire serial interface
SDATA
SCLK
SADDR
DOUT[7:0]
To parallel camera port
Active LOW reset
RESET_BAR
Standby mode
STANDBY
External clock in (6–54 MHz)
EXTCLK
PIXCLK
LINE_VALID
FRAME_VALID
OR[4]
General purpose I/Os (FLASH, OE_BAR, DOUT_LSB[1:0])
GPI0[3:0][3]
DOUT_N
DOUT_P
CLK_N
CLK_P
To serial camera port
VPP[7]
AF control I/Os
VGPI0[7:0][9]
SDATA_2
SCLK_2
EXTCLK_OUT[8]
RESET_BAR_OUT[8]
STANDBY_OUT[8]
RX_DP[8]
RX_DN[8]
RX_CP[8]
RX_CN[8]
DGND
GND_IO
GNDIO_RX
GNDIO_TX[2]
GND_VGPIO[9]
AGND
VDD_IO[10]
VDDIO_RX[10]
VDDIO_TX[2, 10]
VDD_PLL[10]
VDD[10]
VAA[10]
VAA_PIX[10]

Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI Interface is not required, the following pads must be left floating: DOUT_P, DOUT_N, CLK_P, CLK_N, VDDIO_TX, and GNDIO_TX.
3. The GPIO pads can serve multiple features that can be reconfigured. The function and direction will vary by applications.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. A 1.5kΩ resistor value is recommended for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.

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6. V_{AA} and VAA_PIX must be tied together.
7. V_{PP} is the one-time programmable memory (OTPM) signal and should be left floating during normal operation.
8. If the bridging function to the MT9V013 is not required, the following signals can be left floating: EXTCLK_OUT, RESET_BAR_OUT, STANDBY_OUT, RX_DP, RX_DN, RX_CP, and RX_CN.
9. If auto focus is not required the following pads can be floating: V_{DD}_VGPIO, GND_VGPIO and VGPIO[7:0].
10. It is recommended that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

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Bond Pad Location and Identification Tables

Table 1: MT9T111 Bond Pad Location From Center of Pad 1

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND1	0.00	0.00	0.0000000	0.0000000
2	DGND4	6766.60	0.00	0.2664016	0.0000000
3	RESET_BAR_OUT	6766.60	–150.00	0.2664016	–0.0059055
4	STANDBY_OUT	6766.60	–323.42	0.2664016	–0.0127331
5	VDD3	6766.60	–473.42	0.2664016	–0.0186386
6	VDD_IO5	6766.60	–766.27	0.2664016	–0.0301679
7	SDATA_2	6766.60	–928.67	0.2664016	–0.0365616
8	GND_IO5	6766.60	–1079.47	0.2664016	–0.0424986
9	SCLK_2	6766.60	–1230.27	0.2664016	–0.0484356
10	EXTCLK_OUT	6766.60	–1411.39	0.2664016	–0.0555665
11	GPIO3	6766.60	–1584.81	0.2664016	–0.0623941
12	GPIO2	6766.60	–1758.23	0.2664016	–0.0692217
13	VDD_IO6	6766.60	–1912.93	0.2664016	–0.0753120
14	GPIO1	6766.60	–2065.05	0.2664016	–0.0813012
15	GPIO0	6766.60	–2238.47	0.2664016	–0.0881287
16	GND_IO6	6766.60	–2393.17	0.2664016	–0.0942191
17	VAA4	6766.60	–2542.97	0.2664016	–0.1001169
18	VAA3	6766.60	–2692.80	0.2664016	–0.1060157
19	AGND5	6766.60	–2842.73	0.2664016	–0.1119183
20	DNU[2]	6766.60	–2952.93	0.2664016	–0.1162569
21	AGND4	6766.60	–3063.13	0.2664016	–0.1205955
22	DNU	6766.60	–3173.33	0.2664016	–0.1249341
23	AGND3	6766.60	–3283.53	0.2664016	–0.1292726
24	VAA_PIX2	6766.60	–3433.56	0.2664016	–0.1351795
25	VAA_PIX1	6766.60	–3583.52	0.2664016	–0.1410833
26	VPP	6766.60	–3753.46	0.2664016	–0.1477738
27	AGND2	6766.60	–3911.80	0.2664016	–0.1540077
28	DNU	6766.60	–4022.00	0.2664016	–0.1583463
29	AGND1	6766.60	–4132.20	0.2664016	–0.1626848
30	VAA2	6766.60	–4295.42	0.2664016	–0.1691110
31	VAA1	6766.60	–4445.43	0.2664016	–0.1750167
32	SADDR	6766.60	–4655.10	0.2664016	–0.1832717
33	SCLK	6766.60	–5007.74	0.2664016	–0.1971551
34	VDD_IO4	6766.60	–5160.86	0.2664016	–0.2031835
35	SDATA	6766.60	–5311.66	0.2664016	–0.2091205
36	GND_IO4	6766.60	–5462.46	0.2664016	–0.2150575
37	VDD4	6766.60	–5820.27	0.2664016	–0.2291443

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Table 1: MT9T111 Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
38	EXTCLK	6766.60	–5970.27	0.2664016	–0.2350498
39	STANDBY	6766.60	–6119.91	0.2664016	–0.2409411
40	RESET_BAR	6766.60	–6269.55	0.2664016	–0.2468325
41	DGND3	6766.60	–6513.16	0.2664016	–0.2564236
42	VGPIO0	6248.50	–6670.33	0.2460037	–0.2626114
43	VGPIO1	6075.08	–6670.33	0.2391762	–0.2626114
44	GND_VGPIO1	5922.51	–6670.33	0.2331695	–0.2626114
45	VGPIO2	5772.39	–6670.33	0.2272593	–0.2626114
46	VDD_VGPIO1	5619.00	–6670.33	0.2212205	–0.2626114
47	VGPIO3	5468.93	–6670.33	0.2153120	–0.2626114
48	VGPIO4	5295.51	–6670.33	0.2084844	–0.2626114
49	VGPIO5	5122.09	–6670.33	0.2016569	–0.2626114
50	VGPIO6	4948.67	–6670.33	0.1948293	–0.2626114
51	VGPIO7	4775.25	–6670.33	0.1880018	–0.2626114
52	DGND2	0.00	–6513.16	0.0000000	–0.2564236
53	VDD_PLL	0.00	–6363.17	0.0000000	–0.2505183
54	DOUT_P	0.00	–6135.07	0.0000000	–0.2415380
55	DOUT_N	0.00	–5905.07	0.0000000	–0.2324829
56	CLK_P	0.00	–5675.06	0.0000000	–0.2234276
57	CLK_N	0.00	–5445.06	0.0000000	–0.2143724
58	VDDIO_TX	0.00	–5183.45	0.0000000	–0.2040726
59	GNDIO_TX	0.00	–5033.24	0.0000000	–0.1981591
60	RX_DN	0.00	–4858.54	0.0000000	–0.1912809
61	RX_DP	0.00	–4601.26	0.0000000	–0.1811518
62	RX_CN	0.00	–4342.98	0.0000000	–0.1709835
63	RX_CP	0.00	–4085.70	0.0000000	–0.1608543
64	VDDIO_RX	0.00	–3846.56	0.0000000	–0.1514394
65	GNDIO_RX	0.00	–3696.46	0.0000000	–0.1455299
66	VDD2	0.00	–3546.47	0.0000000	–0.1396248
67	FRAME_VALID	0.00	–3232.33	0.0000000	–0.1272571
68	LINE_VALID	0.00	–3061.48	0.0000000	–0.1205307
69	VDD_IO3	0.00	–2911.45	0.0000000	–0.1146240
70	PIXCLK	0.00	–2761.45	0.0000000	–0.1087185
71	GND_IO3	0.00	–2548.76	0.0000000	–0.1003449
72	DOUT7	0.00	–2385.04	0.0000000	–0.0938990
73	DOUT6	0.00	–2211.62	0.0000000	–0.0870715
74	VDD_IO2	0.00	–2058.39	0.0000000	–0.0810390
75	DNU	0.00	–1928.47	0.0000000	–0.0759240

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Table 1: MT9T111 Bond Pad Location From Center of Pad 1 (continued)

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
76	GND_IO2	0.00	–1775.35	0.0000000	–0.0698957
77	DOUT5	0.00	–1625.35	0.0000000	–0.0639902
78	DOUT4	0.00	–1451.93	0.0000000	–0.0571626
79	VDD1	0.00	–1137.79	0.0000000	–0.0447949
80	DOUT3	0.00	–973.02	0.0000000	–0.0383079
81	DOUT2	0.00	–799.60	0.0000000	–0.0314803
82	VDD_IO1	0.00	–649.57	0.0000000	–0.0255736
83	GND_IO1	0.00	–489.75	0.0000000	–0.0192813
84	DOUT1	0.00	–339.73	0.0000000	–0.0133750
85	DOUT0	0.00	–166.31	0.0000000	–0.0065474

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

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Table 2: MT9T111 Bond Pad Location From Center of Die (0, 0)

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND1	–3383.30	3287.03	–0.1332008	0.1294106
2	DGND4	3383.30	3287.03	0.1332008	0.1294106
3	RESET_BAR_OUT	3383.30	3137.03	0.1332008	0.1235051
4	STANDBY_OUT	3383.30	2963.61	0.1332008	0.1166776
5	VDD3	3383.30	2813.61	0.1332008	0.1107720
6	VDD_IO5	3383.30	2520.77	0.1332008	0.0992427
7	SDATA_2	3383.30	2358.37	0.1332008	0.0928490
8	GND_IO5	3383.30	2207.57	0.1332008	0.0869120
9	SCLK_2	3383.30	2056.77	0.1332008	0.0809750
10	EXTCLK_OUT	3383.30	1875.64	0.1332008	0.0738441
11	GPIO3	3383.30	1702.22	0.1332008	0.0670165
12	GPIO2	3383.30	1528.80	0.1332008	0.0601890
13	VDD_IO6	3383.30	1374.11	0.1332008	0.0540986
14	GPIO1	3383.30	1221.98	0.1332008	0.0481094
15	GPIO0	3383.30	1048.56	0.1332008	0.0412819
16	GND_IO6	3383.30	893.87	0.1332008	0.0351915
17	VAA4	3383.30	744.06	0.1332008	0.0292937
18	VAA3	3383.30	594.23	0.1332008	0.0233949
19	AGND5	3383.30	444.31	0.1332008	0.0174923
20	DNU[2]	3383.30	334.11	0.1332008	0.0131537
21	AGND4	3383.30	223.91	0.1332008	0.0088152
22	DNU	3383.30	113.71	0.1332008	0.0044766
23	AGND3	3383.30	3.51	0.1332008	0.0001380
24	VAA_PIX2	3383.30	–146.53	0.1332008	–0.0057689
25	VAA_PIX1	3383.30	–296.49	0.1332008	–0.0116726
26	VPP	3383.30	–466.43	0.1332008	–0.0183632
27	AGND2	3383.30	–624.77	0.1332008	–0.0245970
28	DNU	3383.30	–734.97	0.1332008	–0.0289356
29	AGND1	3383.30	–845.17	0.1332008	–0.0332742
30	VAA2	3383.30	–1008.39	0.1332008	–0.0397004
31	VAA1	3383.30	–1158.40	0.1332008	–0.0456061
32	SADDR	3383.30	–1368.07	0.1332008	–0.0538610
33	SCLK	3383.30	–1720.71	0.1332008	–0.0677445
34	VDD_IO4	3383.30	–1873.83	0.1332008	–0.0737728
35	SDATA	3383.30	–2024.63	0.1332008	–0.0797098
36	GND_IO4	3383.30	–2175.43	0.1332008	–0.0856469
37	VDD4	3383.30	–2533.24	0.1332008	–0.0997337
38	EXTCLK	3383.30	–2683.24	0.1332008	–0.1056392

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Table 2: MT9T111 Bond Pad Location From Center of Die (0, 0) (continued)

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
39	STANDBY	3383.30	–2832.88	0.1332008	–0.1115305
40	RESET_BAR	3383.30	–2982.52	0.1332008	–0.1174219
41	DGND3	3383.30	–3226.13	0.1332008	–0.1270130
42	VGPIO0	2865.20	–3383.30	0.1128030	–0.1332008
43	VGPIO1	2691.78	–3383.30	0.1059754	–0.1332008
44	GND_VGPIO1	2539.21	–3383.30	0.0999687	–0.1332008
45	VGPIO2	2389.09	–3383.30	0.0940585	–0.1332008
46	VDD_VGPIO1	2235.70	–3383.30	0.0880197	–0.1332008
47	VGPIO3	2085.63	–3383.30	0.0821112	–0.1332008
48	VGPIO4	1912.21	–3383.30	0.0752837	–0.1332008
49	VGPIO5	1738.79	–3383.30	0.0684561	–0.1332008
50	VGPIO6	1565.37	–3383.30	0.0616285	–0.1332008
51	VGPIO7	1391.95	–3383.30	0.0548010	–0.1332008
52	DGND2	–3383.30	–3226.13	–0.1332008	–0.1270130
53	VDD_PLL	–3383.30	–3076.14	–0.1332008	–0.1211077
54	DOUT_P	–3383.30	–2848.04	–0.1332008	–0.1121274
55	DOUT_N	–3383.30	–2618.04	–0.1332008	–0.1030722
56	CLK_P	–3383.30	–2388.03	–0.1332008	–0.0940169
57	CLK_N	–3383.30	–2158.03	–0.1332008	–0.0849618
58	VDDIO_TX	–3383.30	–1896.42	–0.1332008	–0.0746620
59	GNDIO_TX	–3383.30	–1746.21	–0.1332008	–0.0687484
60	RX_DN	–3383.30	–1571.51	–0.1332008	–0.0618703
61	RX_DP	–3383.30	–1314.23	–0.1332008	–0.0517411
62	RX_CN	–3383.30	–1055.95	–0.1332008	–0.0415728
63	RX_CP	–3383.30	–798.67	–0.1332008	–0.0314437
64	VDDIO_RX	–3383.30	–559.53	–0.1332008	–0.0220287
65	GNDIO_RX	–3383.30	–409.43	–0.1332008	–0.0161193
66	VDD2	–3383.30	–259.44	–0.1332008	–0.0102142
67	FRAME_VALID	–3383.30	54.70	–0.1332008	0.0021535
68	LINE_VALID	–3383.30	225.55	–0.1332008	0.0088799
69	VDD_IO3	–3383.30	375.58	–0.1332008	0.0147866
70	PIXCLK	–3383.30	525.58	–0.1332008	0.0206921
71	GND_IO3	–3383.30	738.27	–0.1332008	0.0290657
72	DOUT7	–3383.30	902.00	–0.1332008	0.0355116
73	DOUT6	–3383.30	1075.42	–0.1332008	0.0423392
74	VDD_IO2	–3383.30	1228.64	–0.1332008	0.0483717
75	DNU	–3383.30	1358.56	–0.1332008	0.0534866
76	GND_IO2	–3383.30	1511.68	–0.1332008	0.0595150

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Table 2: MT9T111 Bond Pad Location From Center of Die (0, 0) (continued)

Pad	MT9T111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
77	DOUT5	–3383.30	1661.68	–0.1332008	0.0654205
78	DOUT4	–3383.30	1835.10	–0.1332008	0.0722480
79	VDD1	–3383.30	2149.24	–0.1332008	0.0846157
80	DOUT3	–3383.30	2314.01	–0.1332008	0.0911028
81	DOUT2	–3383.30	2487.43	–0.1332008	0.0979303
82	VDD_IO1	–3383.30	2637.46	–0.1332008	0.1038370
83	GND_IO1	–3383.30	2797.29	–0.1332008	0.1101293
84	DOUT1	–3383.30	2947.31	–0.1332008	0.1160356
85	DOUT0	–3383.30	3120.73	–0.1332008	0.1228632

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

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Die Features

Figure 2: Die Outline (Top View)

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+Y
-X
+X
-Y
Pad 1 (Table 1) or center of die (Table 2)

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First clear pixel (col. 100, row 70)

Pixel Array

Die center (0µm, 0µm)

Optical array offset from die center (0µm, –200.00µm)

Last clear pixel (col. 2,191, row 1,649)

51 50 49 48 47 46 45 44 43 42

Die ID: K26A and logo location

Notes: 1. Figure 2 represents physical orientation of the die only. The image projected is flipped horizontally and vertically by the lens.

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Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) *Width (X dimension):* *Length (Y dimension):*	 6,975µm ±25µm 6,981µm ±25µm
Bond pad size (MIN)	100µm x 85µm
Passivation openings (MIN)	90µm x 75µm
Minimum bond pad pitch *Between any two bond pads:*	 150µm
Optical array offset *Optical center from die center:* *Optical center from center of pad 1:*	 X = 0.00µm, Y = –200.00µm X = 3,383.30µm, Y = –3,487.03µm
First clear pixel (col. 100, row 70) *From die center:* *From center of pad 1:*	 X = 1,833.29µm, Y = 1,183.45µm X = 5,216.59µm, Y = –2,103.58µm
Last clear pixel (col. 2,191, row 1,649) *From die center:* *From center of pad 1:*	 X = –1,825.96µm, Y = –1,579.70µm X = 1,557.34µm, Y = –4,866.73µm

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Figure 3: MT9M113 Die Orientation in Reconstructed Wafer

TBD

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992
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Advance: This data sheet contains initial descriptions of products still under development.

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Revision History

Rev. B, Advance 05/07

- Corrected typo, Table 3 on page 14

Rev. A, Advance 05/07

- Initial release

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