1/4-Inch 2Mp CMOS Active-Pixel Digital Image Sensor Die

MT9D014

For the product data sheet, refer to Micron's Web site: www.micron.com

Features

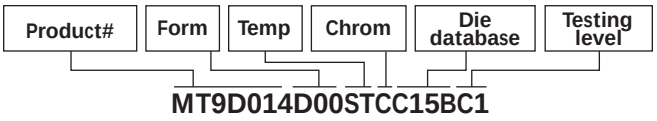
- DigitalClarity® CMOS imaging technology
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size and panning
- Data interface: CCP2 compliant sub-low-voltage differential signaling (sub-LVDS)
- SMIA-compatible
- On-die phase-lock loop (PLL) oscillator
- Bayer-pattern down-size scaler
- Integrated lens shading correction
- Superior low-light performance
- Internal power switch for ultra-low standby current consumption
- 30 fps full resolution

General Physical Specifications

- Die thickness: 200µm ±12µm
  (Consult factory for other die thickness)
- Backside wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

MT9D014D00STC C15BC1



Die Database C15B

- Die outline, see Figure 2 on page 7
- Singulated die size: 5,488µm x 4,799µm
- Bond Pad Location and Identification Tables, see pages 5–6

Option

- Form
  – Die D
- Testing
  – Standard (level 1) probe C1

Notes: 1. Consult die distributor or factory before ordering to verify long-term availability of these die products.

General Description

The Micron® Imaging MT9D014 die is a UXGA-format 1/4-inch CMOS active-pixel digital image sensor, with a pixel array of 1608H x 1208V (1600H x 1200V with a 4-pixel border on each edge). It incorporates sophisticated on-die camera functions such as windowing, mirroring, and column and row skip modes. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9D014 digital image sensor die features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

When operated in its default mode, the sensor generates a UXGA image at 24.04 frames per second (fps). An on-die analog-to-digital converter (ADC) generates a 10-bit value for each pixel. The pixel data is encoded with line and framing information in a high-speed CCP2 differential data stream. The sensor can be programmed by the user to control the frame size, exposure, gain setting, and other parameters.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Micron's standard package. Because the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided here are for reference only. For target functional and parametric specifications, refer to the packaged product data sheet found on Micron's Web site.

Bonding Instructions

The MT9D014 imager die has 29 bond pads. Refer to Table 1 and Table 2 on pages 5–6 for a complete list of bond pads and coordinates.

The MT9D014 imager die does not require the user to determine bond option features.

Figure 1 on page 4 shows the MT9D014 typical die connections. For low-noise operation, the MT9D014 die requires separate supplies for analog and digital power. Power supply rails should be decoupled from ground using capacitors. Use of inductance filters is not recommended.

Storage Requirements

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

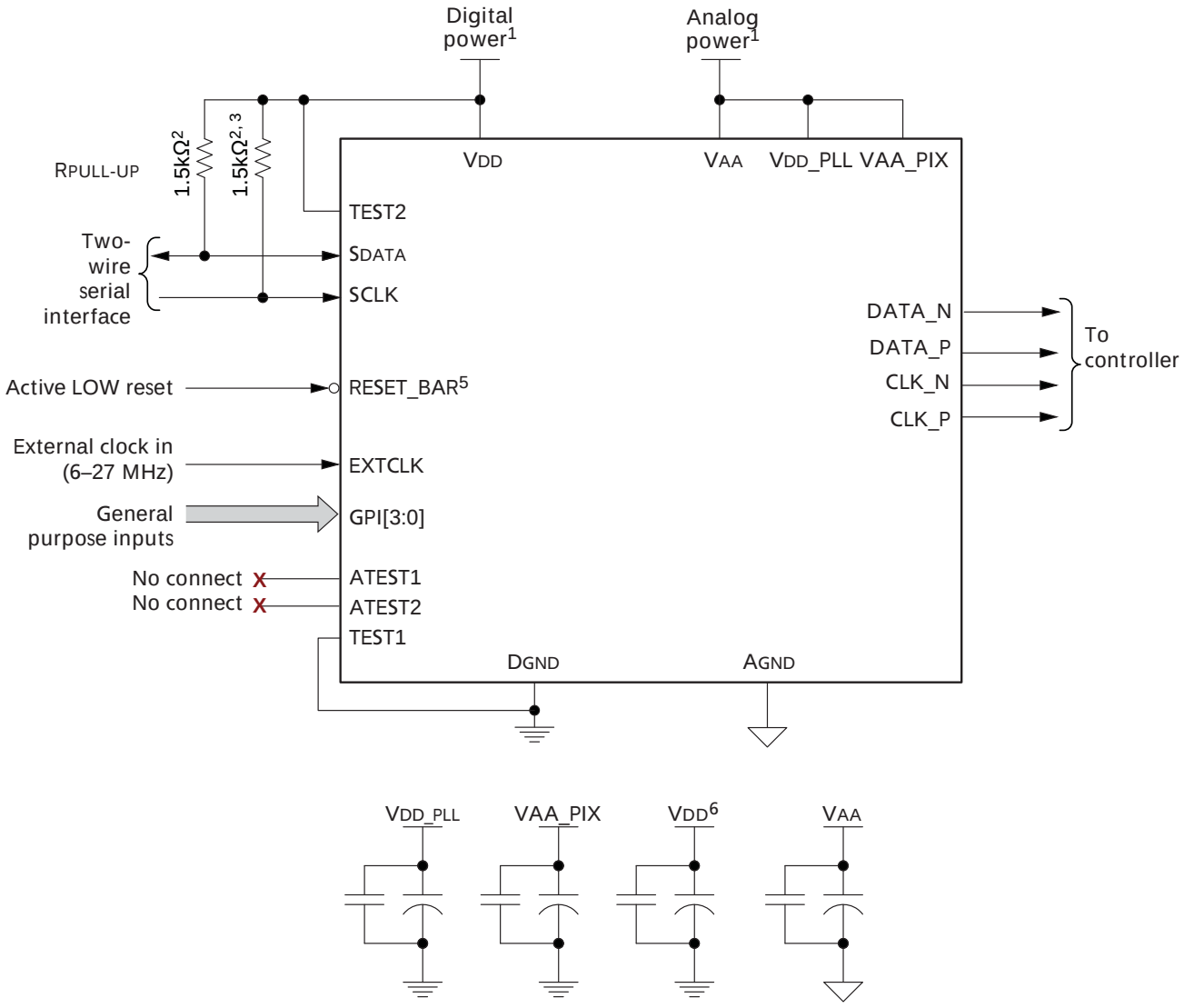
Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the "Accelerated Life" and "Environmental Stress" tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Output Modes

Figure 1 shows typical configuration schematics for the MT9D014 operating in serial mode.

Figure 1: Typical Configuration (Connection) – Serial Output Mode



Notes:
1. All power supplies should be adequately decoupled.
2. A resistor value of 1.5kΩ is recommended, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level at all times.
4. TEST1 must be tied to GND. TEST2 must be tied to VDD.
5. Also referred to as XSHUTDOWN.
6. The GPI pins can be statically pulled HIGH or LOW and used as module IDs, or they can be programmed to perform special functions (SADDR, STANDBY) and be dynamically controlled. After reset, these pads are powered up (enabled). Failure to bond as required will result in excessive power consumption.
7. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Bond Pad Location and Identification Tables

Table 1: MT9D014 Bond Pad Location From Center of Pad 1

Pad	MT9D014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND	0.00	0.00	0.000000	0.000000
2	VDD	377.28	0.00	0.014854	0.000000
3	TEST2	532.28	0.00	0.020956	0.000000
4	RESET_BAR	708.07	0.00	0.027877	0.000000
5	SCLK	877.99	0.00	0.034567	0.000000
6	SDATA	1087.30	0.00	0.042807	0.000000
7	GPI3	1281.19	0.00	0.050441	0.000000
8	GPI2	1451.11	0.00	0.057130	0.000000
9	GPI1	1621.03	0.00	0.063820	0.000000
10	GPI0	1790.95	0.00	0.070510	0.000000
11	TEST1	1960.87	0.00	0.077200	0.000000
12	VAA	3995.23	0.00	0.157293	0.000000
13	VAA	4151.07	0.00	0.163428	0.000000
14	ATEST2	4292.91	0.00	0.169012	0.000000
15	ATEST1	4423.95	0.00	0.174171	0.000000
16	VAA_PIX	4554.99	0.00	0.179330	0.000000
17	VAA_PIX	4709.99	0.00	0.185433	0.000000
18	AGND	4865.12	0.00	0.191540	0.000000
19	AGND	5023.64	0.00	0.197781	0.000000
20	DGND	5023.64	–4516.21	0.197781	–0.177804
21	VDD_PLL	4868.64	–4516.21	0.191679	–0.177804
22	VDD	4506.48	–4516.21	0.177420	–0.177804
23	CLK_N	4288.24	–4516.21	0.168828	–0.177804
24	CLK_P	3998.24	–4516.21	0.157411	–0.177804
25	DATA_N	3631.60	–4516.21	0.142976	–0.177804
26	DATA_P	3341.60	–4516.21	0.131559	–0.177804
27	EXTCLK	3148.00	–4516.21	0.123937	–0.177804
28	DGND	2976.48	–4516.21	0.117184	–0.177804
29	VDD	2601.36	–4516.21	0.102416	–0.177804

Notes: 1. Reference to center of each bond pad from center of bond pad 1.
2. To ensure proper device operation, all power supply bond pads must be bonded.

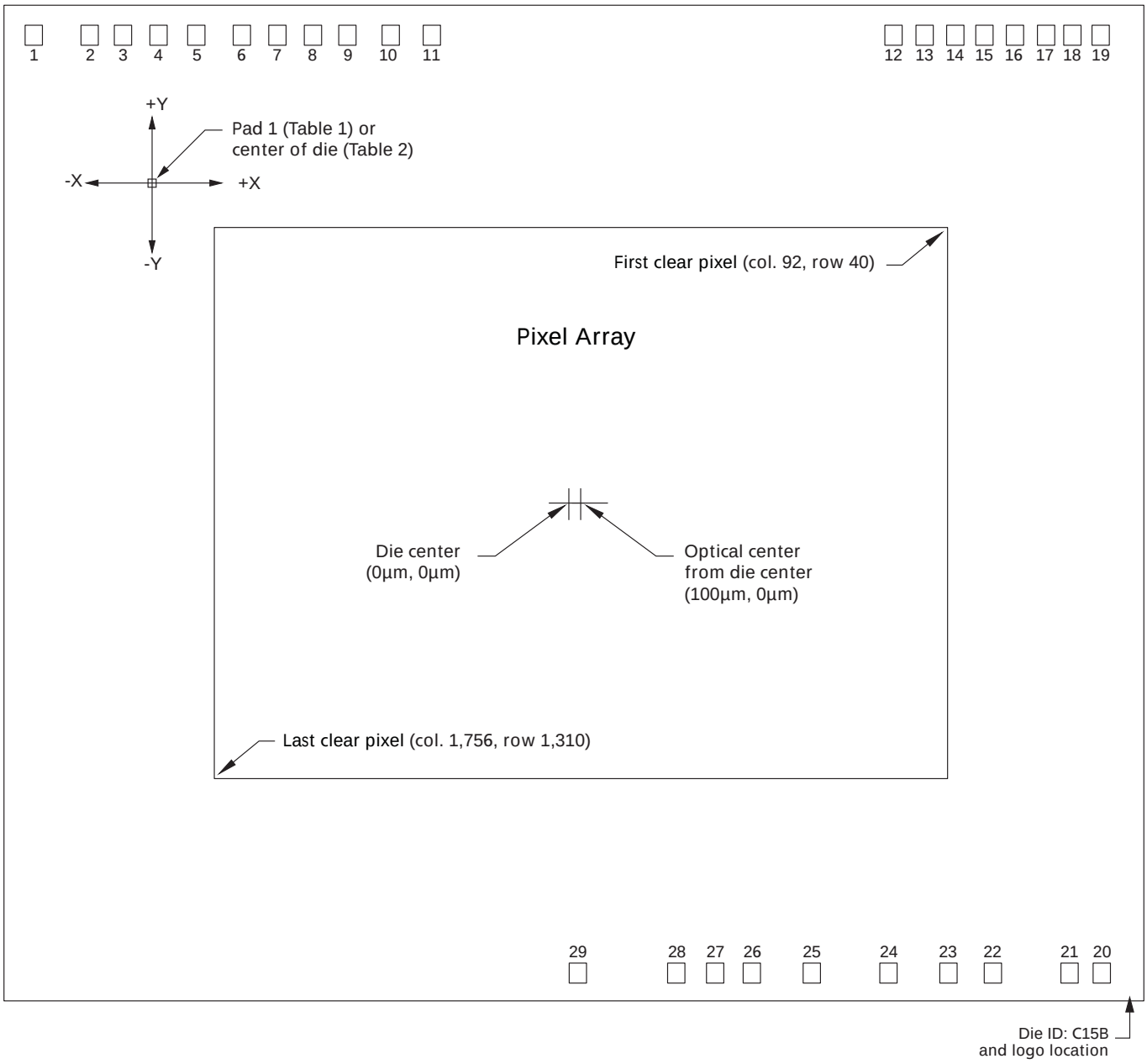
Table 2: MT9D014 Bond Pad Location From Center of Die (0, 0)

Pad	MT9D014	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND	–2511.82	2258.11	–0.098891	0.088902
2	VDD	–2134.54	2258.11	–0.084037	0.088902
3	TEST2	–1979.54	2258.11	–0.077935	0.088902
4	RESET_BAR	–1803.75	2258.11	–0.071014	0.088902
5	SCLK	–1633.83	2258.11	–0.064324	0.088902
6	SDATA	–1424.53	2258.11	–0.056084	0.088902
7	GPI3	–1230.63	2258.11	–0.048450	0.088902
8	GPI2	–1060.71	2258.11	–0.041760	0.088902
9	GPI1	–890.79	2258.11	–0.035070	0.088902
10	GPI0	–720.87	2258.11	–0.028381	0.088902
11	TEST1	–550.95	2258.11	–0.021691	0.088902
12	VAA	1483.41	2258.11	0.058402	0.088902
13	VAA	1639.25	2258.11	0.064537	0.088902
14	ATEST2	1781.09	2258.11	0.070122	0.088902
15	ATEST1	1912.13	2258.11	0.075281	0.088902
16	VAA_PIX	2043.17	2258.11	0.080440	0.088902
17	VAA_PIX	2198.17	2258.11	0.086542	0.088902
18	AGND	2353.30	2258.11	0.092650	0.088902
19	AGND	2511.82	2258.11	0.098891	0.088902
20	DGND	2511.82	–2258.11	0.098891	–0.088902
21	VDD_PLL	2356.82	–2258.11	0.092788	–0.088902
22	VDD	1994.66	–2258.11	0.078530	–0.088902
23	CLK_N	1776.42	–2258.11	0.069938	–0.088902
24	CLK_P	1486.42	–2258.11	0.058520	–0.088902
25	DATA_N	1119.78	–2258.11	0.044086	–0.088902
26	DATA_P	829.78	–2258.11	0.032669	–0.088902
27	EXTCLK	636.18	–2258.11	0.025046	–0.088902
28	DGND	464.66	–2258.11	0.018294	–0.088902
29	VDD	89.54	–2258.11	0.003525	–0.088902

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 2: Die Outline (Top View)

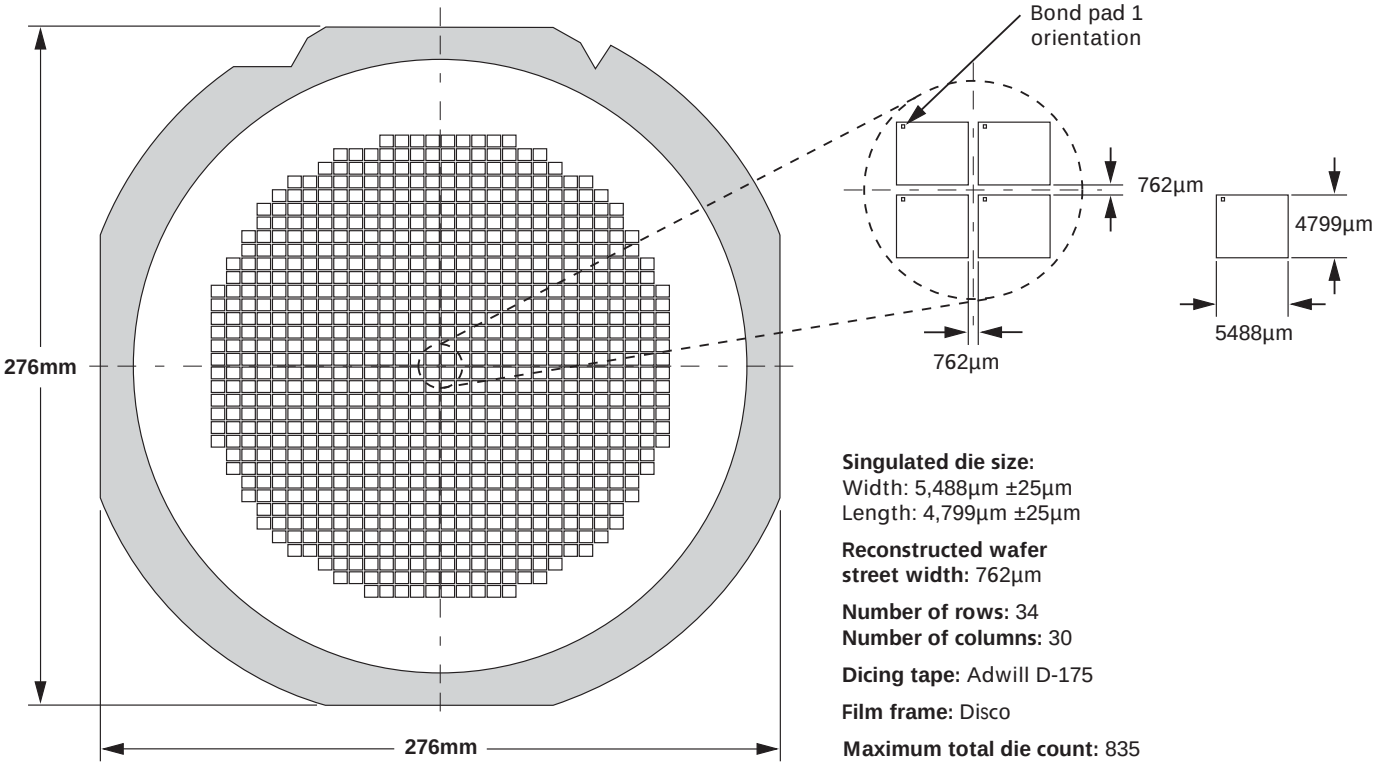


Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) *Width (X dimension)* *Length (Y dimension)*	 5,488 ±25µm 4,799 ±25µm
Bond pad size (MIN)	85µm x 100µm
Passivation openings (MIN)	75µm x 90µm
Minimum bond pad pitch	155µm
Optical array *Optical center from die center:* *Optical center from center of pad 1:*	 X = 100.00µm, Y = 0.00µm X = 2,611.82µm, Y = –2,258.11µm
First clear pixel (col. 92, row 40) *Die center to pixel corner:* *Pad 1 center to pixel corner:*	 X = 1,930.40µm, Y = 1,390.40µm X = 4,442.22µm, Y = –867.71µm
Last clear pixel (col. 1,756, row 1,310) *Die center to pixel corner:* *Pad 1 center to pixel corner:*	 X = –1,730.40µm, Y = –1,390.40µm X = 781.42µm, Y = –3,648.51µm

Figure 3: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 5,488µm ±25µm
Length: 4,799µm ±25µm

Reconstructed wafer street width: 762µm

Number of rows: 34
Number of columns: 30

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 835

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

Rev. B 11/07

- Corrected First clear pixel row from 46 to 40 in Figure 2 on page 7 and Table 3 on page 8
- Updated Figure 3, Die Orientation in Reconstructed Wafer, on page 9
- Corrected singulated die size on page 1 and in Table 3 on page 8

Rev. A 10/07

- Initial release