1/4-Inch 2Mp System-on-a-Chip (SOC) UXGA CMOS Digital Image Sensor Die

MT9D112

For the product data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Superior low-light performance
- Ultra low-power, low-cost image sensor
- Internal master clock generated by on-die phase-lock loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement, including 4-channel lens shading correction with independent corner correction
- Arbitrary image decimation with anti-aliasing
- Integrated microcontroller for flexibility
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: ITU-R BT.601 (YCbCr), 565RGB, 555RGB, 444RGB, processed Bayer, RAW8, and RAW10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate
- Parallel and serial MIPI data output
- Xenon and LED flash support with fast exposure adaptation
- Flexible support for external auto focus, optical zoom, and mechanical shutter
- Independently configurable gamma correction

Applications

- Cellular phones
- PC cameras
- PDAs

Order Information

Table 1: Available Part Numbers

Part Number	Description
MT9D112D00STCK15AC1	Bare die (22.1 deg. CRA)
MT9D112D00STCZK15AC1	Bare die (27.0 deg. CRA)

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database

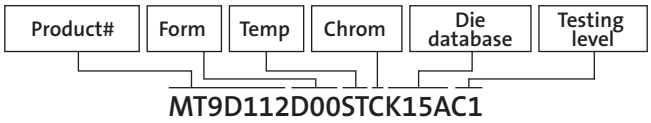
- Die outline, see Figure 2 on page 10
- Singulated die size (nominal dimension): 6,704µm ±25µm x 7,204µm ±25µm
- Bond Pad Location and Identification Tables, see pages 6–9

Options

- Form
  - Die D
- Testing
  - Standard (level 1) probe C1

General Physical Specifications

- Die thickness: 200µm ±12µm
- (Consult factory for other die thickness)
- Backside die surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm



Key Performance Parameters

- Optical format: 1/4-inch (4:3)
- Full resolution: 1600 x 1200 pixels (UXGA)
- Pixel size: 2.2µm x 2.2µm
- Chief ray angles: 22.1 degree maximum at 75 percent image height and 27.0 degree maximum at 80 percent image height
- Color filter array: RGB Bayer pattern
- Active-pixel array area: 3.56mm x 2.68mm
- Shutter type: electronic rolling shutter (ERS) with global reset
- Input clock frequency: 6–54 MHz

Key Performance Parameters (continued)

- Maximum frame rate: 15 fps at full resolution, 24 fps in preview mode, and 30 fps in video mode
- Maximum data rate/master clock: 80MB/s/6 MHz to 80 MHz
- Supply voltage
  - Analog: 2.5–3.1V
  - Digital: 1.7–1.95V
  - I/O: 1.7–3.1V
  - PLL: 2.5–3.1V
  - AF: 1.7–3.1V
- ADC resolution: 10-bit, on-die
- Responsivity: 0.53V/lux-sec (preliminary)
- Dynamic range: 59.5dB (preliminary)
- SNR MAX: 37.7dB (preliminary)
- Power consumption
  - 245mW at 15 fps, full resolution
  - 168mW at 24 fps, preview mode
  - 230mW at 30fps, video mode
  - 30µW, standby/shutdown
- Operating temperature: –30°C to +70°C (at junction)

General Description

The Aptina™ MT9D112 die is a ¼-inch 2Mp CMOS image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), and both a parallel and a serial MIPI interface. It also includes a programmable general purpose I/O module (GPIO), which can be used to control external auto focus (AF), optical zoom, or mechanical shutter.

The microcontroller manages all components of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1616 x 1216 pixels; programmable timing and control circuitry; including a PLL and external flash support; analog signal chain with automatic offset correction and programmable gain; and two 10-bit analog-to-digital converters (ADC). The entire system-on-a-chip (SOC) has ultra-low power requirements and superior low-light performance that is particularly suitable for mobile applications.

The MT9D112 is based on Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, power consumption, and integration advantages of CMOS.

MT9D112 Overview

The MT9D112 has a color image sensor with a Bayer color filter arrangement and a 2-megapixel active-pixel array with electronic rolling shutter and global reset. The sensor core readout is 10-bit and supports skipping, binning and can be flipped and/or mirrored. The sensor core also supports separate analog and digital gain for all four color channels (R, Gr, Gb, B).

The MT9D112 also has an embedded phase-locked loop (PLL) oscillator that can generate the internal sensor clock from the common wireless system clock. When in use, the PLL adjusts the incoming clock frequency up, allowing the MT9D112 to run at almost any desired resolution and frame rate within the sensor's capabilities. The PLL can be bypassed and powered down to reduce power consumption.

Low power consumption is a very important requirement for all components of wireless devices. The MT9D112 has numerous power-conserving features, including internal soft standby modes, hard, and an external SHUTDOWN pin which allows the internal power bus to be disabled.

Electromagnetic emission (EMI) is another important consideration for wireless devices. The MT9D112 can be used with either a serial MIPI interface or the parallel data output interface which has a programmable I/O slew rate to minimize EMI and an output FIFO to eliminate output data bursts.

The advanced image flow processor and flexible programmability of the MT9D112 provide a variety of ways to enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9D112 to operate at factory settings as a fully automatic, highly adaptable camera; however, most of its settings are user-programmable.

These algorithms include black level conditioning, lens shading correction, defect correction, noise reduction, color interpolation, edge detection, color correction, aperture correction, and image formatting such as cropping and scaling.

The MT9D112 also includes a sequencer which coordinates all events triggered by the user. The sequencer manages auto focus, auto white balance, flicker detection and auto exposure for the different operating modes which include preview, still capture, video, and snapshot with flash.

A two-wire serial register interface bus enables read/write access to control registers, variables and special function registers within the MT9D112. Hardware registers are grouped internally by pages and include sensor core controls, color pipeline controls, and output controls. Variables are located in the microcontroller's RAM memory and are used for drivers such as the auto exposure (AE), auto white balance (AWB), and auto focus (AF). Special function registers are registers connected to the local bus of the microcontroller and include GPIO and the waveform generator.

The general purpose I/O can be configured in a number of ways allowing the user to output a flash or shutter pulse, achieve 10-bit parallel output, or they can be configured as inputs to enable features such as an external trigger.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's standard package. Because the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9D112 die has 74 bond pads. Refer to Tables 2 and 3 on pages 6–9 for a complete list of bond pads and coordinates.

The MT9D112 die does not require the user to determine bond option features.

To ensure proper device operation, all power supply bond pads must be bonded. If auto focus is not required the following pads can be left floating: VDDAF, GNDAF, and GPIO_AF.

Storage Requirements

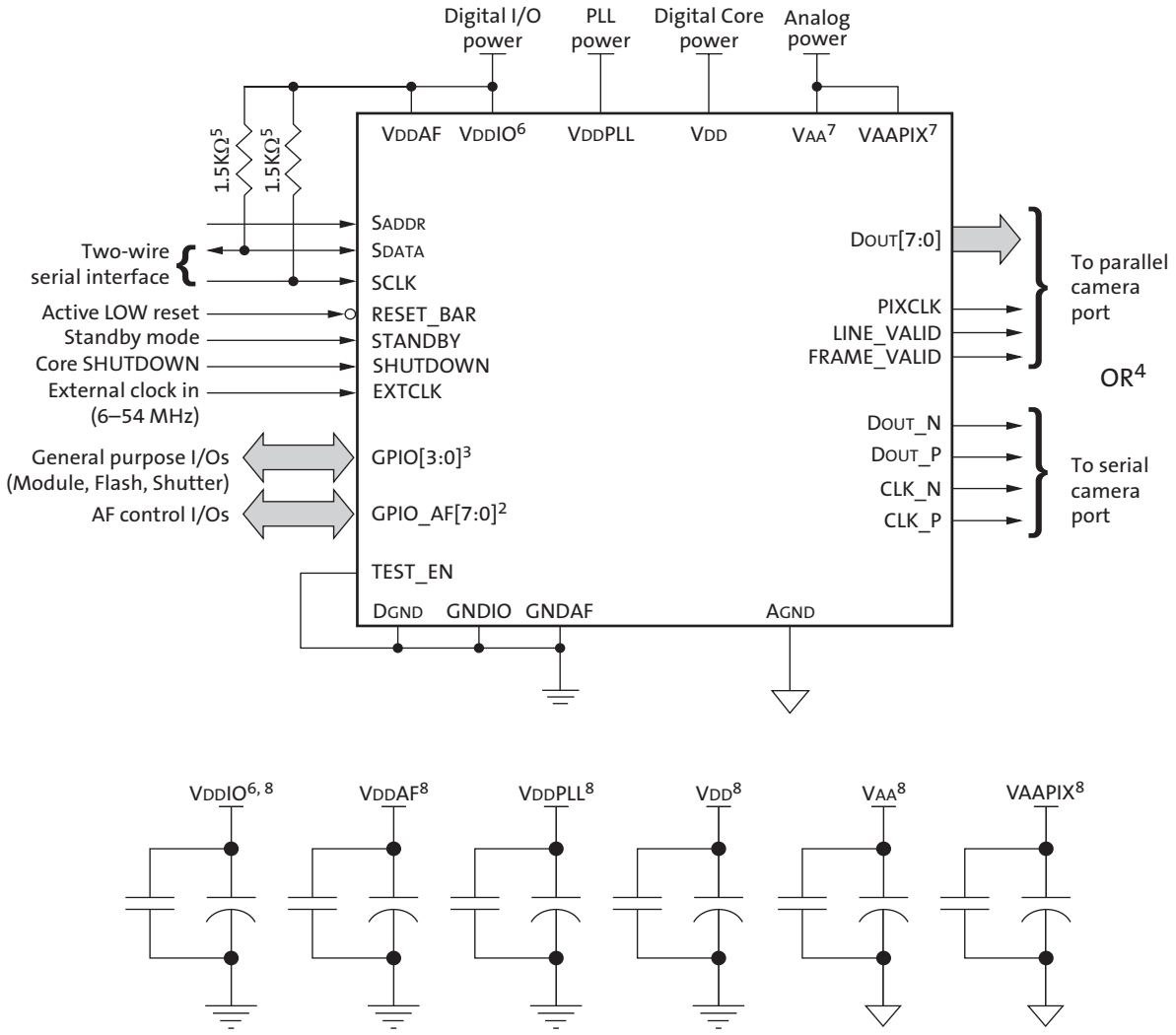
Aptina die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connections

Figure 1 shows typical MT9D112 device connections. For low-noise operation, the MT9D112 requires separate analog and digital power supplies. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9D112 also supports different digital core (VDD/DGND) and I/O power (VDDIO/DGND) power domains that can be at different voltages. PLL requires a clean power source (VDDPLL).

Figure 1: Typical Configuration (connection)



Note:
1. The typical connection shows only one scenario out of multiple possible variations for this sensor.
2. If auto focus is not required the following pads can be left floating: VDDAF, GNDAF, and GPIO_AF.
3. The GPIO pads can serve multiple features that can be reconfigured. The function and direction will vary by applications
4. Only one of the output modes (serial or parallel) can be used at any time.
5. A 1.5kΩ resistor value is recommended for the two-wire serial interface, however, greater value may be used for slower transmission speed.
6. All inputs must be configured with VDDIO.
7. VAA and VAAPIX must be tied together.
8. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Bond Pad Location and Identification Tables

Table 2: MT9D112 Bond Pad Location From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD2	0.00	0.00	0.0000000	0.0000000
2	VDD3	5903.04	0.00	0.2324031	0.0000000
3	DGND3	6150.63	–116.55	0.2421506	–0.0045884
4	SCLK	6150.63	–382.71	0.2421506	–0.0150673
5	SDATA	6150.63	–612.71	0.2421506	–0.0241224
6	VDDIO1	6150.63	–842.71	0.2421506	–0.0331776
7	GPIO0	6150.63	–1072.71	0.2421506	–0.0422327
8	GPIO1	6150.63	–1327.27	0.2421506	–0.0522547
9	GNDIO1	6150.63	–1557.27	0.2421506	–0.0613098
10	SHUTDOWN	6150.63	–1787.27	0.2421506	–0.0703650
11	GPIO2	6150.63	–2017.28	0.2421506	–0.0794203
12	GPIO3	6150.63	–2271.84	0.2421506	–0.0894423
13	VDDIO2	6150.63	–2501.84	0.2421506	–0.0984974
14	GNDIO2	6150.63	–2731.84	0.2421506	–0.1075526
15	AGND3	6150.63	–3191.84	0.2421506	–0.1256628
16	AGND2	6150.63	–3421.84	0.2421506	–0.1347179
17	DNU[2]	6150.63	–3552.88	0.2421506	–0.1398770
18	VAA3	6150.63	–3694.72	0.2421506	–0.1454612
19	DNU	6150.63	–3825.76	0.2421506	–0.1506203
20	AGND1	6150.63	–3956.80	0.2421506	–0.1557793
21	DNU	6150.63	–4087.84	0.2421506	–0.1609384
22	VAA2	6150.63	–4229.68	0.2421506	–0.1665226
23	VAA1	6150.63	–4459.68	0.2421506	–0.1755778
24	VAAPIX3	6150.63	–4821.84	0.2421506	–0.1898360
25	VAAPIX2	6150.63	–5051.84	0.2421506	–0.1988911
26	VAAPIX1	6150.63	–5281.84	0.2421506	–0.2079463
27	SADDR	6150.63	–5861.67	0.2421506	–0.2307742
28	STANDBY	6150.63	–6091.67	0.2421506	–0.2398293
29	VDDIO3	6150.63	–6321.67	0.2421506	–0.2488844
30	RESET_BAR	6150.63	–6551.67	0.2421506	–0.2579396
31	Dgnd4	6150.63	–6781.67	0.2421506	–0.2669947
32	VDD1	5903.04	–6898.21	0.2324031	–0.2715831
33	TEST_EN[3]	5511.42	–6898.21	0.2169848	–0.2715831
34	VDDAF2	4893.68	–6898.21	0.1926646	–0.2715831
35	GNDAF2	4663.39	–6898.21	0.1835980	–0.2715831
36	GPIO_AF7	4433.39	–6898.21	0.1745429	–0.2715831
37	GPIO_AF6	4203.39	–6898.21	0.1654878	–0.2715831
38	GPIO_AF5	3948.83	–6898.21	0.1554657	–0.2715831
39	GPIO_AF4	3718.83	–6898.21	0.1464106	–0.2715831
40	VDDAF1	3488.83	–6898.21	0.1373555	–0.2715831
41	GNDAF1	3258.83	–6898.21	0.1283004	–0.2715831
42	GPIO_AF3	3028.83	–6898.21	0.1192453	–0.2715831
43	GPIO_AF2	2798.83	–6898.21	0.1101902	–0.2715831

Table 2: MT9D112 Bond Pad Location From Center of Pad 1 (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	GPIO_AF1	2544.27	–6898.21	0.1001681	–0.2715831
45	GPIO_AF0	2314.27	–6898.21	0.0911130	–0.2715831
46	VDDAF0	2084.27	–6898.21	0.0820579	–0.2715831
47	GNDAF0	1854.27	–6898.21	0.0730028	–0.2715831
48	VDDPLL	–247.59	–6781.67	–0.0097474	–0.2669947
49	GNDIO3	–247.59	–6551.67	–0.0097474	–0.2579396
50	CLKIN	–247.59	–6183.80	–0.0097474	–0.2434567
51	VDDIO6	–247.59	–5893.80	–0.0097474	–0.2320394
52	DOUT_P	–247.59	–5660.22	–0.0097474	–0.2228433
53	DOUT_N	–247.59	–5404.22	–0.0097474	–0.2127646
54	CLK_P	–247.59	–5153.35	–0.0097474	–0.2028878
55	CLK_N	–247.59	–4897.35	–0.0097474	–0.1928091
56	DGND1	–247.59	–4647.59	–0.0097474	–0.1829758
57	VDD0	–247.59	–4282.49	–0.0097474	–0.1686018
58	DGND0	–247.59	–3907.37	–0.0097474	–0.1538333
59	LINE_VALID	–247.59	–3677.37	–0.0097474	–0.1447781
60	FRAME_VALID	–247.59	–3447.37	–0.0097474	–0.1357230
61	DOUT7	–247.59	–3192.81	–0.0097474	–0.1257010
62	DOUT6	–247.59	–2962.81	–0.0097474	–0.1166459
63	VDDIO5	–247.59	–2732.81	–0.0097474	–0.1075907
64	DOUT5	–247.59	–2502.81	–0.0097474	–0.0985356
65	DOUT4	–247.59	–2272.81	–0.0097474	–0.0894805
66	DOUT3	–247.59	–2018.25	–0.0097474	–0.0794585
67	VDDIO0	–247.59	–1788.25	–0.0097474	–0.0704033
68	PIXCLK	–247.59	–1558.25	–0.0097474	–0.0613482
69	GNDIO0	–247.59	–1328.25	–0.0097474	–0.0522931
70	DOUT2	–247.59	–1098.25	–0.0097474	–0.0432380
71	DOUT1	–247.59	–868.25	–0.0097474	–0.0341829
72	DOUT0	–247.59	–613.69	–0.0097474	–0.0241608
73	VDDIO4	–247.59	–383.69	–0.0097474	–0.0151057
74	DGND2	–247.59	–116.55	–0.0097474	–0.0045884

Note:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use.
3. TEST_EN must be connected to DGND for proper device functionality.
4. To ensure proper device operation, all power supply bond pads must be bonded.

Table 3: MT9D112 Bond Pad Location From Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD2	–2951.52	3449.11	–0.1162016	0.1357915
2	VDD3	2951.52	3449.11	0.1162016	0.1357915
3	DGND3	3199.11	3332.56	0.1259490	0.1312031
4	SCLK	3199.11	3066.40	0.1259490	0.1207242
5	SDATA	3199.11	2836.40	0.1259490	0.1116691
6	VDDIO1	3199.11	2606.40	0.1259490	0.1026140
7	GPIO0	3199.11	2376.40	0.1259490	0.0935589
8	GPIO1	3199.11	2121.84	0.1259490	0.0835368
9	GNDIO1	3199.11	1891.84	0.1259490	0.0744817
10	SHUTDOWN	3199.11	1661.84	0.1259490	0.0654266
11	GPIO2	3199.11	1431.83	0.1259490	0.0563713
12	GPIO3	3199.11	1177.27	0.1259490	0.0463492
13	VDDIO2	3199.11	947.27	0.1259490	0.0372941
14	GNDIO2	3199.11	717.27	0.1259490	0.0282390
15	AGND3	3199.11	257.27	0.1259490	0.0101287
16	AGND2	3199.11	27.27	0.1259490	0.0010736
17	DNU[2]	3199.11	–103.77	0.1259490	–0.0040854
18	VAA3	3199.11	–245.61	0.1259490	–0.0096697
19	DNU	3199.11	–376.65	0.1259490	–0.0148287
20	AGND1	3199.11	–507.69	0.1259490	–0.0199878
21	DNU	3199.11	–638.73	0.1259490	–0.0251469
22	VAA2	3199.11	–780.57	0.1259490	–0.0307311
23	VAA1	3199.11	–1010.57	0.1259490	–0.0397862
24	VAAPIX3	3199.11	–1372.73	0.1259490	–0.0540445
25	VAAPIX2	3199.11	–1602.73	0.1259490	–0.0630996
26	VAAPIX1	3199.11	–1832.73	0.1259490	–0.0721547
27	SADDR	3199.11	–2412.56	0.1259490	–0.0949827
28	STANDBY	3199.11	–2642.56	0.1259490	–0.1040378
29	VDDIO3	3199.11	–2872.56	0.1259490	–0.1130929
30	RESET_BAR	3199.11	–3102.56	0.1259490	–0.1221480
31	Dgnd4	3199.11	–3332.56	0.1259490	–0.1312031
32	VDD1	2951.52	–3449.11	0.1162016	–0.1357915
33	TEST_EN	2559.90	–3449.11	0.1007833	–0.1357915
34	VDDAF2	1942.16	–3449.11	0.0764630	–0.1357915
35	GNDAF2	1711.87	–3449.11	0.0673965	–0.1357915
36	GPIO_AF7	1481.87	–3449.11	0.0583413	–0.1357915
37	GPIO_AF6	1251.87	–3449.11	0.0492862	–0.1357915
38	GPIO_AF5	997.31	–3449.11	0.0392642	–0.1357915
39	GPIO_AF4	767.31	–3449.11	0.0302091	–0.1357915

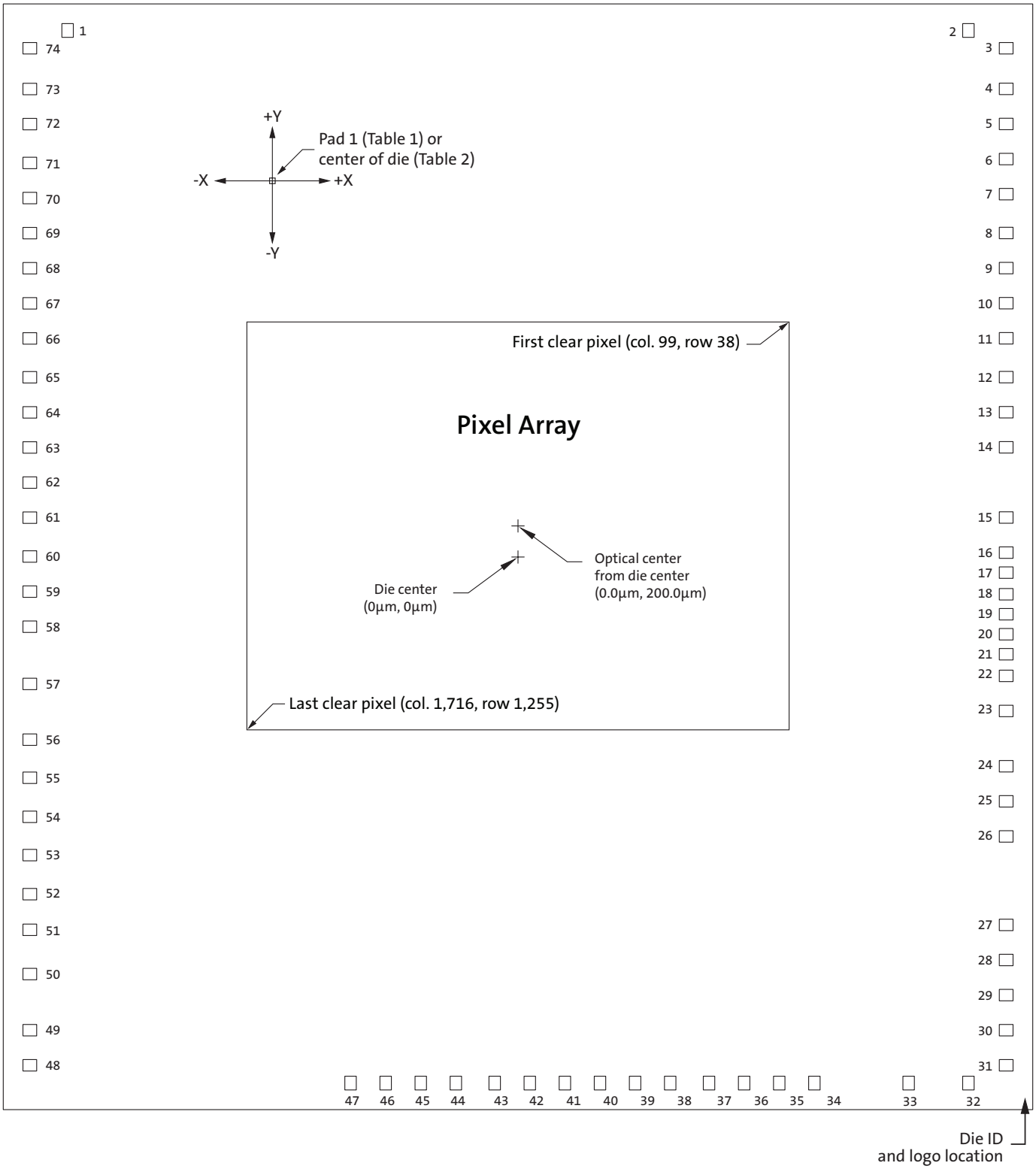
Table 3: MT9D112 Bond Pad Location From Center of Die (0, 0) (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
40	VDDAF1	537.31	–3449.11	0.0211539	–0.1357915
41	GNDAF1	307.31	–3449.11	0.0120988	–0.1357915
42	GPIO_AF3	77.31	–3449.11	0.0030437	–0.1357915
43	GPIO_AF2	–152.69	–3449.11	–0.0060114	–0.1357915
44	GPIO_AF1	–407.25	–3449.11	–0.0160335	–0.1357915
45	GPIO_AF0	–637.25	–3449.11	–0.0250886	–0.1357915
46	VDDAF0	–867.25	–3449.11	–0.0341437	–0.1357915
47	GNDAF0	–1097.25	–3449.11	–0.0431988	–0.1357915
48	VDDPLL	–3199.11	–3332.56	–0.1259490	–0.1312031
49	GNDIO3	–3199.11	–3102.56	–0.1259490	–0.1221480
50	CLKIN	–3199.11	–2734.70	–0.1259490	–0.1076652
51	VDDIO6	–3199.11	–2444.70	–0.1259490	–0.0962478
52	DOUT_P	–3199.11	–2211.12	–0.1259490	–0.0870518
53	DOUT_N	–3199.11	–1955.12	–0.1259490	–0.0769730
54	CLK_P	–3199.11	–1704.25	–0.1259490	–0.0670963
55	CLK_N	–3199.11	–1448.25	–0.1259490	–0.0570175
56	DGND1	–3199.11	–1198.48	–0.1259490	–0.0471843
57	VDD0	–3199.11	–833.38	–0.1259490	–0.0328102
58	DGND0	–3199.11	–458.26	–0.1259490	–0.0180417
59	LINE_VALID	–3199.11	–228.26	–0.1259490	–0.0089866
60	FRAME_VALID	–3199.11	1.74	–0.1259490	0.0000685
61	DOUT7	–3199.11	256.30	–0.1259490	0.0100906
62	DOUT6	–3199.11	486.30	–0.1259490	0.0191457
63	VDDIO5	–3199.11	716.30	–0.1259490	0.0282008
64	DOUT5	–3199.11	946.30	–0.1259490	0.0372559
65	DOUT4	–3199.11	1176.30	–0.1259490	0.0463110
66	DOUT3	–3199.11	1430.86	–0.1259490	0.0563331
67	VDDIO0	–3199.11	1660.86	–0.1259490	0.0653882
68	PIXCLK	–3199.11	1890.86	–0.1259490	0.0744433
69	GNDIO0	–3199.11	2120.86	–0.1259490	0.0834984
70	DOUT2	–3199.11	2350.86	–0.1259490	0.0925535
71	DOUT1	–3199.11	2580.86	–0.1259490	0.1016087
72	DOUT0	–3199.11	2835.42	–0.1259490	0.1116307
73	VDDIO4	–3199.11	3065.42	–0.1259490	0.1206858
74	DGND2	–3199.11	3332.56	–0.1259490	0.1312031

Note: 1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use.
3. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 2: Die Outline (Top View)

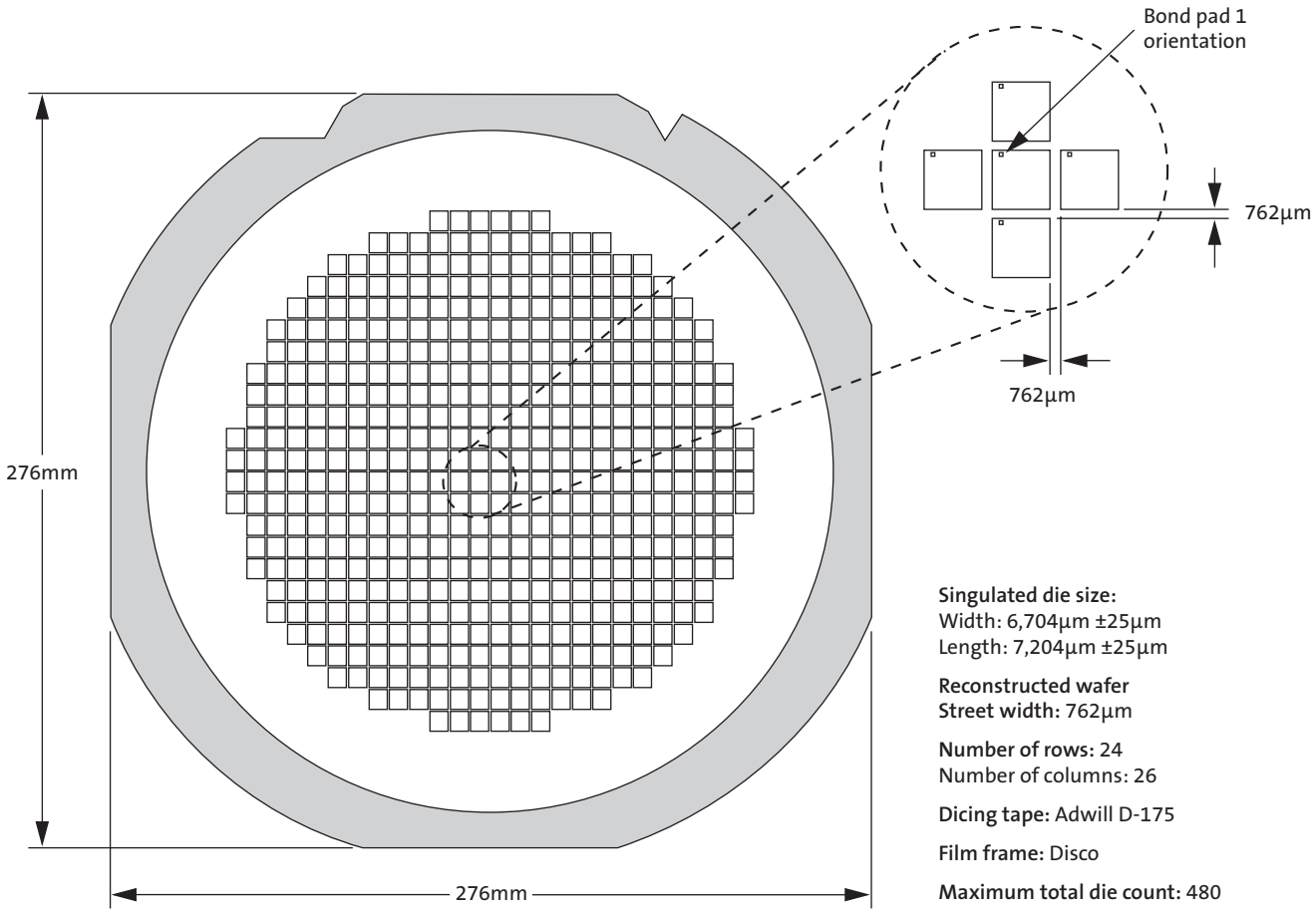


Physical Specifications

Table 4: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) Width (X dimension): Length (Y dimension):	 6,704µm ±25µm 7,204µm ±25µm
Bond pad size (MIN)	100µm x 85µm (3.94 mil x 3.35 mil)
Passivation openings (MIN)	90µm x 75µm (3.54 mil x 2.95mil)
Minimum bond pad pitch Between any two bond pads: For device functional use:	 131.04µm (5.159 mil) 230.00µm (9.055 mil)
Optical array *Optical center from die center:* Optical center from center of pad 1:	 X = 0.00µm, Y = 200.00µm X = 2,951.52µm, Y = –3,249.11µm
First clear pixel (col. 99, row 38) *From die center:* *From center of pad 1:*	 X = 1,778.65µm, Y = 1,541.00µm X = 4,730.17µm, Y = –1,908.11µm
Last clear pixel (col. 1,716, row 1,255) *From die center:* *From center of pad 1:*	 X = –1,778.65µm, Y = –1,136.50µm X = 1,172.87µm, Y = –4,585.61µm

Figure 3: MT9D112 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 6,704µm ±25µm
Length: 7,204µm ±25µm

Reconstructed wafer
Street width: 762µm

Number of rows: 24
Number of columns: 26

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 480

Revision History

Rev. H 5/2/11

- Removed Digital Clarity
- Applied updated Aptina template

Rev. G 10/10

- Updated to non-confidential

Rev. F 8/10

- Updated to Aptina template

Rev. E 3/08

- Updated template
- Updated part numbers in Table 1, “Available Part Numbers,” on page 1
- Updated document from Preliminary to Production to match data sheet

Rev. D 6/07

- Added DigitalClarity to trademarks on last page
- Updated Figure 3 on page 12
- Updated format

Rev. C 7/06

- Corrected part number typographic error in Bond Pad Location and Identification Tables on pages 6–9

Rev. B 2/06

- Changed first clear pixel to: Col 99, Row 38 and last clear pixel to: Col 1,716, Row 1,255, pages 10 and 11

Rev. A 12/05

- Initial release, Advance

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