



The Perfect Fit for Thin Cell Phone Designs

Aptina's 2-Megapixel, 1/4-Inch CMOS Camera System-on-a-Chip

Features

- An industry first – parallel and serial mobile industry processor interface (MIPI) data output
- Industry-leading 2.2 μ m pixel technology
- 15 frames per second (fps) at full resolution; 30 fps in video mode
- Superior low-light performance
- Ultra-low-power, low-cost
- Internal master clock generated by on-chip phase-locked loop (PLL) oscillator
- Integrated image flow processor (IFP)
- Automatic image correction and enhancement, including lens shading correction
- Arbitrary image decimation with anti-aliasing
- Xenon and LED flash support with fast exposure adaptation
- Two-wire serial interface
- Selectable output data format: ITU-R BT.601 (YCbCr), 565RGB, 555RGB, 444RGB, processed bayer, RAW8 and RAW10-bit

Thin Phone? Think Aptina.

High resolution; small factor. Aptina's new 2-megapixel, 1/4-inch CMOS image sensor is the perfect fit for today's increasingly popular thin phone designs.

The MT9D112 SOC image sensor—developed using Aptina's advanced 2.2 μ m pixel technology and featuring our exclusive low-noise technology—provides best-in-class image quality while maintaining a small form factor. Aptina's MT9D112 is also the industry's first sensor to incorporate mobile industry processor interface (MIPI) standards that support both a parallel and serial interface (CSI-2 and D-PHY)—a significant advancement in enabling simpler camera designs.

The MT9D112 is a fully integrated SOC sensor with additional logic that simplifies the camera module design, related manufacturing processes, system integration, power management, and component count. As the first

sensor to incorporate MIPI standards, it also provides a common platform for design engineers, leading to higher performance, lower development costs, and faster time to market.

Applications

- Cell phones
- PDAs
- PC cameras

Automated, Integrated, Sophisticated Functionality

The MT9D112 camera system features an integrated microcontroller, a sophisticated IFP, and both parallel and serial MIPI data out. It also includes a programmable general purpose I/O module (GPIO), which can be used to control external auto focus (AF), optical zoom, or mechanical shutter.

The microcontroller manages all components of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1600 x 1200 pixels; programmable timing and control circuitry, including a PLL and external flash support; analog signal chain with automatic offset correction and programmable gain; and two 10-bit analog-to-digital converters (ADCs).

Low power consumption is an important requirement for all components in wireless devices. The MT9D112 has numerous power-conserving features, including an external SHUTDOWN pin, internal soft standby modes, and the ability to individually shut down unused digital blocks. The ultra-low power requirements and superior low-light performance of this system-on-a-chip (SOC) make it particularly well suited to mobile applications.

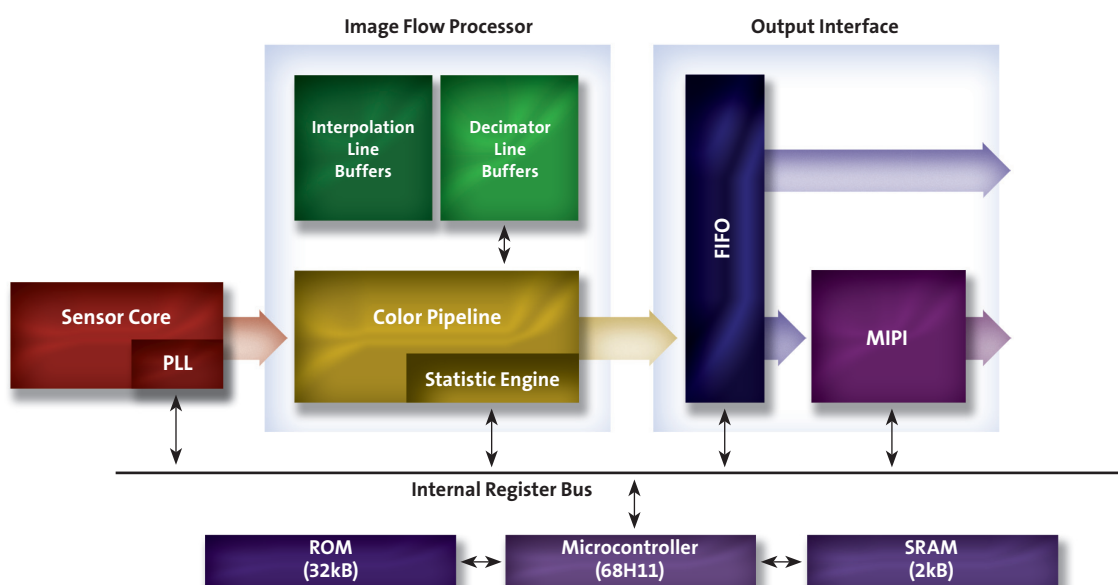
How to Buy

Production and sample quantities of Aptina products may be ordered through qualified distributors. See our Web site for details. You may also request access to NDA data sheets and other technical documentation by visiting our Web site.

Specifications

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|--------------------------|--|--------------------------|--|
| • Pixel Size: | 2.2 μ m x 2.2 μ m | • ADC: | 10 bit, on-chip |
| • Array Format (Active): | 1600H x 1200V | • Dynamic Range: | 59.5dB |
| • Imaging Area: | 3.55mm x 2.68mm | • Signal-to-Noise Ratio: | 37.7dB (MAX) |
| • Optical Format: | 1/4 inch (4:3) | • Responsivity: | 0.53 V/lux-sec |
| • Color Filter Array: | RGB Bayer pattern | • Supply Voltage: | Analog: 2.5–3.1V Digital: 1.7–1.95V I/O: 1.7–3.1V PLL: 2.5–3.1V |
| • Frame Rates: | 15 fps (full resolution) 24 fps (preview mode) 30 fps (video mode) | • Flash Support: | Xenon and LED |
| • MAX Data Rate: | 40 megapixels per second at 80 MHz | • Operating Temp: | –30°C to +70°C |
| • Master Clock: | 6 MHz to 80 MHz | • Package: | Die |

SOC Block Diagram



aptina.com

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