1/5-Inch 2Mp System-on-a-Chip (SOC) CMOS Digital Image Sensor Die

MT9D113 Die Data Sheet

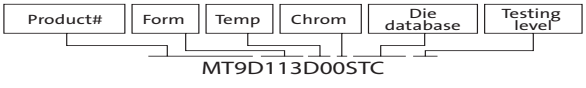
For the product data sheets, refer to Aptina's Web site: www.aptina.com

Features

- Enables 6.5mm^2 module size (compared to 8.5mm^2 module size for the MT9D112)
- Same or better image quality compared to MT9D112
- Individual module ID support through one-time programmable (OTP) memory
- Surface-fit lens correction (LC) to compensate for lens/small-pixel vignetting and corner color variations
- Automatic functions: exposure, white balance, black level offset correction, flicker detection and avoidance, color saturation control, defect identification and correction, aperture correction, and GPIO
- Programmable controls: exposure, white balance, horizontal and vertical blanking, color, sharpness, gamma, lens shading correction, horizontal and vertical image flip, zoom, windowing, sampling rates, and GPIO
- 15 frames per second at 1600H x 1200V with moderate pixel clock frequency to minimize baseband reception interference and 30 fps at 800H x 600V
- 2 x 2 pixel binning to improve low-light image quality
- Support for external LED or xenon flash
- On-die phase-lock loop (PLL) to minimize the number of system clocks
- Low-power modes to prolong battery life of portable devices
- Fail-safe I/Os with programmable output slew rate
- Industry-standard two-wire serial interface for controls
- 10-bit parallel or MIPI serial interfaces for image data

Ordering Information

MT9D113D00STC



Die Database

- Die outline, see Figure 2 on page 10
- Singulated die size (nominal dimension): 5,041µm ±25µm x 5,221µm ±25µm
- Bond Pad Location and Identification Tables, see pages 6–9

Options	Designator
• Form	
– Die	D
• Testing	
– Standard (level 1) probe	C1

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

General Physical Specifications

- Die thickness: 200µm ±12µm (Consult factory for other die thickness)
- Back side die surface of bare silicon
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 3.1kÅ
- Typical metal 4 thickness: 4.15kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Key Performance Parameters

- Pixel size: 1.75µm x 1.75µm
- Optical format: 1/5-inch (4:3 aspect ratio)
- Targeted module size (estimated): 6.5mm x 6.5mm x 5mm
- Array format (active): 1600H x 1200V pixels
- Imaging area: 2.80mm x 2.10mm, 3.50mm diagonal
- CRA: 25° MAX at 90% image height (preliminary)
- Color filter array: RGB color filters

Key Performance Parameters (continued)

- Frame rate: 15 fps at full resolution, 30 fps (video mode)
- Scan mode: progressive
- Shutter: electronic rolling shutter (ERS)
- Windowing: programmable
- Output interfaces: MIPI single-lane or parallel 10-bit
- Data rate
  - MIPI: up to 640 Mb/s and up to 85 MHz parallel data
  - Parallel: 80 Mb/s
- Responsivity: 0.2 V/lux-sec (550nm)
- Signal-to-noise ratio: >37dB maximum
- Dynamic range: >60dB (pixel)
- Full well: >6900e- (linear)
- Read noise: 4e- (8x gain)
- Supply voltage
  - Analog: 2.8V
  - Digital: 1.8V
  - I/O: 1.8V or 2.8V
  - OTP: 8V
- Operating temperature: –30°C to 70°C (at junction)

General Description

Aptina's MT9D113 is a complete camera system-on-a-chip (SOC) image sensor die that outputs sharp, clear, progressive-scan images while extending an application's battery life. It provides best-in-class image quality while maintaining a small form factor.

The MT9D113 was developed using Aptina's industry-leading 1.75µm pixel technology and features our exclusive low-noise technology that enables the sensor to capture superior-quality color images without increasing power requirements.

The MT9D113 integrates many advanced features—scaling, windowing, row mirroring, left-right frame reversal, column mirroring, and power-on-reset—right on the die. This minimizes its form factor and maximizes board-space efficiency.

The MT9D113 enables the end-user to adjust its variable functions—such as frame rate, programmable gain, and exposure control—through a simple two-wire serial interface. Designers will benefit from the easy application designs they can make around the MT9D113. Designs can be smaller than ever, ensuring higher-performance products that take better-quality pictures and consume less power.

Along with its 1.75µm^2 pixel size and 1/5-inch optical format, the MT9D113 holds—within its small form factor—a lot of features, such as programmable gain and exposure control, horizontal and vertical blanking, windowing, ADC reference, as well as left-right and top-bottom image reversal.

Die Testing Procedures

Aptina® imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's characterization package. Because the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications in this document are provided for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9D113 die has 65 bond pads. Refer to Table 1 and 2 on pages 6–8 for a complete list of bond pads and coordinates.

The MT9D113 die does not require the user to determine bond option features. The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

All DGND pads must be tied together, as must all AGND pads, all GND_IO pads, all VDD pads, all VDD_IO pads, and all VAA pads with the VAA_PIX pad.

Storage Requirements

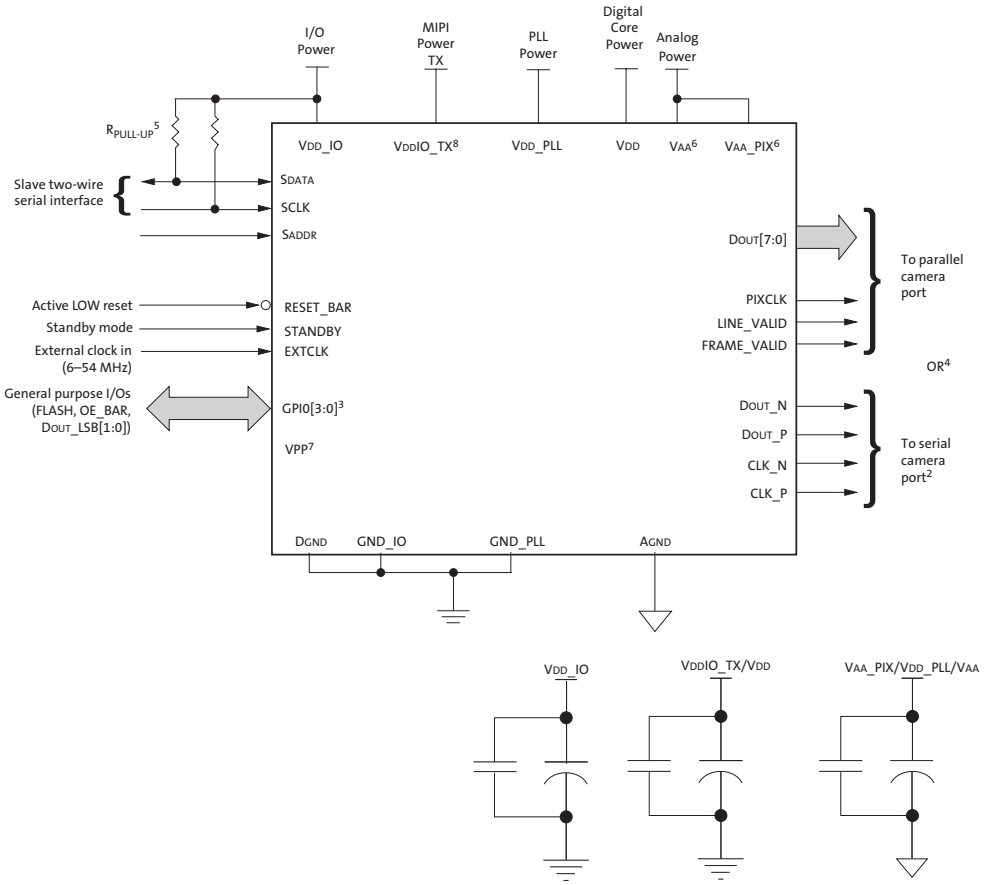
Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connections

Figure 1 on page 4 shows typical MT9D113 device connections. For low-noise operation, the MT9D113 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9D113 also supports different digital core power (VDD/DGND), MIPI output power (VDDIO_TX/GNDIO_TX), and I/O power (VDD_IO/GND_IO) power domains that can be at different voltages. The PLL requires a clean power source (VDD_PLL).

Figure 1: MT9D113 Typical Connections[1] (Single Camera)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI Interface is not required, the following pads must be left floating: DOUT_P, DOUT_N, CLK_P, and CLK_N.
3. The general purpose input/output (GPIO) pads can serve multiple features that can be reconfigured. The function and direction will vary by applications.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. Aptina recommends a resistor value of 1.5KΩ to VDD_IO for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
6. VAA and VAA_PIX may be tied together. Although separate decoupling capacitors are recommended for VAA and VAA_PIX, decoupling capacitors can be shared if one would like to reduce module size.
7. VPP is the one-time programmable (OTP) memory programming voltage and should be left floating during normal operation.

8. 1.8V supply shared by MIPI interface and V_{DD} to reduce number of decoupling caps, hence, module size. V_{DD}IO_TX must be connected to a 1.8v power supply source even though MIPI interface is not used.
9. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad and that a 10µF capacitor be placed nearby off-module. Actual values and results may vary depending on layout and design considerations.
10. V_{DD}_PLL and V_{AA} can share the same power source in which case GND_PLL must be connected to GND.
11. Internal pull-up in RESET_BAR pin and can be left floating when not connected.

Decoupling Capacitor Recommendations

It is important to provide clean, well regulated power to each power supply. The Aptina recommendation for capacitor placement and values are based on our internal demo camera design and verified in hardware.

Note: Because hardware design is influenced by many factors, such as layout, operating conditions, and component selection, the customer is ultimately responsible to ensure that clean power is provided for their own designs.

In order of preference, Aptina recommends:

1. Mount 0.1µF and 1µF decoupling capacitors for each power supply as close as possible to the pad and place a 10µF capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design, use a 0.1µF and 1µF capacitor for each of the three regulated supplies. Aptina also recommends placing a 10µF capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, a 1µF capacitor for each of the three regulated supplies is preferred. Aptina recommends placing a 10µF capacitor for each supply off-module but closed to each supply.
4. If module limitations allow for only three decoupling capacitors, a 0.1µF capacitor for each of the three regulated supplies is preferred. Aptina recommends placing a 10ìFcapacitor for each supply off-module but close to each supply.
5. Priority should be given to the VAA supply for additional decoupling capacitors.
6. Inductive filtering components are not recommended.
7. Follow best practices when performing physical layout. Refer to technical note TN-09-131.

Bond Pad Location and Identification Tables

Table 1: MT9D113 Bond Pad Location From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	SDATA	0	0	0.0000000	0.0000000
2	VDD3	162.46	0	0.0063961	0.0000000
3	DGND4	502.86	0	0.0197976	0.0000000
4	SADDR	655.06	0	0.0257898	0.0000000
5	VDD_IO1	813.06	0	0.0320102	0.0000000
6	RESET_BAR	971.06	0	0.0382307	0.0000000
7	GND_IO1	1129.06	0	0.0444512	0.0000000
8	STANDBY	1287.06	0	0.0506717	0.0000000
9	SCLK	1445.06	0	0.0568921	0.0000000
10	DNU[2]	1603.06	0	0.0631126	0.0000000
11	EXTCLK	1761.06	0	0.0693331	0.0000000
12	VDD1	1919.06	0	0.0755535	0.0000000
13	GND_IO2	2200.31	0	0.0866264	0.0000000
14	GPIO_0/DOUT_LSB0	2358.31	0	0.0928469	0.0000000
15	DGND1	2516.31	0	0.0990673	0.0000000
16	GPIO_1/DOUT_LSB1	2674.31	0	0.1052878	0.0000000
17	VDD_IO2	2832.31	0	0.1115083	0.0000000
18	GPIO_2/OE_BAR	2990.31	0	0.1177287	0.0000000
19	VDDIO_TX0	3148.31	0	0.1239492	0.0000000
20	CLK_N	3409.92	0	0.1342488	0.0000000
21	CLK_P	3639.92	0	0.1433039	0.0000000
22	DOUT_N	3869.93	0	0.1523594	0.0000000
23	DOUT_P	4099.93	0	0.1614146	0.0000000
24	VDD_PLL	4492.68	–394.5	0.1768772	–0.0155315
25	GND_PLL	4492.68	–504.7	0.1768772	–0.0198701
26	VAA4	4492.68	–1269.7	0.1768772	–0.0499882
27	AGND5	4492.68	–1444.7	0.1768772	–0.0568780
28	VAA3	4492.68	–1619.7	0.1768772	–0.0637677
29	AGND4	4492.68	–1794.7	0.1768772	–0.0706575
30	AGND3	4492.68	–1994.9	0.1768772	–0.0785394
31	DNU[2]	4492.68	–2165.1	0.1768772	–0.0852402
32	DNU[2]	4492.68	–2275.3	0.1768772	–0.0895787
33	DNU[2]	4492.68	–2385.5	0.1768772	–0.0939173
34	VAA_PIX	4492.68	–2545.7	0.1768772	–0.1002244
35	VPP	4492.68	–2984.04	0.1768772	–0.1174819
36	AGND2	4492.68	–3272.38	0.1768772	–0.1288339
37	VAA2	4492.68	–3447.38	0.1768772	–0.1357236
38	AGND1	4492.68	–3622.38	0.1768772	–0.1426134
39	VAA1	4492.68	–3797.38	0.1768772	–0.1495031
40	GND_IO6	4492.68	–3969.18	0.1768772	–0.1562669
41	VDD_IO6	4492.68	–4189.38	0.1768772	–0.1649362
42	GPIO_3/FLASH	4492.68	–4532.91	0.1768772	–0.1784610
43	PIXCLK	4492.68	–4706.33	0.1768772	–0.1852886
44	GND_IO5	4335.51	–5006.6	0.1706894	–0.1971102

Table 1: MT9D113 Bond Pad Location From Center of Pad 1 (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
45	LINE_VALID	4176.44	–5006.6	0.1644268	–0.1971102
46	VDD_IO5	4020.44	–5006.6	0.1582850	–0.1971102
47	FRAME_VALID	3864.44	–5006.6	0.1521433	–0.1971102
48	DOUT7	3691.02	–5006.6	0.1453157	–0.1971102
49	DOUT6	3517.6	–5006.6	0.1384882	–0.1971102
50	GND_IO4	3361.6	–5006.6	0.1323465	–0.1971102
51	DOUT5	3205.6	–5006.6	0.1262047	–0.1971102
52	VDD_IO4	3049.6	–5006.6	0.1200630	–0.1971102
53	DOUT4	2893.6	–5006.6	0.1139213	–0.1971102
54	DOUT3	2720.18	–5006.6	0.1070937	–0.1971102
55	GND_IO3	2564.18	–5006.6	0.1009520	–0.1971102
56	DOUT2	2408.18	–5006.6	0.0948102	–0.1971102
57	DOUT1	2234.76	–5006.6	0.0879827	–0.1971102
58	VDD_IO3	2078.76	–5006.6	0.0818409	–0.1971102
59	DOUT0	1922.76	–5006.6	0.0756992	–0.1971102
60	DNU[2]	1759.95	–5006.6	0.0692894	–0.1971102
61	DNU	1603.95	–5006.6	0.0631476	–0.1971102
62	VDD2	1447.95	–5006.6	0.0570059	–0.1971102
63	DGND3	1166.7	–5006.6	0.0459331	–0.1971102
64	DGND2	1010.7	–5006.6	0.0397913	–0.1971102
65	VDD4	729.46	–5006.6	0.0287189	–0.1971102

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

Table 2: MT9D113 Bond Pad Location From Center of Die (0, 0)

Pad	MT9D113	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	SDATA	–2079.38	2503.30	–0.0818654	0.0985551
2	VDD3	–1916.93	2503.30	–0.0754697	0.0985551
3	DGND4	–1576.52	2503.30	–0.0620677	0.0985551
4	SADDR	–1424.32	2503.30	–0.0560756	0.0985551
5	VDD_IO1	–1266.32	2503.30	–0.0498551	0.0985551
6	RESET_BAR	–1108.32	2503.30	–0.0436346	0.0985551
7	GND_IO1	–950.32	2503.30	–0.0374142	0.0985551
8	STANDBY	–792.32	2503.30	–0.0311937	0.0985551
9	SCLK	–634.32	2503.30	–0.0249732	0.0985551
10	DNU[2]	–476.32	2503.30	–0.0187528	0.0985551
11	EXTCLK	–318.32	2503.30	–0.0125323	0.0985551
12	VDD1	–160.32	2503.30	–0.0063118	0.0985551
13	GND_IO2	120.93	2503.30	0.0047610	0.0985551
14	GPIO_0/DOUT_LSB0	278.93	2503.30	0.0109815	0.0985551
15	DGND1	436.93	2503.30	0.0172020	0.0985551
16	GPIO_1/DOUT_LSB1	594.93	2503.30	0.0234224	0.0985551
17	VDD_IO2	752.93	2503.30	0.0296429	0.0985551
18	GPIO_2/OE_BAR	910.93	2503.30	0.0358634	0.0985551
19	VDDIO_TX0	1068.93	2503.30	0.0420839	0.0985551
20	CLK_N	1330.54	2503.30	0.0523835	0.0985551
21	CLK_P	1560.54	2503.30	0.0614386	0.0985551
22	DOUT_N	1790.55	2503.30	0.0704941	0.0985551
23	DOUT_P	2020.55	2503.30	0.0795492	0.0985551
24	VDD_PLL	2413.30	2108.80	0.0950118	0.0830236
25	GND_PLL	2413.30	1998.60	0.0950118	0.0786850
26	VAA4	2413.30	1233.60	0.0950118	0.0485669
27	AGND5	2413.30	1058.60	0.0950118	0.0416772
28	VAA3	2413.30	883.60	0.0950118	0.0347874
29	AGND4	2413.30	708.60	0.0950118	0.0278976
30	AGND3	2413.30	508.40	0.0950118	0.0200157
31	DNU[2]	2413.30	338.20	0.0950118	0.0133150
32	DNU[2]	2413.30	228.00	0.0950118	0.0089764
33	DNU[2]	2413.30	117.80	0.0950118	0.0046378
34	VAA_PIX	2413.30	–42.40	0.0950118	–0.0016693
35	VPP	2413.30	–480.74	0.0950118	–0.0189268
36	AGND2	2413.30	–769.08	0.0950118	–0.0302787
37	VAA2	2413.30	–944.08	0.0950118	–0.0371685
38	AGND1	2413.30	–1119.08	0.0950118	–0.0440583
39	VAA1	2413.30	–1294.08	0.0950118	–0.0509480
40	GND_IO6	2413.30	–1465.88	0.0950118	–0.0577118
41	VDD_IO6	2413.30	–1686.08	0.0950118	–0.0663811
42	GPIO_3/FLASH	2413.30	–2029.61	0.0950118	–0.0799059
43	PIXCLK	2413.30	–2203.03	0.0950118	–0.0867335
44	GND_IO5	2256.13	–2503.30	0.0888240	–0.0985551
45	LINE_VALID	2097.06	–2503.30	0.0825614	–0.0985551
46	VDD_IO5	1941.06	–2503.30	0.0764197	–0.0985551

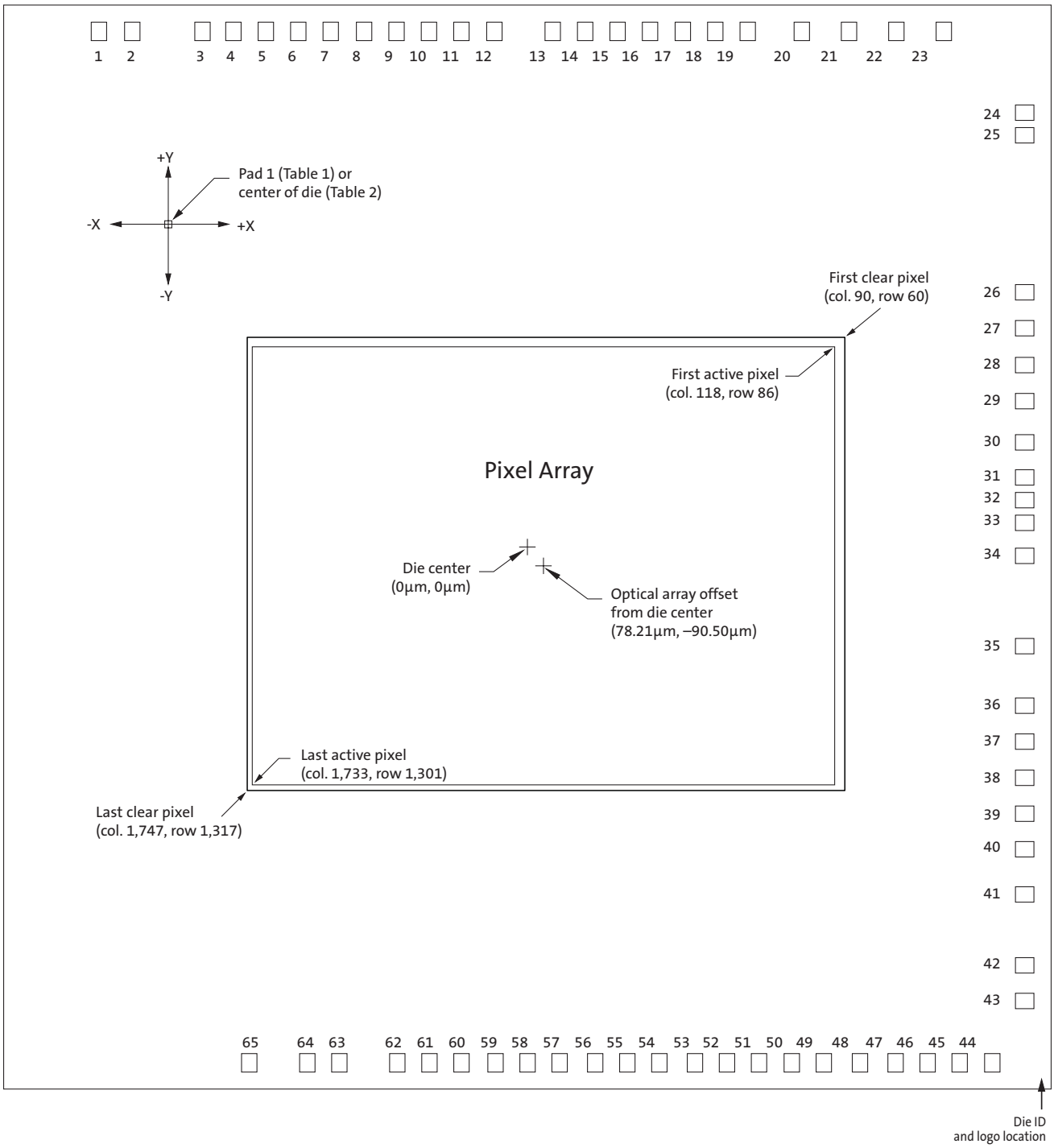
Table 2: MT9D113 Bond Pad Location From Center of Die (0, 0) (continued)

Pad	MT9D113	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
47	FRAME_VALID	1785.06	–2503.30	0.0702780	–0.0985551
48	DOUT7	1611.64	–2503.30	0.0634504	–0.0985551
49	DOUT6	1438.22	–2503.30	0.0566228	–0.0985551
50	GND_IO4	1282.22	–2503.30	0.0504811	–0.0985551
51	DOUT5	1126.22	–2503.30	0.0443394	–0.0985551
52	VDD_IO4	970.22	–2503.30	0.0381976	–0.0985551
53	DOUT4	814.22	–2503.30	0.0320559	–0.0985551
54	DOUT3	640.80	–2503.30	0.0252283	–0.0985551
55	GND_IO3	484.80	–2503.30	0.0190866	–0.0985551
56	DOUT2	328.80	–2503.30	0.0129449	–0.0985551
57	DOUT1	155.38	–2503.30	0.0061173	–0.0985551
58	VDD_IO3	–0.62	–2503.30	–0.0000244	–0.0985551
59	DOUT0	–156.62	–2503.30	–0.0061661	–0.0985551
60	DNU[2]	–319.44	–2503.30	–0.0125764	–0.0985551
61	DNU[2]	–475.44	–2503.30	–0.0187181	–0.0985551
62	VDD2	–631.44	–2503.30	–0.0248598	–0.0985551
63	DGND3	–912.68	–2503.30	–0.0359323	–0.0985551
64	DGND2	–1068.68	–2503.30	–0.0420740	–0.0985551
65	VDD4	–1349.93	–2503.30	–0.0531469	–0.0985551

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 2: Die Outline (Top View)



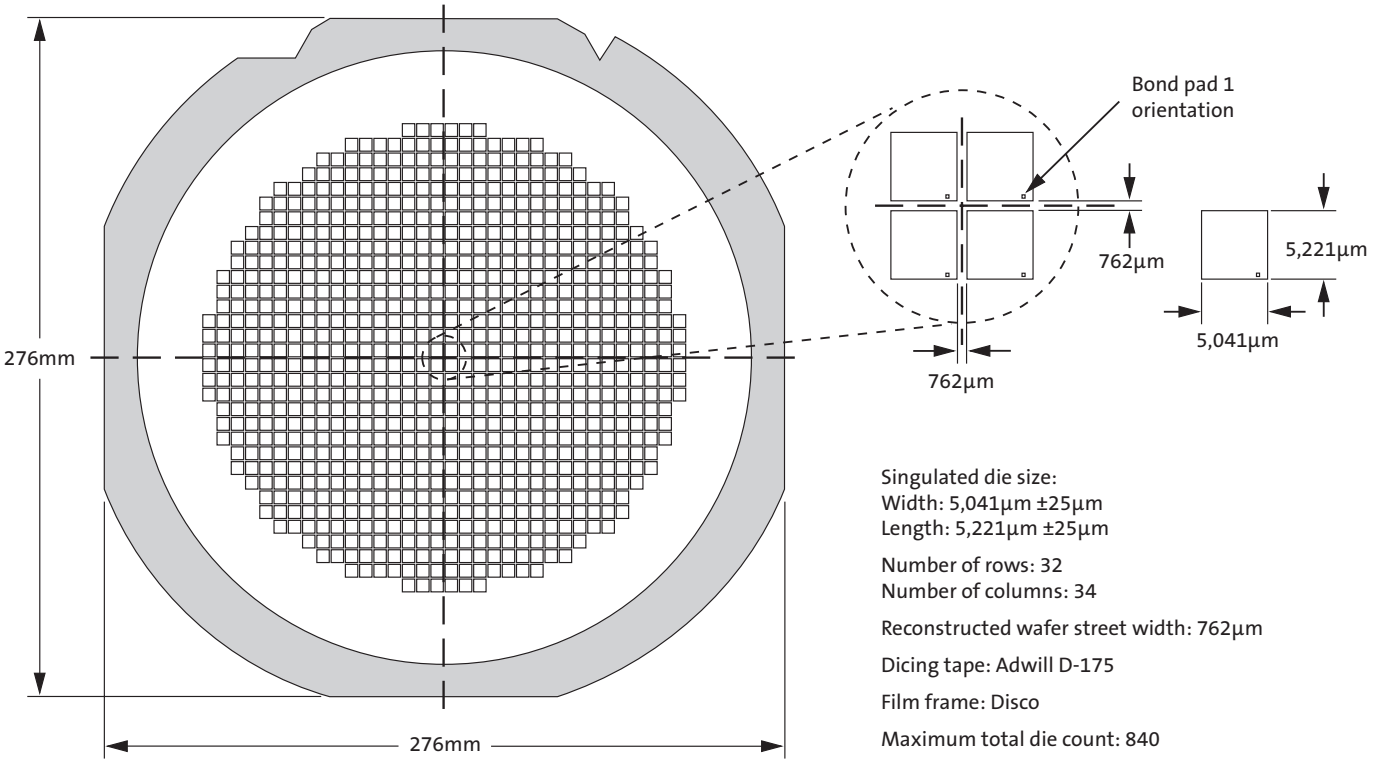
Note: Figure 2 represents physical orientation of the die only. The image projected is flipped horizontally and vertically by the lens.

Physical Specifications

Table 3: Physical Dimensions

Features	Dimensions
Wafer diameter	200mm
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) Width (X dimension): Length (Y dimension):	 5,041µm ±25µm 5,221µm ±25µm
Bond pad size (MIN)	85µm x 100µm
Passivation openings (MIN)	75µm x 90µm
Minimum bond pad pitch between any two bond pads	 110.20µm
Optical array offset Optical center from die center: Optical center from center of pad 1:	 X = 78.21µm, Y = –90.50µm X = 2,157.59µm, Y = –2,593.80µm
First clear pixel (col. 90, row 60) From die center: From center of pad 1:	 X = 1,540.40µm, Y = 1,018.11µm X = 3,619.78µm, Y = –1,485.19µm
First active pixel (col. 118, row 86) From die center: From center of pad 1:	 X = 1,491.36µm, Y = 972.86µm X = 3,570.74µm, Y = –1,530.44µm
Last clear pixel (col. 1,747, row 1,317) From die center: From center of pad 1:	 X = –1,359.55µm, Y = –1,181.62µm X = 719.83µm, Y = –3,684.92µm
Last active pixel (col. 1,733, row 1,301) From die center: From center of pad 1:	 X = –1,334.86µm, Y = –1,153.77µm X = 744.52µm, Y = –3,657.07µm

Figure 3: MT9D113 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 5,041µm ±25µm
Length: 5,221µm ±25µm

Number of rows: 32
Number of columns: 34

Reconstructed wafer street width: 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 840

Revision History

Rev. H 9/10

- Updated to non-confidential

Rev. G 5/10

- Updated to Aptina template

Rev. F, Preliminary 9/08

- Updated Figure 1 on page 4, including notes.
- Added "Decoupling Capacitor Recommendations" on page 5
- Deleted section on product reliability monitors to comply with Aptina template.

Rev. E, Advance 4/08

- Updated to Aptina template.
- Updated to 10-bit parallel interface throughout document.
- Updated notes to Figure 1: "MT9D113 Typical Connections[1] (Single Camera)," on page 4.

Rev. D, Advance 1/08

- Updated singulated die orientation in Table 3 on page 11 and Figure 3 on page 12.

Rev. C, Advance 1/08

- Updated singulated die orientation in Table 3 on page 11 and Figure 3 on page 12.

Rev. B, Advance 11/07

- Added Figure 3: "MT9D113 Die Orientation in Reconstructed Wafer," on page 12.

Rev. A, Advance 09/07

- Initial release.

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