Technical Note

MT9E001 Global Reset Release

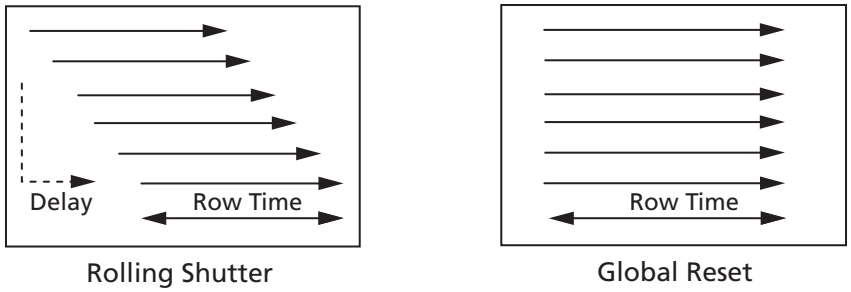
Introduction

This technical note discusses Micron's MT9E001 CMOS image sensor global reset release (GRR) feature.

GRR vs. ERS

The GRR feature enables the active rows in the sensor to be integrated at the same time. This addresses the delay between the first and last row using the electronic rolling shutter (ERS) mode. This delay causes the sensor to capture a fast moving object in one position early in the frame integration and at another position nearer to the end—leaving the resulting image to appear skewed diagonally.

Figure 1: Delay Between the First and Last Row in a Rolling Shutter Image



The delay is the inverse of the maximum frame rate of the sensor at its set resolution. For example, the delay between the start of integration between the first and last row for the MT9E001 8MP sensor—configured to run at full resolution and 10 fps—will be 100ms. Equation 1 shows the formula to calculate image skew.

$$Image\ Skew = 1/fps - blanking\ period \quad \text{(EQ 1)}$$

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Electromechanical Shutter and Flash

The GRR is a sequence consisting of a simultaneous row integration followed by readout. The resulting image is a combination of this sequence. It is important that the light integrated during the readout portion is negligible relative to the integration sequence. For this reason, the use of an electromechanical shutter and/or flash is recommended. The summation of the GRR frame is shown in Equation 2.

$$GRR_{Frame} = Integration + Readout \quad \text{(EQ 2)}$$

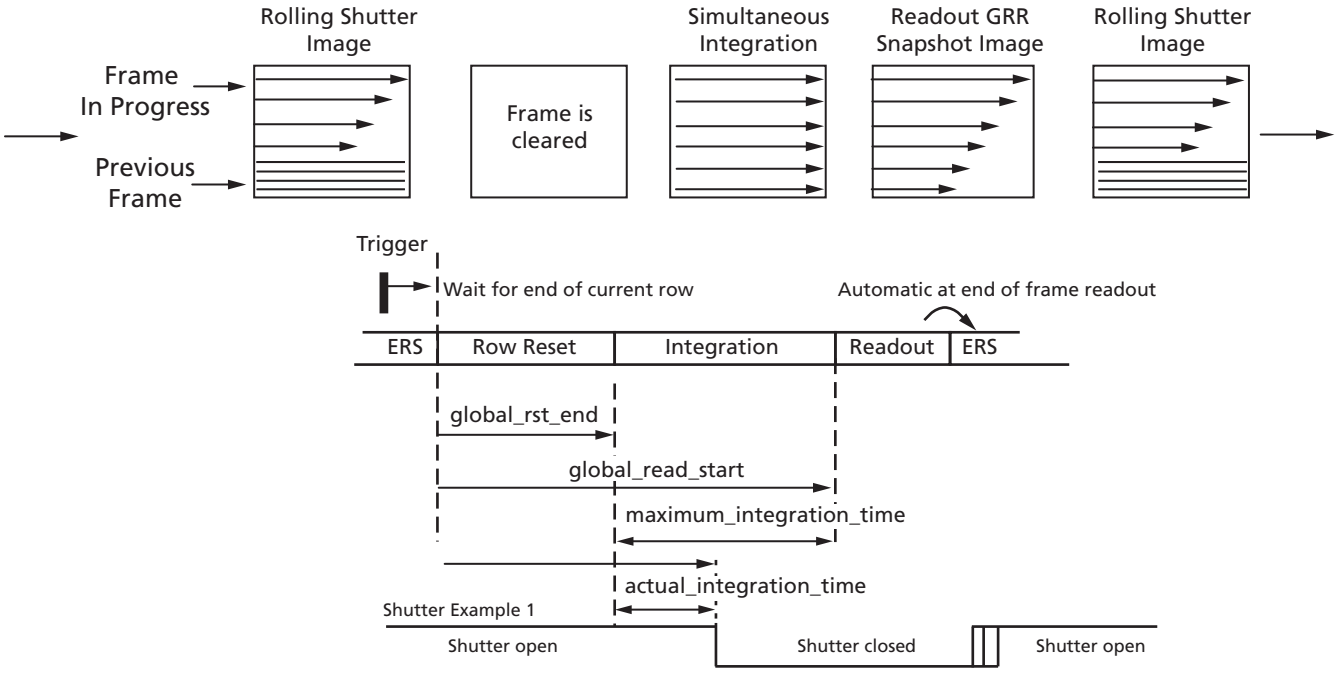
GRR Sequence

The GRR sequence will be triggered while the sensor is streaming in ERS mode. A trigger will interrupt a rolling shutter sequence in mid-frame.

The basic elements of the GRR sequence are:

1. A GRR sequence is triggered.
2. All of the rows of the pixel array are placed in reset.
3. All of the rows of the pixel array are taken out of reset simultaneously.
4. All of the rows of the pixel array start to integrate incident light.
5. After the desired integration time, the electromechanical shutter is closed.
6. A single output frame is generated by the sensor, with the LINE_VALID (LV), FRAME_VALID (FV), PIXCLK, and DOUT timing.
7. When the output frame is complete (FV negates) the electromechanical shutter may be opened again. The sensor automatically resumes operation in ERS mode.

Figure 2: Outline of GRR Sequence



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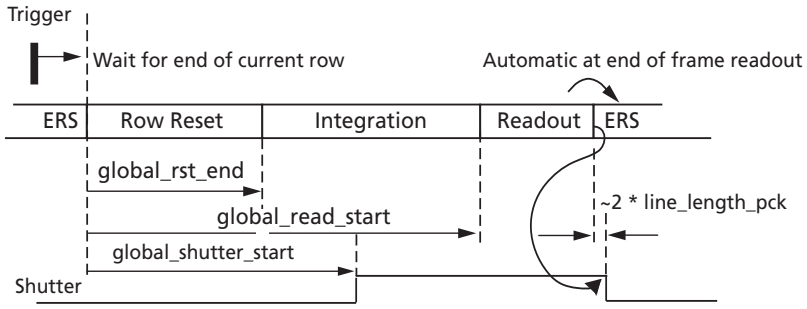
GRR Register Configuration

The global shutter timing is configured by the timing or the row readout and the assertion of the shutter output. A GRR sequence can be triggered either by a register WRITE to R0x3160[0] or by a rising edge on a suitably configured general purpose input (GPI). If the GRR is configured to use a hardware trigger, the beginning of the readout sequence will be triggered by the falling edge of the GPI.

The registers used to adjust the timing of the GRR are:

- Global reset end (global_rst_end)
  Controls the duration of the row reset phase.
- Global read start (global_read_start)
  Controls the delay before the start of the readout phase after the GRR sequence has begun.
- Global shutter start (global_shutter_start)
  Controls the delay before the SHUTTER signal is driven HIGH. This signal can be used to close the mechanical shutter to regulate the exposure time of the GRR snapshot image.

Figure 3: Programming of GRR using Registers



The integration time of the GRR sequence is defined as:

$$Integration = \frac{(global\_read\_start - global\_rst\_end)\ x\ 512}{vt\_pix\_clk\_freq\_mhz} \quad \text{(EQ 3)}$$

When programming the sensor registers, these rules should be followed:

1. The recommended registers included in Table 3 on page 12 should be used.
2. global_read_start > global_rst_end.
3. global_read_start > global_shutter_start.

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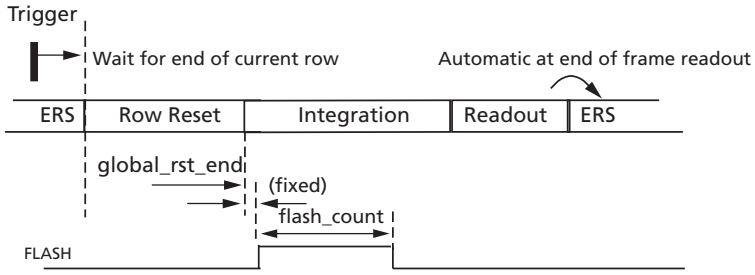
Flash and SHUTTER

The flash can be enabled by setting global_seq_trigger[2] = 1. When a GRR sequence is triggered, the FLASH output signal will be pulsed during the integration phase of the GRR sequence. The FLASH output will assert a fixed number of cycles after the start of the integration phase and will remain asserted for a time that is controlled by the value of the flash_count (R0x3048).

This register controls the length of the flash pulse when xenon flash is enabled. The value specifies the length in units of 256 x PIXCLK cycle increments (by default, PIXCLK = system_clock). When the xenon count is set to its maximum value (0x3FF), the flash pulse will automatically be truncated prior to the readout of the first row, giving the longest pulse possible.

Figure 4: Programming of FLASH and GRR



SHUTTER is negative by default. The point at which it asserts is controlled by the programming of global_shutter_start. At the end of the global reset readout phase, SHUTTER will switch to negative again approximately (2 * line_length_pck) after the negation of FV.

GRR Trigger

The GRR can be configured using a register setting. The register settings will only allow up to 174ms. The hardware GPI can be used to run up to 2 seconds.

Instructions to configure the hardware GRR trigger:

1. Enable the GPI feature on the sensor (R0x301A [8] = 1).
2. Configure a specific GPI pin to use the GRR trigger ((R0x3026 [9:7]).
   - 2a. 0 – GPI #0
   - 2b. 1 – GPI #1
   - 2c. 2 – GPI #3
   - 2d. 3 – GPI #4

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Schematic Design

The specific current draw from the GRR can be mitigated by using a 10µf capacitor placed in parallel with VAA. Electrical measurements of the GRR sequence show that the power supply fluctuations are reasonable.

Figure 5: Electrical Measurements for the GRR Sequence

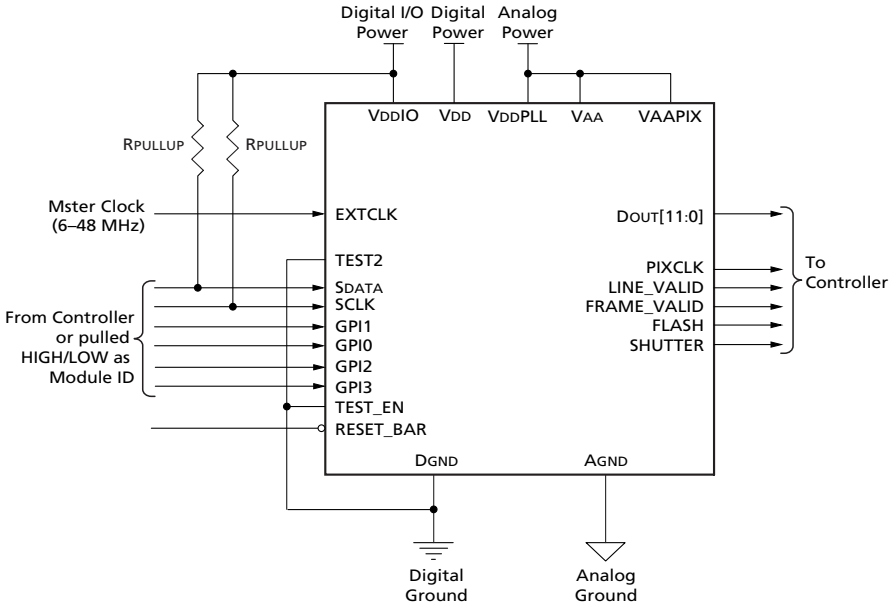

Table 1: Electrical Measurement for the GRR Sequence

Symbol	ERS		Global Shutter		Difference		Unit
	Min	Max	Min	Max	Min	Max	
IDD	38.253	42.077	38.242	42.483	-0.011	0.406	mA
IAA	95.094	95.265	95.082	95.273	-0.012	0.008	mA
IAA_PIX	0.757	0.847	0.360	0.849	0.004	0.002	mA

Scope Plots

The use-case of the GRR snapshot is:

1. A switch from a preview mode to full resolution.
2. A GRR sequence.

The switch from preview to full resolution mode can typically be made without a change to the sensor's PLL configuration. The set of changes required for this mode can be made simultaneously using the group parameter hold feature.

Following the mode switch to full resolution, the GRR sequence can be triggered at the beginning of the output of the first ERS frame. This can be tracked using FV.

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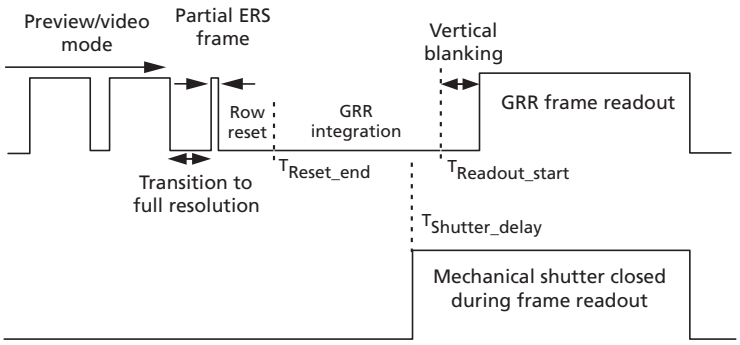
Figure 6: Explanation of FV and SHUTTER with GRR Scope Plot



FV will remain LOW during the row reset and integration sequence of the GRR sequence. SHUTTER will not be raised before FV indicates the frame readout. This is due to a specific vertical blanking period of 80 rows between the integration and readout sequence. SHUTTER may be asserted earlier depending on whether the global_shutter_start register value is configured to be less than global_read_start.

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Register Description

Table 2: Manufacturer-Specific Register Settings

Reg. #	Bits	Default	Name	Frame Sync'd	Bad Frame
R12314 R0x301A	**15:0**	**0x0058**	**reset_register (RW)**		
	15	0x0000	Grouped Parameter Hold 0 = Update of many of the registers is synchronized to frame start. 1 = Inhibit register updates; register changes will remain pending until this bit is returned to "0." When this bit is returned to "0," all pending register updates will be made on the next frame start.	N	N
	14:13	X	Reserved		
	12	0x0000	Reserved Not used.	N	N
	11	X	Reserved		
	10	0x0000	Restart Bad Frames 1 = A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	Mask Bad Frames 0 = The sensor will produce bad (corrupted) frames as a result of some register changes. 1 = Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	GPI Enable 0 = The primary input buffers associated with the GPI[0], GPI[1], GPI[2], and GPI[3] inputs are powered down and the GPI cannot be used. 1 = The input buffers are enabled and can be read through R0x3026–7.	N	N

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Table 2: Manufacturer-Specific Register Settings (continued)

Reg. #	Bits	Default	Name	Frame Sync'd	Bad Frame
R12314 R0x301A	7	0x0000	Parallel Enable 0 = The parallel data interface (DOUT[11:0], LV, FV, and PIXCLK) is disabled and the outputs are placed in a High-Z state. 1 = The parallel data interface is enabled. The output signals can be switched between a driven and a High-Z state using output enable control.	N	N
	6	0x0001	Drive Pins 0 = The parallel data interface (DOUT[11:0], LV, FV, and PIXCLK) may enter a High-Z state (depending upon the configuration of R0x3026). 1 = The parallel data interface is driven. This bit is "Don't Care" unless bit[7] = 1.	N	N
	5	X	Reserved		
	4	0x0001	Standby EOF 0 = Transition to standby is synchronized to the end of a sensor row readout (held off until LV has fallen). 1 = Transition to standby is synchronized to the end of a frame.	N	Y
	3	0x0001	Lock Reg Many SMIA registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	Stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N
R12314 R0x301A	1	0x0000	Restart This bit always reads as "0." Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	Y
	0	0x0000	Reset This bit always reads as "0." Setting this bit initiates a reset sequence (the frame being generated will be truncated).	N	Y

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Table 2: Manufacturer-Specific Register Settings (continued)

Reg. #	Bits	Default	Name	Frame Sync'd	Bad Frame
R12326 R0x3026	12:10	0x0007	OE_N Pin Select Associate the output enable function with an active LOW input pin 0 = Associate with GPI[0] 1 = Associate with GPI[1] 2 = Associate with GPI[2] 3 = Associate with GPI[3] 4–6 = Reserved 7 = Output enable function is not controlled by any pin Must be set to 7 if reset[8] = 0.	N	N
	9:7	0x0007	Trigger Pin Select Associate the trigger function with an active HIGH input pin 0 = Associate with GPI[0] 1 = Associate with GPI[1] 2 = Associate with GPI[2] 3 = Associate with GPI[3] 4–6 = Reserved 7 = Trigger function is not controlled by any pin Must be set to 7 if R0x301A–B[8] = 0.	N	N
	6:4	0x0007	SADDR Pin Select Associate the SADDR function with an active HIGH input pin 0 = Associate with GPI[0] 1 = Associate with GPI[1] 2 = Associate with GPI[2] 3 = Associate with GPI[3] 4–6 = Reserved 7 = SADDR function is not controlled by any pin Must be set to 7 if R0x301A–B[8] = 0.	N	N

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Table 2: Manufacturer-Specific Register Settings (continued)

Reg. #	Bits	Default	Name	Frame Sync'd	Bad Frame
R12326 R0x3026	3	RO	GPI3 Read-only. Return the current state of the GPI[3] input pin. Invalid if R0x301A–B[8] = 0.	N	N
	2	RO	GPI2 Read-only. Return the current state of the GPI[2] input pin. Invalid if R0x301A–B[8] = 0.	N	N
	1	RO	GPI1 Read-only. Return the current state of the GPI[1] input pin. Invalid if R0x301A–B[8] = 0.	N	N
	0	RO	GPI0 Read-only. Return the current state of the GPI[0] input pin. Invalid if R0x301A–B[8] = 0.	N	N
	0	0x0000	Horizontal Mirror 0 = Normal readout 1 = Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order (see R0x3024).	Y	YM
R12360 R0x3048	**15:0**	**0x0008**	**flash_count (RW)**	N	N
	Length of flash pulse when xenon flash is enabled. The value specifies the length in units of 256 * PIXCLK cycle increments (by default, PIXCLK = system_clock). When the xenon count is set to its maximum value (0x3FF), the flash pulse will automatically be truncated prior to the readout of the first row, giving the longest pulse possible.				
R12640 R0x3160	**15:0**	**0x0000**	**global_seq_trigger (RW)**		
	15:10	X	Reserved		
	9	RO	Grst Rd Read-only. Global reset read sequence indicator.	N	N
	8	RO	Grst Sequence Read-only. GRR sequence indicator.	N	N
	7:3	X	Reserved		
	2	0x0000	Global Flash 0 = When a GRR sequence is triggered, the FLASH output will remain negated. 1 = When a GRR sequence is triggered, the FLASH output will pulse during the integration phase.	N	Y

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Table 2: Manufacturer-Specific Register Settings (continued)

Reg. #	Bits	Default	Name	Frame Sync'd	Bad Frame
R12640 R0x3160	1	0x0000	Global Bulb 0 = Shutter open is triggered from bit[0] and shutter close is timed from the trigger point. 1 = Shutter open and close are triggered from bit[0]. This corresponds to the shutter "B" setting on a traditional camera, where "B" originally stood for "Bulb" (the shutter setting used for synchronization with a magnesium foil flash bulb) and was later considered to stand for "Brief" (an exposure that was longer than the shutter could automatically accommodate).	N	Y
	0	0x0000	Global Trigger When bit[1] = 0, a 0-to-1 transition of this bit initiates (triggers) a GRR sequence. When bit[1] = 1, a 0-to-1 transition of this bit initiates a GRR sequence, and leaves the shutter open; a 1-to-0 transition of this bit closes the shutter. These operations can also be controlled from the signal interface by enabling one of the GPI[3:0] signals as a trigger input.	N	Y
R12642 R0x3162	**15:0**	**0x0050**	**global_rst_end (RW)**	N	N
	Controls the duration of the global reset row reset phase. A value of N gives a duration of N * 512 / vt_pix_clk_freq_mhz.				
R12644 R0x3164	**15:0**	**0x0078**	**global_shutter_start (RW)**	N	N
	Controls the delay before the assertion of the SHUTTER output during a GRR sequence. A value of N gives an assertion time of N * 512 / vt_pix_clk_freq_mhz timed from the end of row that was in progress when the GRR sequence was triggered.				
R12646 R0x3166	**15:0**	**0x00A0**	**global_read_start (RW)**	N	N
	Controls the delay before the start of the global reset readout phase (equivalent to the end of global reset integration phase). A value of N gives a delay of N * 512 / vt_pix_clk_freq_mhz. The integration time is given by (global_read_start - global_rst_end) * 512 / vt_pix_clk_freq_mhz.				

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Register Settings

Table 3: MT9E001

Register Address	Recommended Value	Description
0x309A[10]	1	Reserved
0x309A[13]	1	Reserved
0x3158	0x97C7	Reserved
0x315A	0x97C6	Reserved
0x3162	0x074C	global_rst_end
0x3154	0x1482	Reserved
0x3156	0x1C81	Reserved

Conclusion

For more information on GRR, or for additional features, refer to the MT9E001 CMOS digital image sensor data sheet on Micron's Web site at www.micron.com/imaging.

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Revision History

Rev. B **08/21/2007**

- Update Table 3, “MT9E001,” on page 12

Rev. A **04/04/2007**

- Initial release.

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