MT9M001 Register Reference

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

MT9M001 Register Reference

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Introduction

This reference document describes the MTM001registers and variables. Summary and detailed information are presented in separate sections:

- “Register List and Default Values” on page 5
- “Register Description” on page 6

Note: Througout this document, Green1 to corresponds to greenB; green2 corresponds to greenB.

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the MT9M001 data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to “1.”

Registers

Register Map

Table 1: Register List and Default Values

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x00	Chip Version	1000 0100 0001 0001	0x8431
0x01	Row Start	0000 0ddd dddd dddd	0x000C
0x02	Column Start	0000 0ddd dddd dddd	0x0014
0x03	Row Size (Window Height)	0000 0ddd dddd dddd	0x03FF
0x04	Col Size (Window Width)	0000 0ddd dddd dddd	0x04FF
0x05	Horizontal Blanking	0000 0ddd dddd dddd	0x0009
0x06	Vertical Blanking	0000 0ddd dddd dddd	0x0019
0x07	Output Control	0000 0000 0d00 00dd	0x0002
0x09	Shutter Width	00dd dddd dddd dddd	0x0419
0x0B	Restart	0000 0000 0000 000d	0x0000
0x0C	Shutter Delay	0000 0ddd dddd dddd	0x0000
0x0D	Reset	0000 0000 0000 000d	0x0000
0x1E	Read Options 1	1000 dddd 00dd dd00	0x8000
0x20	Read Options 2	dd01 0dd1 d00d d10d	0x1104
0x2B	Even Row, Even Column	0000 0000 0ddd dddd	0x0008
0x2C	Odd Row, Even Column	0000 0000 0ddd dddd	0x0008
0x2D	Even Row, Odd Column	0000 0000 0ddd dddd	0x0008
0x2E	Odd Row, Odd Column	0000 0000 0ddd dddd	0x0008
0x35	Global Gain	0000 0000 0ddd dddd	0x0008
0x5F	Cal Threshold	dddd dddd d0dd dddd	0x0904
0x60	Even Row, Even Column	0000 000d dddd dddd	0x0000
0x61	Odd Row, Odd Column	0000 000d dddd dddd	0x0000
0x62	Cal Ctrl	d00d d100 1001 1ddd	0x0498
0x63	Even Row, Odd Column	0000 000d dddd dddd	0x0000
0x64	Odd Row, Even Column	0000 000d dddd dddd	0x0000
0xF1	Chip Enable	0000 0000 0000 00dd	0x0001

Note: 1 = always 1
0 = always 0
d = programmable

Table 2: Register Description

Register	Bit	Description
Chip ID		
0x00	15:0	This register is read-only and gives the chip identification number: 0x8431.
Window Control These registers control the size of the window.		
0x01	10:0	First row to be read out—default = 0x000C (12).
0x02	10:0	First column to be read out—default = 0x0014 (20). Register value must be an even number.
0x03	10:0	Window height (number of rows - 1)—default = 0x03FF (1023). Minimum value for 0x03 = 0x0002.
0x04	10:0	Window width (number of columns - 1)—default = 0x04FF (1279). Register value must be an odd number. Minimum value for 0x04 = 0x0003.
Blanking Control These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using Table 4, “Frame Timing,” on page 11 of the data sheet.		
0x05	10:0	Horizontal Blanking—default = 0x0009 (9 pixels).
0x06	10:0	Vertical Blanking—default = 0x0019 (25 rows).
Output Control This register controls various features of the output format for the sensor.		
0x07	0	Synchronize changes (copied to Reg0xF1, bit1). 0 = normal operation. Update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip or row mirror) at the next frame boundary. The “frame boundary” is 8 row_times before the rising edge of FRAME_VALID. (If “Show Dark Rows” is set, it will be coincident with the rising edge of FRAME_VALID.) 1 = do not update any changes to these settings until this bit is returned to “0.”
	1	Chip Enable (copied to Reg0xF1, bit0). 1 = normal operation. 0 = stop sensor readout. When this is returned to “1,” sensor readout restarts at the starting row in a new frame. The digital power consumption can then also be reduced to less than 5uA by turning off the master clock.
	2	Reserved—default is 0; set to zero at all times.
	3	Reserved—default is 0; set to zero at all times.
	6	Use Test Data. When set, a test pattern will be output instead of the sampled image from the sensor array. The value sent to the DOUT[9:0] pins will alternate between the Test Data register (Reg0x32) in even columns and the inverse of the Test Data register for odd columns. The output “image” will have the same width, height, and frame rate as it would otherwise have. No digital processing (gain or offset) is applied to the data. When clear (the default), sampled pixel values are output normally.

Table 2: Register Description (continued)

Register	Bit	Description
Pixel Integration Control These registers (along with the window sizing and blanking registers) control the integration time for the pixels. The actual total integration time (^{t}INT) is: ^{t}INT = Reg0x09 x row time - overhead time - reset delay, where: Row time = ((Reg0x04 + 1) + 244 + Reg0x05 - 19) pixel clock periods Overhead time = 180 pixel clock periods Reset delay = 4 x Reg0x0C pixel clock periods If the value in Reg0x0C exceeds (row time - 548)/4 pixel clock cycles, the row time will be extended by (4 x Reg0x0C - (row time - 548)) pixel clock cycles. In this expression, the row time term, Reg0x09 x ((number of columns) + 244 + horizontal blanking register - 19), corresponds to the number of rows integrated. The overhead time (180 pixel clocks) is the overhead time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay. Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows) such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9M001 will add additional blanking rows as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means ^{t}INT must be a multiple of 1/120 of a second. Under 50Hz flicker, ^{t}INT must be a multiple of 1/100 of a second.		
0x09	13:0	Number of rows of integration—default = 0x0419 (1049).
0x0C	10:0	Shutter delay—default = 0x0000 (0). This is the number of master clocks times four that the timing and control logic waits before asserting the reset for a given row.
Frame Restart		
0x0B	0	Setting bit 0 to “1” of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for Reg0x20, bit0).
Reset		
0x0D	0	This register is used to reset the sensor to its default, power-up state. To put the MT9M001 in reset mode first write a “1” into bit 0 of this register, then write a “0” into bit 0 to resume operation.

Table 2: Register Description (continued)

Register	Bit	Description
Read Mode 1 In read mode 1, this register is used to control many aspects of the readout of the sensor.		
0x1E	0	Reserved—default is 0; set to zero at all times.
	1	Reserved—default is 0; set to zero at all times.
	2	Column Skip 4—default is 0 (disable). 1 = enable.
	3	Row Skip 4—default is 0 (disable). 1 = enable.
	4	Column Skip 8—default is 0 (disable). 1 = enable.
	5	Row Skip 8—default is 0 (disable). 1 = enable.
	6	Reserved—default is 0; do not change.
	7	Reserved—default is 0; do not change.
	8	Snapshot Mode—default is 0 (continuous mode). 1 = enable (wait for TRIGGER; TRIGGER can come from outside signal (TRIGGER pin on the sensor) or from serial interface register restart, i.e. programming a "1" to bit 0 of Reg0x0B.
	9	STROBE Enable—default is 0 (no STROBE signal). 1 = enable STROBE (signal output from the sensor during the time all rows are integrating. See STROBE width for more information).
	10	STROBE Width—default is 0 (STROBE signal width at minimum length, 1 row of integration time, prior to line valid going HIGH). 1 = extend STROBE width (STROBE signal width extends to entire time all rows are integrating).
	11	Strobe Override—default is 0 (STROBE signal created by digital logic). 1 = override STROBE signal (STROBE signal is set HIGH when this bit is set, LOW when this bit is set LOW. It is assumed that STROBE enable is set to "0" if STROBE override is being used).
	12	Reserved—default is 0; do not change.
	13	Reserved—default is 0; do not change.
	14	Reserved—default is 0; do not change.
	15	Reserved—default is 1; do not change.
Gain Settings The gain is individually controllable for each of the four groups of pixels that lie in odd rows and columns, even rows and columns, odd rows and even columns, and even rows and odd columns. This is shown in the register chart. Formula for gain setting: Gain ≤ 8 Gain = (bit[6] + 1) x (bit[5-0] x 0.125) Gain > 8 (bit[6] = 1 and bit[5] = 1) Gain = 8.0 + bit[2-0] Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings: Gain — Increments — Recommended Settings 1.000 to 4.000 — 0.125 — 0x08 to 0x20 4.25 to 8.00 — 0.25 — 0x51 to 0x60 9.0 to 15.0 — 1.0 — 0x61 to 0x67		
0x2B	6:0	Even row, even column—default = 0x08 (8) = 1x gain.
0x2C	6:0	Odd row, even column—default = 0x08 (8) = 1x gain.
0x2D	6:0	Even row, odd column—default = 0x08 (8) = 1x gain.

Table 2: Register Description (continued)

Register	Bit	Description
0x2E	6:0	Odd row, odd column—default = 0x08 (8) = 1x gain.
0x35	6:0	Global gain—default = 0x08 (8) = 1x gain. This register can be used to set all four gains at once.
Test Data		
0x32	11:2	Test Data. The value used to produce a test pattern in "Use Test Data" mode (Reg0x07 bit 6).
Read Mode 2 This register is used to control many aspects of the readout of the sensor.		
0x20	0	No bad frames—1 = output all frames (including bad frames). 0 (default) = only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
	1	Reserved—default is 0; do not change.
	2	Reserved—default is 1; set to "1" at all times.
	3	Column skip—1= read out two columns, and then skip two columns (for example, col 0, col 1, col 4, col 5...). 0 = normal readout (default).
	4	Row skip—1 = read out two rows, and then skip two rows (for example, row 0, row 1, row 4, row 5...). 0 = normal readout (default).
	5	Reserved—default is 0; do not change.
	6	Reserved—default is 0; set to zero at all times.
	7	Flip Row—1 = readout starting 1 row later (alternate color pair). 0 (default) = normal readout.
	8	Reserved—default is 1; set to "1" at all times.
	9	1 = "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking). 0 = normal LINE_VALID (default, no LINE_VALID during vertical blanking).
	10	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9.
	11	Reserved—default is 0; do not change.
	12	Reserved—default is 1; do not change.
	13	Reserved—default is 0; do not change.
	14	Reserved—default is 0; do not change.
	15	Mirror Row—1 = read out from bottom to top (upside down). 0 (default) = normal readout (top to bottom).
Test Data		
0x32	11:2	Test Data. The value used to produce a test pattern in "Use Test Data" mode (Reg0x07 bit 6).
Black Level Calibration These registers are used in the black level calibration. Their functionality is described in detail in the next section.		
0x5F	5:0	Thres_lo—Lower threshold for black level in ADC LSBs—default = 000100.
	7	1 = override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14:8; Thres_lo always = bits 5:0). Default = 0 = Automatic Thres_hi and Thres_lo adjustment.
	14:8	Thres_hi—Maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1; black level maximum is reset to this value after every black level average restart if bit 15 = 1 and bit 7 = 0.
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5:0, Thres_hi is reset to the programmed value (bits 14:8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically, as described above.

Table 2: Register Description (continued)

Register	Bit	Description
0x60	8:0	Even row, even column—analog offset correction value for even row, even column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x61	8:0	Odd row, odd column—analog offset correction value for odd row, odd column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x62	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).
	2:1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1= disable black level correction (Offset Correction Voltage = 0.0V). (In this case, no black level correction is possible).
	4:3	Reserved—default is 1; do not change.
	6:5	Reserved—default is 0; do not change.
	7	Reserved—default is 1; do not change.
	9:8	Reserved—default is 0; do not change.
	10	Reserved—default is 1; do not change.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	14:3	Reserved—default is 0; set to zero at all times.
	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
0x63	8:0	Even row, odd column—analog offset correction value for even row, odd column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x64	8:0	Odd row, even column—analog offset correction value for odd row, even column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
Chip Enable and Two-Wire Serial Interface Write Synchronize.		
0xF1	0	Mirrors the functionality of Reg0x07 bit1 (Chip Enable). 1 = normal operation. 0 = stop sensor readout; when this is returned to "1," sensor readout restarts at the starting row in a new frame.

Table 3: Black Level Registers

Register	bit	Description
Reg0x5F This register controls the operation of the black level calibration thresholds.		
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5:0, Thres_hi is reset to the programmed value (bits 14:8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically as described below.
	14:8	Thres_hi—maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1, black level maximum is reset to this value after every black level average restart if bit 15 = 1 and bit 7 = 0.
	7	1 = override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14:8, Thres_lo always = bits 5:0). 0 = automatic Thres_hi and Thres_lo adjustment.
	5:0	Thres_lo—Lower threshold for black level in ADC LSBs. Under default automatic operation (bit 7 = 0, bit 15 = 0), Thres_lo = $RegGain_{max}$/4 x ($RegGain_{max}$, bit 6 +1) x ($RegGain_{max}$, bit 7 +1), where $RegGain_{max}$ is the maximum of the four independent gain register settings. Whenever a jump in the calibration causes the black level data to change from below Thres_lo to above Thres_hi, Thres_hi is adjusted according to the following: If new black level < 64: Thres_hi = Thres_lo + 2 + (2 x Delta), where Delta = new black level - Thres_lo If new black level > 63 and < 119: Thres_hi = new black level + 4 If new black level > 119: Thres_hi = 123 After any recalculation of the black level and average restart, Thres_hi is reset to either Thres_lo + 5 (automatic, default mode), Thres_hi (bit 7 = 1). Reg0x62, bit 11 will override this.
Reg0x62 This register is used to control the automatic black level calibration circuitry.		
	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
	14	Reserved—default is 0; do not change.
	13	Reserved—default is 0; do not change.
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	10:3	Reserved—default is 1; do not change.
	2:1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1 = disable black level correction (Offset Correction Voltage = Skew Voltage = 0.0V). (In this case, no black level correction is possible).
	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).

Table 3: Black Level Registers (continued)

Register	bit	Description
Reg0x60, Reg0x61, Reg0x63, Reg0x64		These registers contain the 9-bit signed black level calibration values. In normal operation, these values are calculated at the beginning of each frame. However, if Reg0x62, bit 0 is set to "1," these registers can be written to, overriding the automatic black level calculation. This feature can be used in conjunction with readout of the black rows (Reg0x20, bit 11) if the user would like to use an external black level calibration circuit. The offset correction voltage is generated according to the following formula: Offset Correction Voltage = (9-bit signed calibration value, -256 to 255) x (2mV x Enable bit) two's complement, if bit 8 = 1, Offset = bits [0:7] - 256 ADC input voltage = Pixel Output Voltage x Analog Gain - Offset Correction Voltage

Revision History

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- Copied register tables from data sheet to new document

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