1/4.5-Inch 1.6Mp CMOS Digital Image Sensor

MT9M002 Data Sheet Addendum

Refer to the MT9M002 data sheet on Aptina's Web site: www.aptina.com.

Introduction

This document supplements Aptina's MT9M002 advance data sheet (Revision B) with an update to the typical parallel configuration schematic. The standard CMOS digital image sensor data sheet should be referenced for a complete description of this 1/4.5-inch 1.6Mp image sensor. The specifications contained in this addendum supersede the specifications listed in the referenced CMOS digital image sensor data sheet.

Addendum Changes

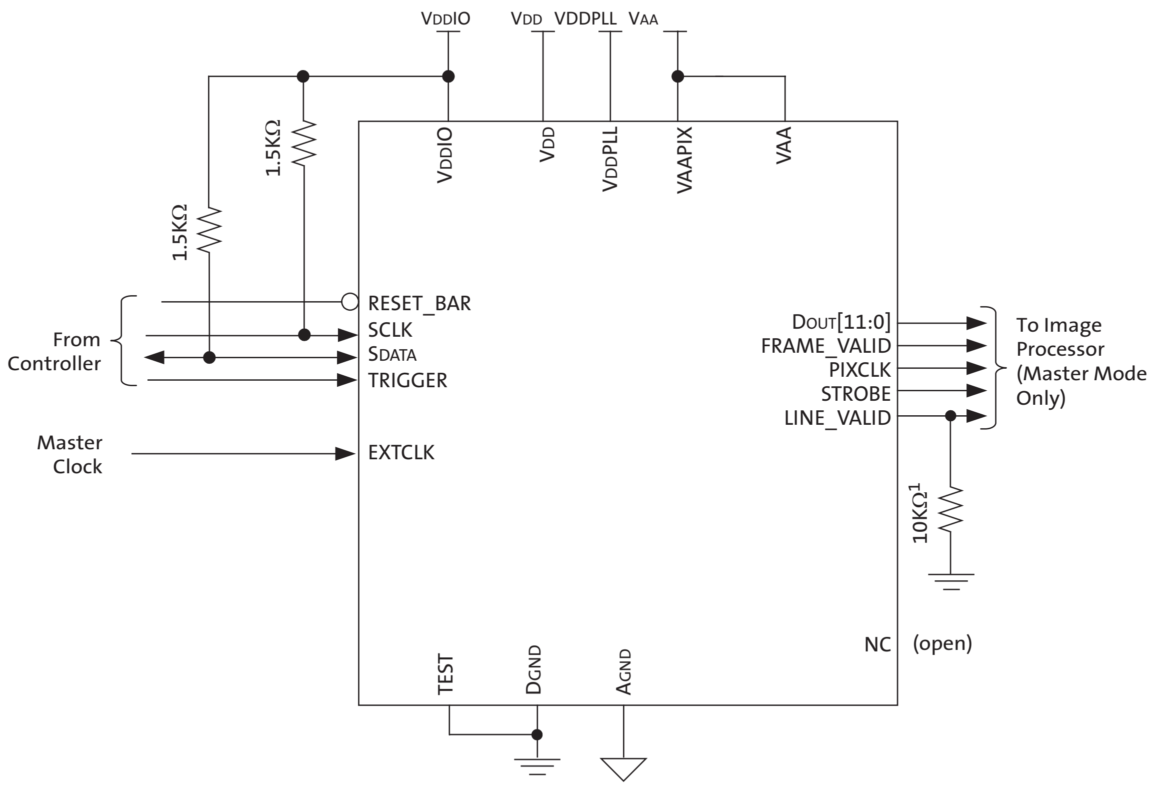
This addendum supplements Table 3, "Signal Descriptions," on page 8 and Figure 3: "Typical Configuration – Parallel Connection," on page 10 of the MT9M002 Advance data sheet.

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Aptina without notice. Products are only warranted by Aptina to meet Aptina's production data sheet specifications.

Table 1: Signal Descriptions

Name	Type	Description
SCLK	Input	Serial clock. Connected externally through a resistor to VDD_IO. Typically the resistor value is 1.5KΩ but may vary depending on the system configuration and bus loading.
LINE_VALID	Output	Line valid output. Qualified by PIXCLK. Driven HIGH with active pixels of each line and LOW during horizontal blanking periods. External pull-down resistor to DGND (typically 10K-100KΩ) required for proper initialization sequence.

Figure 1: Typical Configuration – Parallel Connection



Note: 1. External pull-down resistor to DGND (typically 10K-100KΩ) required for proper initialization.

Revision History

Rev. C 5/11

- Updated trademarks
- Applied updated template

Rev. B 8/10

- Updated to Aptina template

Rev. A 5/07

- Initial release

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