MT9M024 and MT9M034 Registers

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

MT9M024 and MT9M034 Register Reference

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Introduction

This register reference is provided for engineers who are designing cameras that use the MT9M024 and MT9M034.

Register Address Space

The MT9M024 and MT9M034 provide a 16-bit register address space accessed through a serial interface. Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1.

Table 1: Address Space Regions

Address Range	Description
0x0000–0x0FFF	Reserved
0x1000–0x1FFF	Reserved
0x2000–0x2FFF	Reserved
0x3000–0x3FFF	Manufacturer-specific registers (read-only and read-write dynamic registers)
0x4000–0xFFFF	Reserved

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The MT9M024 and MT9M034 use 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 8-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Register Aliases

A consequence of the internal architecture of the MT9M024 and MT9M034 is that some registers are decoded at multiple addresses. Some registers in “configuration space” are also decoded in “manufacturer-specific space.” To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0000–1 is model_id, and R0x3000–1 is model_id_. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the model_id register are referred to as model_id[3:0] or R0x0000–1[3:0].

Byte Ordering

Registers that occupy more than 1 byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the bus. For example, the model_id register is R0x0000–1. In the register table the default value is shown as 0x2400. This means that a READ from address 0x0000 would return 0x24, and a READ from address 0x0001 would return 0x00. When reading this register as two 8-bit transfers on the serial interface, the 0x26 will appear on the serial interface first, followed by the 0x00.

Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses, and registers that occupy four bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2: Data Formats

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = –128, 0xFFFF = –0.0039065
UFIX16	Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from “read-only,” “read/write,” and “read, write-1-to-clear.”

Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing x_addr_start partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the MT9M024 and MT9M034 double-buffers many registers by implementing a “pending” and a “live” version. READs and WRITEs access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the “Sync’d” column shows which registers or register fields are double-buffered in this way.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.
Y—Yes. Changing the register value might produce a bad frame.
YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to “1.”

Register Summary Table

Note: Green1 (G1) corresponds to greenR (Gr); green2 (G2) corresponds to greenB (Gb).

Caution **Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.**

Manufacturer-Specific Register List and Default Values

Table 3: Manufacturer-Specific Register List and Default Values
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	9216 (0x2400)
R12290 (R0x3002)	y_addr_start	0000 00dd dddd dddd	2 (0x0002)
R12292 (R0x3004)	x_addr_start	0000 0ddd dddd dddd	0 (0x0000)
R12294 (R0x3006)	y_addr_end	0000 00dd dddd dddd	965 (0x03C5)
R12296 (R0x3008)	x_addr_end	0000 0ddd dddd dddd	1283 (0x0503)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	990 (0x03DE)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd ddd0	1650 (0x0672)
R12302 (R0x300E)	revision_number	dddd dddd	65 (0x41)
R12304 (R0x3010)	lock_control	dddd dddd dddd dddd	48879 (0xBEEF)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
R12308 (R0x3014)	fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12312 (R0x3018)	fine_integration_time_cb	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	88 (0x0058)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	168 (0x00A8)
R12326 (R0x3026)	gpi_status	0000 0000 0000 ????	0 (0x0000)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 dddd dddd	6 (0x0006)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	2 (0x0002)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	44 (0x002C)
R12338 (R0x3032)	digital_binning	0000 0000 00dd 00dd	0 (0x0000)
R12346 (R0x303A)	frame_count	dddd dddd dddd dddd	65535 (0xFFFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12352 (R0x3040)	read_mode	dd00 0000 0000 0000	0 (0x0000)
R12356 (R0x3044)	dark_control	000d ddd0 d000 0d00	0 (0x0000)
R12358 (R0x3046)	flash	??00 000d d000 0000	0 (0x0000)
R12374 (R0x3056)	green1_gain	0000 0000 dddd dddd	32 (0x0020)
R12376 (R0x3058)	blue_gain	0000 0000 dddd dddd	32 (0x0020)
R12378 (R0x305A)	red_gain	0000 0000 dddd dddd	32 (0x0020)
R12380 (R0x305C)	green2_gain	0000 0000 dddd dddd	32 (0x0020)
R12382 (R0x305E)	global_gain	0000 0000 dddd dddd	32 (0x0020)
R12388 (R0x3064)	embedded_data_ctrl	000d dddd d000 dddd	6530 (0x1982)
R12398 (R0x306E)	datapath_select	dddd dddd 000d 00dd	37392 (0x9210)
R12400 (R0x3070)	test_pattern_mode	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12412 (R0x307C)	exposure_t2	???? ???? ???? ????	0 (0x0000)
R12416 (R0x3080)	exposure_t3	???? ???? ???? ????	0 (0x0000)
R12418 (R0x3082)	operation_mode_ctrl	0000 0000 00dd dddd	41 (0x0029)
R12420 (R0x3084)	operation_mode_ctrl_cb	0000 0000 00dd dd00	40 (0x0028)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)
R12424 (R0x3088)	seq_ctrl_port	?d00 000d dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 0ddd dddd dddd	0 (0x0000)
R12428 (R0x308C)	y_addr_start_cb	0000 00dd dddd dddd	2 (0x0002)
R12430 (R0x308E)	x_addr_end_cb	0000 0ddd dddd dddd	1283 (0x0503)
R12432 (R0x3090)	y_addr_end_cb	0000 00dd dddd dddd	965 (0x03C5)
R12446 (R0x309E)	ers_prog_start_addr	0000 000d dddd dddd	0 (0x0000)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 000d	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0ddd dddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0ddd dddd	1 (0x0001)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	990 (0x03DE)
R12460 (R0x30AC)	exposure_t1	???? ???? ???? ????	0 (0x0000)
R12464 (R0x30B0)	digital_test	dddd dddd dddd 0dd0	4976 (0x1370)
R12466 (R0x30B2)	tempsens_data	0000 00dd dddd dddd	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	0000 0000 00dd dddd	0 (0x0000)
R12474 (R0x30BA)	digital_ctrl	0000 0000 0000 dddd	3 (0x0003)
R12476 (R0x30BC)	green1_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12478 (R0x30BE)	blue_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12480 (R0x30C0)	red_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12482 (R0x30C2)	green2_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12484 (R0x30C4)	global_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12486 (R0x30C6)	tempsens_calib1	dddd dddd dddd dddd	291 (0x0123)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12488 (R0x30C8)	tempsens_calib2	dddd dddd dddd dddd	17767 (0x4567)
R12490 (R0x30CA)	tempsens_calib3	dddd dddd dddd dddd	35243 (0x89AB)
R12492 (R0x30CC)	tempsens_calib4	dddd dddd dddd dddd	52719 (0xCDEF)
R12500 (R0x30D4)	column_correction	ddd0 0000 0000 dddd	49159 (0xC007)
R12544 (R0x3100)	ae_ctrl_reg	0000 0000 dddd dddd	0 (0x0000)
R12546 (R0x3102)	ae_luma_target_reg	dddd dddd dddd dddd	1638 (0x0666)
R12548 (R0x3104)	ae_hist_target_reg	dddd dddd dddd dddd	49152 (0xC000)
R12550 (R0x3106)	ae_hysteresis_reg	dddd dddd dddd dddd	29491 (0x7333)
R12552 (R0x3108)	ae_min_ev_step_reg	0000 0000 dddd dddd	2 (0x0002)
R12554 (R0x310A)	ae_max_ev_step_reg	0000 0000 dddd dddd	2 (0x0002)
R12556 (R0x310C)	ae_damp_offset_reg	dddd dddd dddd dddd	16 (0x0010)
R12558 (R0x310E)	ae_damp_gain_reg	dddd dddd dddd dddd	16 (0x0010)
R12560 (R0x3110)	ae_damp_max_reg	dddd dddd dddd dddd	224 (0x00E0)
R12562 (R0x3112)	ae_dcg_exposure_high_reg	dddd dddd dddd dddd	671 (0x029F)
R12564 (R0x3114)	ae_dcg_exposure_low_reg	dddd dddd dddd dddd	140 (0x008C)
R12566 (R0x3116)	ae_dcg_gain_factor_reg	dddd dddd dddd dddd	714 (0x02CA)
R12568 (R0x3118)	ae_dcg_gain_factor_inv_reg	dddd dddd dddd dddd	91 (0x005B)
R12572 (R0x311C)	ae_max_exposure_reg	dddd dddd dddd dddd	960 (0x03C0)
R12574 (R0x311E)	ae_min_exposure_reg	dddd dddd dddd dddd	1 (0x0001)
R12576 (R0x3120)	ae_low_mean_target_reg	dddd dddd dddd dddd	100 (0x0064)
R12578 (R0x3122)	ae_hist_low_thresh_reg	dddd dddd dddd dddd	3932 (0x0F5C)
R12580 (R0x3124)	ae_dark_cur_thresh_reg	dddd dddd dddd dddd	32767 (0x7FFF)
R12582 (R0x3126)	ae_alpha_v1_reg	dddd dddd dddd dddd	128 (0x0080)
R12584 (R0x3128)	ae_alpha_coef_reg	dddd dddd dddd dddd	1260 (0x04EC)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12586 (R0x312A)	ae_current_gains	0000 0??? ???? ????	32 (0x0020)
R12608 (R0x3140)	ae_roi_x_start_offset	0000 0ddd dddd ddd0	0 (0x0000)
R12610 (R0x3142)	ae_roi_y_start_offset	0000 00dd dddd ddd0	0 (0x0000)
R12612 (R0x3144)	ae_roi_x_size	0000 0ddd dddd ddd0	1284 (0x0504)
R12614 (R0x3146)	ae_roi_y_size	0000 00dd dddd ddd0	964 (0x03C4)
R12616 (R0x3148)	ae_hist_begin_perc	dddd dddd dddd dddd	656 (0x0290)
R12618 (R0x314A)	ae_hist_end_perc	dddd dddd dddd dddd	65528 (0xFFF8)
R12620 (R0x314C)	ae_hist_div	dddd dddd dddd dddd	256 (0x0100)
R12622 (R0x314E)	ae_norm_width_min	dddd dddd dddd dddd	32 (0x0020)
R12624 (R0x3150)	ae_mean_h	0000 0000 0000 ????	0 (0x0000)
R12626 (R0x3152)	ae_mean_l	???? ???? ???? ????	0 (0x0000)
R12628 (R0x3154)	ae_hist_begin_h	0000 0000 0000 ????	0 (0x0000)
R12630 (R0x3156)	ae_hist_begin_l	???? ???? ???? ????	0 (0x0000)
R12632 (R0x3158)	ae_hist_end_h	0000 0000 0000 ????	0 (0x0000)
R12634 (R0x315A)	ae_hist_end_l	???? ???? ???? ????	0 (0x0000)
R12636 (R0x315C)	ae_hist_end_mean_h	0000 0000 0000 ????	0 (0x0000)
R12638 (R0x315E)	ae_hist_end_mean_l	???? ???? ???? ????	0 (0x0000)
R12640 (R0x3160)	ae_perc_low_end	???? ???? ???? ????	0 (0x0000)
R12642 (R0x3162)	ae_norm_abs_dev	???? ???? ???? ????	0 (0x0000)
R12644 (R0x3164)	ae_coarse_integration_time	???? ???? ???? ????	1 (0x0001)
R12646 (R0x3166)	ae_ag_exposure_hi	dddd dddd dddd dddd	671 (0x029F)
R12648 (R0x3168)	ae_ag_exposure_lo	dddd dddd dddd dddd	280 (0x0118)
R12650 (R0x316A)	ae_ag_gain1	dddd dddd dddd dddd	512 (0x0200)
R12652 (R0x316C)	ae_ag_gain2	dddd dddd dddd dddd	512 (0x0200)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12654 (R0x316E)	ae_ag_gain3	dddd dddd dddd dddd	512 (0x0200)
R12656 (R0x3170)	ae_inv_ag_gain1	dddd dddd dddd dddd	128 (0x0080)
R12658 (R0x3172)	ae_inv_ag_gain2	dddd dddd dddd dddd	128 (0x0080)
R12660 (R0x3174)	ae_inv_ag_gain3	dddd dddd dddd dddd	128 (0x0080)
R12672 (R0x3180)	delta_dk_control	dddd 0000 0000 0000	32768 (0x8000)
R12674 (R0x3182)	delta_dk_clip	dddd dddd dddd dddd	32767 (0x7FFF)
R12676 (R0x3184)	delta_dk_t1	???? ???? ???? ????	0 (0x0000)
R12678 (R0x3186)	delta_dk_t2	???? ???? ???? ????	0 (0x0000)
R12680 (R0x3188)	delta_dk_t3	???? ???? ???? ????	0 (0x0000)
R12682 (R0x318A)	hdr_mc_ctrl1	0000 dddd dddd dddd	4000 (0x0FA0)
R12684 (R0x318C)	hdr_mc_ctrl2	dddd dddd dddd dddd	64 (0x0040)
R12686 (R0x318E)	hdr_mc_ctrl3	dddd 00dd dddd dddd	272 (0x0110)
R12688 (R0x3190)	hdr_mc_ctrl4	dddd dddd dddd dddd	2976 (0x0BA0)
R12690 (R0x3192)	hdr_mc_ctrl5	000d dddd dddd dddd	1024 (0x0400)
R12692 (R0x3194)	hdr_mc_ctrl6	0000 dddd dddd dddd	3000 (0x0BB8)
R12694 (R0x3196)	hdr_mc_ctrl7	0000 dddd dddd dddd	3500 (0x0DAC)
R12696 (R0x3198)	hdr_mc_ctrl8	0000 dddd dddd dddd	4000 (0x0FA0)
R12698 (R0x319A)	hdr_comp_knee1	000? ???? 000? ????	4107 (0x100B)
R12700 (R0x319C)	hdr_comp_knee2	0000 0000 000? ????	20 (0x0014)
R12702 (R0x319E)	hdr_mc_ctrl9	dddd dddd dddd dddd	20544 (0x5040)
R12704 (R0x31A0)	hdr_mc_ctrl10	0000 dddd dddd dddd	2976 (0x0BA0)
R12706 (R0x31A2)	hdr_mc_ctrl11	0000 dddd dddd dddd	3000 (0x0BB8)
R12736 (R0x31C0)	hispi_timing	0ddd dddd dddd dddd	0 (0x0000)
R12742 (R0x31C6)	hispi_control_status	??00 00dd dddd dd00	32768 (0x8000)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12744 (R0x31C8)	hispi_crc_0	???? ???? ???? ????	65535 (0xFFFF)
R12746 (R0x31CA)	hispi_crc_1	???? ???? ???? ????	65535 (0xFFFF)
R12748 (R0x31CC)	hispi_crc_2	???? ???? ???? ????	65535 (0xFFFF)
R12750 (R0x31CE)	hispi_crc_3	???? ???? ???? ????	65535 (0xFFFF)
R12752 (R0x31D0)	hdr_comp	0000 0000 0000 00dd	1 (0x0001)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R12768 (R0x31E0)	pix_def_id	d000 0000 0000 00dd	0 (0x0000)
R12770 (R0x31E2)	pix_def_id_base_ram	000d dddd dddd dddd	0 (0x0000)
R12772 (R0x31E4)	pix_def_id_stream_ram	000d dddd dddd dddd	0 (0x0000)
R12774 (R0x31E6)	pix_def_ram_rd_addr	d000 0000 dddd dddd	0 (0x0000)
R12776 (R0x31E8)	horizontal_cursor_position	0000 00dd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 00dd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12788 (R0x31F4)	fuse_id1	dddd dddd dddd dddd	0 (0x0000)
R12790 (R0x31F6)	fuse_id2	dddd dddd dddd dddd	0 (0x0000)
R12792 (R0x31F8)	fuse_id3	dddd dddd dddd dddd	0 (0x0000)
R12794 (R0x31FA)	fuse_id4	dddd dddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	12320 (0x3020)
R16100 (R0x3EE4)	dac_ld_24_25	dddd dddd dddd dddd	53768 (0xD208)
R16336 (R0x3FD0)	bist_buffers_control1	0000 dddd dddd dddd	3840 (0x0F00)
R16338 (R0x3FD2)	bist_buffers_control2	0000 0ddd dddd dddd	0 (0x0000)
R16340 (R0x3FD4)	bist_buffers_status1	0??? ???? ???? ????	0 (0x0000)

Table 3: Manufacturer-Specific Register List and Default Values (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R16342 (R0x3FD6)	bist_buffers_status2	0000 0??? ???? ????	0 (0x0000)
R16344 (R0x3FD8)	bist_buffers_data1	000? ???? ???? ????	0 (0x0000)
R16346 (R0x3FDA)	bist_buffers_data2	000? ???? ???? ????	0 (0x0000)

Register Descriptions

Manufacturer-Specific Register Descriptions

Table 4: Manufacturer-Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12288 R0x3000	15:0	0x2400	chip_version_reg (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].				
12290 R0x3002	15:0	0x0002	y_addr_start (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				
12292 R0x3004	15:0	0x0000	x_addr_start (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.				
12294 R0x3006	15:0	0x03C5	y_addr_end (R/W)	Y	YM
	The last row of visible pixels to be read out.				
12296 R0x3008	15:0	0x0503	x_addr_end (R/W)	Y	N
	The last column of visible pixels to be read out.				
12298 R0x300A	15:0	0x03DE	frame_length_lines (R/W)	Y	YM
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. The rows included are: Column correction (tied) rows. Default 8. Delta dark rows. Default 6. Extra reset. 4 rows (2 used for embedded data when enabled), Image data (y_addr_end - y_addr_start +1) Extra reset. 4 rows (2 used for embedded stats data when enabled). Zebra Test rows. Default 4.				
12300 R0x300C	15:0	0x0672	line_length_pck (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. The minimum value supported in HiDY mode is 0x672. The minimum in linear mode is 0x5A0.				
12302 R0x300E	7:0	0x41	revision_number (R/W)	N	N
12304 R0x3010	15:0	0xBEEF	lock_control (R/W)	N	N
	This register protects the mirror mode select (register read mode). When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed, otherwise these values are locked.				
12306 R0x3012	15:0	0x0010	coarse_integration_time (R/W)	Y	N
	Integration time specified in multiples of line_length_pck_.				
12308 R0x3014	15:0	0x0000	fine_integration_time (R/W)	Y	N
	In HiDY mode, fine integration time is not used. In linear ERS mode, fine integration is used to delay the sampling operation. Thus, the integration time is increased. The resolution is 1 pixel clock time.				
12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N
	Coarse integration time in context B.				
12312 R0x3018	15:0	0x0000	fine_integration_time_cb (R/W)	N	N
	Fine integration time in context B.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12314 R0x301A	15:0	0x0058	reset_register (R/W)	N	Y
	15	0x0000	grouped_parameter_hold Must be set to 0.	N	N
	14:13	X	Reserved		
	12	0x0000	smia_serialiser_dis This bit disables the serial (HISPI) interface	N	N
	11	0x0000	forced_pll_on When set, enables the PLL immediately.	N	N
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	gpi_en 0 : The primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER and STANDBY inputs are powered down and cannot be used. 1: The input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0000	parallel_en 0 : The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N
	6	0x0001	drive_pins 0 : The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the enabling and use of the pad OUTPUT_ENABLE_N) 1: The parallel data interface is driven. This bit is “do not care” unless bit[7]=1.	N	N
	5	0x0000	reg_rd_en Enable signal to allow read from fuse ID registers.	N	N
	4	0x0001	stdby_eof 0: Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1: Transition to standby is synchronized to the end of a frame.	N	Y
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	Y
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y
	Controls the operation of the sensor. For details see the bit field descriptions.				
12318 R0x301E	15:0	0x00A8	data_pedestal (R/W)	N	Y
	Constant offset that is added to pixel values at the end of datapath (after all corrections).				
12326 R0x3026	15:0	0x0000	gpi_status (RO)	N	N
	15:4	X	Reserved		
	3	RO	standby Read-only. Return the current state of the STANDBY input pin. Invalid if R0x301A-B[8]=0.	N	N
	2	RO	trigger Read-only. Return the current state of the TRIGGER input pin. Invalid if R0x301A-B[8]=0.	N	N
	1	RO	oe_n Read-only. Return the current state of the OUTPUT_ENABLE_N input pin. Invalid if R0x301A-B[8]=0.	N	N
	0	RO	saddr Read-only. Return the current state of the pin SADDR input pin. This pad is not controlled by gpi_en.	N	N
	Reflects the status of the input pins: STANDBY(3), TRIGGER(2), OUTPUT_ENABLE_N(1). Bit 0 is not used.				
12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N
	Bits [6:4] of this register define the phase of the output pixclk. 2 set of values are correct: a) 000, 010, 100, 110 => 0 delay (rising edge of pixclk coincides DOUT change). b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of pixclk coincides DOUT change).				
12330 R0x302A	15:0	0x0006	vt_pix_clk_div (R/W)	N	N
	Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL).				
12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N
	sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL).				
12334 R0x302E	15:0	0x0002	pre_pll_clk_div (R/W)	N	N
	Referring to the PLL documentation: shows the n+1 value.				
12336 R0x3030	15:0	0x002C	pll_multiplier (R/W)	N	N
	PLL_MULTIPLIER: shows 2m value.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12338 R0x3032	15:0	0x0000	digital_binning (R/W)	N	N
	15:6	X	Reserved		
	5:4	0x0000	digital_binning_cb SCALING_MODE for context B 00: No binning 01: Horizontal only binning 10 : Horizontal and vertical binning	N	N
	3:2	X	Reserved		
	1:0	0x0000	digital_binning_ca DIGITAL_BINNING for context A 00: No binning 01 : Horizontal only binning 10: Horizontal and vertical binning	N	N
12346 R0x303A	15:0	0xFFFF	frame_count (R/W)	N	N
	Counts the number of output frames. At the startup is initialized to 0xffff.				
12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N
	15:2	X	Reserved		
	1	RO	standby_status This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].	N	N
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N
12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	14	0x0000	horiz_mirror 0 : Normal readout 1 : Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	13:0	X	Reserved		

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12356 R0x3044	15:0	0x0000	dark_control (R/W)	N	N
	15:13	X	Reserved		
	12	0x0000	show_colcorr_rows When set, the column correction rows and delta dark rows (including guard rows) will be included in FV and output. the order of output rows will be: column correction rows, delta dark rows, embedded data, image,. No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data.	N	N
	11	0x0000	show_dark_extra_rows When set, the delta dark rows (including guard rows) will be included in FV and output. the order of output rows will be: delta dark rows, embedded data, image,. No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data.	N	N
	10	0x0000	row_noise_correction_en 0 : Row-noise cancellation algorithm is disabled 1: Row-noise cancellation algorithm is enabled.	N	N
	9	0x0000	show_dark_cols When set, dark columns (tied) used for row noise correction are included to LV and output. No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data. Displaying dark columns can only be enabled if x_addr_start is set to 0	N	N
	8	X	Reserved		
	7	0x0000	show_zebra_test_rows When set, the zebra test rows are included in FV (after stats data rows) and will be output. No correction (except offset correction and gain equalization when AGS enabled) will be applied to the data.	N	N
	6:3	X	Reserved		
	2	0x0000	cancel_tx_col_corr Enables canceling of TX pulse when in column correction rows.	N	N
	1:0	X	Reserved		
12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N
	13:9	X	Reserved		
	8	0x0000	en_flash Enables the flash. The flash is asserted when an integration (either T1, T2 or T3 is ongoing).	Y	Y
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	6:0	X	Reserved		

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12374 R0x3056	15:0	0x0020	green1_gain (R/W)	Y	N
	Digital gain for green1 (Gr) pixels, in format of xxx.yyyyy.				
12376 R0x3058	15:0	0x0020	blue_gain (R/W)	Y	N
	Digital gain for Blue pixels, in format of xxx.yyyyy.				
12378 R0x305A	15:0	0x0020	red_gain (R/W)	Y	N
	Digital gain for Red pixels, in format of xxx.yyyyy.				
12380 R0x305C	15:0	0x0020	green2_gain (R/W)	Y	N
	Digital gain for green2 (Gb) pixels in format of xxx.yyyyy.				
12382 R0x305E	15:0	0x0020	global_gain (R/W)	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.				
12388 R0x3064	15:0	0x1982	embedded_data_ctrl (R/W)	N	N
	15:13	X	Reserved		
	12	0x0001	Reserved		
	11:10	0x0002	Reserved		
	9	0x0000	Reserved		
	8	0x0001	embedded_data 1: Frames of data out of the sensor include 2 rows of embedded data. 0: Frames out of the sensor exclude the embedded data. This register field should only be change while the sensor is in software standby.	N	N
	7	0x0001	embedded_stats_en Enables two rows of statistical data (used by external AE,.) after the transmission image data. Can not be enabled unless EMBEDDED_DATA_EN is enabled.	N	Y
	6:4	X	Reserved		
	3:0	0x0002	Reserved		

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12398 R0x306E	15:0	0x9210	datapath_select (R/W)	N	N
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[9:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	9	0x0001	high_vcm 0: For slvs low vcm. VDDSLVS must be 0.4V 1: For sub-SLVS high vcm. VDDSLVS = VDDIO = 1.8V	N	N
	8	0x0000	postscaler_data_sel 0: Statistics data are generated from pixel data before scaler. 1: Statistics data are generated from pixel data after scaler.	N	N
	7:5	X	Reserved		
	4	0x0001	true_bayer Enables true Bayer scaling mode.	N	N
	3:2	X	Reserved		
	1:0	0x0000	special_line_valid 00 : Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10 : LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID	N	N
12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y
	0 : Normal operation. Generate output data from pixel array 1: Solid color test pattern. 2: Full color bar test pattern 3: Fade to gray color bar test pattern 256 = Walking 1 test pattern (12-bit) Other : Reserved.				
12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.				
12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.				
12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
12412 R0x307C	15:0	0x0000	exposure_t2 (RO)	N	N
	T2 exposure time in rows.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12416 R0x3080	15:0	0x0000	exposure_t3 (RO)	N	N
	Actual T3 time in pixel clocks. Read only.				
12418 R0x3082	15:0	0x0029	operation_mode_ctrl (R/W)	N	Y
	15:6	X	Reserved		
	5:4	0x0002	ratio_t2_t3 Requested integration time ratio (T2 to T3): 00 : 4 01: 8 10: 16 11: 32	N	Y
	3:2	0x0002	ratio_t1_t2 Requested integration time ratio (T1 t0 T2): 00 : 4 01: 8 10: 16 11: 32	N	Y
	1:0	0x0001	operation_mode 00 : ERS HiDy mode 01: ERS Linear mode 10 : Not valid. 11: Not valid.	N	Y
12420 R0x3084	15:0	0x0028	operation_mode_ctrl_cb (R/W)	N	N
	15:6	X	Reserved		
	5:4	0x0002	ratio_t2_t3_cb RATIO_T2_T3_CB	N	N
	3:2	0x0002	ratio_t1_t2_cb RATIO_T1_T2_CB	N	N
	1:0	X	Reserved		
12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N
	Register used to write to or read from the sequencer RAM.				
12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N
	14	0x0001	auto_inc_on_read If 1 => The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte)	N	N
	13:9	X	Reserved		
	8:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N
	Register controlling the read and write to sequencer RAM.				
12426 R0x308A	15:0	0x0000	x_addr_start_cb (R/W)	N	N
	x_address_start context B				
12428 R0x308C	15:0	0x0002	y_addr_start_cb (R/W)	N	N
	Y_ADDR_START for context B				
12430 R0x308E	15:0	0x0503	x_addr_end_cb (R/W)	N	N
	X_ADDR_END for context B				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12432 R0x3090	15:0	0x03C5	y_addr_end_cb (R/W)	N	N
	Y_ADDR_END for context B				
12446 R0x309E	15:0	0x0000	ers_prog_start_addr (R/W)	N	N
	In case, an ERS sequencer program is also available after the HiDY program, this register must be loaded (from OTPM or M3ROM) with the correct start address in the sequencer RAM.				
12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N
	Read-only.				
12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM
	Not used. Do not change.				
12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N
	Read-only.				
12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM
	Not supported. Do not change.				
12456 R0x30A8	15:0	0x0001	y_odd_inc_cb (R/W)	N	N
	Y_ODD_INC context B				
12458 R0x30AA	15:0	0x03DE	frame_length_lines_cb (R/W)	N	N
	FRAME_LENGTH_LINES context B. See description for R0x3012				
12460 R0x30AC	15:0	0x0000	exposure_t1 (RO)	N	N
	Shows the t1 exposure time in HDR mode (in rows) and not used in linear mode.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12464 R0x30B0	15:0	0x1370	digital_test (R/W)	N	Y
	15	0x0000	Reserved		
	14	0x0000	pll_complete_bypass When set, the EXTCLK will be used and PLL will be bypassed. Note that the serial interface would not function.	N	N
	13	0x0000	context_b 0: Use context A 1: Use Context B	N	N
	12:10	0x0004	zebra_test_row_nr Number of the zebra test rows.	N	N
	9:8	0x0003	col_gain_cb Column gain for Context B	N	N
	7	0x0000	mono_chrome When set the CFA is mono chrome and not color. Some features like skipping and corrections are affected.	N	N
	6	0x0001	ags_enable When set, AGS is enabled.	N	N
	5:4	0x0003	col_gain Column gain: 00 : 1 01: 2 10: 4 11: 8	N	N
	3	X	Reserved		
	2	0x0000	ags_enable_t2 When set, AGS is enabled for T2.	N	N
	1	0x0000	no_sh_jump_limit When set, prevents logic from limiting the shutter increase. Normally shutter increase is limited to 4 *(ratio_t1_t2). To ensure this mode operate correctly, the frame_length_lines must be increased by 52 more than needed (meaning that VB is increased by 52).	N	N
	0	X	Reserved		
12466 R0x30B2	15:0	0x0000	tempsens_data (R/W)	Y	N
	Output value from temperature sensor.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)	N	N
	15:6	X	Reserved		
	5	0x0000	temp_clear_value Clear data register (sanity check).	N	N
	4	0x0000	temp_start_conversion When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated.	N	N
	3:1	0x0000	tempsens_test_ctrl Temp sensor test modes: 0: Normal operation 1d: Vb output on vtest_in_out 2d: Vctat output on vtest_in_out 3d: ADC conversion w/vtest_in_out replacing Vctat 4d: ADC conversion w/vtest_in_out replacing both Vctat and Vbg (expected output is zero).	N	N
	0	0x0000	tempsens_power_on tempsens_power_on	N	N
	Control register for temperature sensor				
12474 R0x30BA	15:0	0x0003	digital_ctrl (R/W)	Y	N
	15:4	X	Reserved		
	3	0x0000	colcorr_correct_always When set (=1) column FPN correction is applied also during collection and recalculation of new column FPN correction values.	N	N
	2	0x0000	Reserved		
	1	0x0001	enable_ags_colcorr_retrigg When set the AGS (analog/ column gain) change will retrigger the column FPN correction algorithm.	Y	N
	0	0x0001	enable_dcg_colcorr_retrigg When set, a DCG change will retrigger the column FPN correction algorithm.	Y	N
12476 R0x30BC	15:0	0x0020	green1_gain_cb (R/W)	N	N
	Digital gain green1 context B				
12478 R0x30BE	15:0	0x0020	blue_gain_cb (R/W)	N	N
	digital gain blue context B				
12480 R0x30C0	15:0	0x0020	red_gain_cb (R/W)	N	N
	digital gain red context B				
12482 R0x30C2	15:0	0x0020	green2_gain_cb (R/W)		
	digital gain green 2 context B				
12484 R0x30C4	15:0	0x0020	global_gain_cb (R/W)	N	N
	global digital gain context B				
12486 R0x30C6	15:0	0x0123	tempsens_calib1 (R/W)		
12488 R0x30C8	15:0	0x4567	tempsens_calib2 (R/W)	N	N
12490 R0x30CA	15:0	0x89AB	tempsens_calib3 (R/W)	N	N
12492 R0x30CC	15:0	0xCDEF	tempsens_calib4 (R/W)	N	N

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12500 R0x30D4	15:0	0xC007	column_correction (R/W)	N	N
	15	0x0001	enable Enable column correction.	N	N
	14	0x0001	double_range Double the range of the correction value but halves the precision.	N	N
	13	0x0000	double_samples Makes the column correction use 128 rows instead of 64. Adds 64 to the minimum frame blanking.	N	N
	12:4	X	Reserved		
	3:0	0x0007	colcorr_rows value showing the number of column correction rows - 1.	N	N
12544 R0x3100	15:0	0x0000	ae_ctrl_reg (R/W)	N	N
	15:8	X	Reserved		
	7	0x0000	dcg_manual_set_cb Manual dcg value used in context B.	N	N
	6:5	0x0000	min_ana_gain Minimum analog gain to be used by AE. '00'=1x (default) '01'=2x '10'=4x '11'=8x	N	N
	4	0x0000	auto_dg_en Automatic control of digital gain by AE is enabled.	N	N
	3	0x0000	auto_dcg_enable Enables automatic (AE controlled) DCG control.	N	N
	2	0x0000	dcg_manual_set If AE is disabled or automatic DCG is disabled, this bit will be used to decide the DCG gain. 1: High gain. 0: Low gain.	N	N
	1	0x0000	auto_ag_en When set, enables the automatic ae control of analog gain.	N	N
	0	0x0000	ae_enable 1: Enables the on-chip AE algorithm	N	N
12546 R0x3102	15:0	0x0666	ae_luma_target_reg (R/W)		
	Average luma target value to be reached by the auto exposure				
12548 R0x3104	15:0	0xC000	ae_hist_target_reg (R/W)	N	N
	Histogram high end target / 16				
12550 R0x3106	15:0	0x7333	ae_hysteresis_reg (R/W)		
	Hysteresis coefficient for histogram high end exposure ratio. Calculation of default value: Hysteresis * 32768 = 0.9 *32768 = 29491 = 0x7333.				
12552 R0x3108	15:0	0x0002	ae_min_ev_step_reg (R/W)		
	Minimum exposure value step size [15:8]: Reserved [7:0] : Min_EV_stepsize = (min step size)*256. Since Min_EV_stip sizes are small and they are typically less than 1 e.g. 1/16, 7/16 etc... these are multiplied by 256 and then the value is written to this register.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12554 R0x310A	15:0	0x0002	ae_max_ev_step_reg (R/W)		
	Maximum exposure value step size. Note that since this value is always greater than 1 there is no need to multiply by 256 as in the case of min_EV_stepsize.				
12556 R0x310C	15:0	0x0010	ae_damp_offset_reg (R/W)		
	Adjusts step size and settling speed.				
12558 R0x310E	15:0	0x0010	ae_damp_gain_reg (R/W)		
	Adjusts step size and settling speed.				
12560 R0x3110	15:0	0x00E0	ae_damp_max_reg (R/W)		
	Max value allowed for recursiveDamp (multiplied by 256 since internal value is typical <1). For most applications, the value of recursiveDamp should be <1, otherwise AE will overshoot the target. For applications with fast settling required, it may be desirable to allow recursiveDamp >1. Default value: 0.875 * 256 = 0x00E0				
12562 R0x3112	15:0	0x029F	ae_dcg_exposure_high_reg (R/W)		
	Integration time above which AE (if enabled) switches to DCG high gain. The value must be greater than: AEDCGGAINFACTOR (reg 0x3114) * AEDCGEXPOSURELOW (reg. 0x3116)				
12564 R0x3114	15:0	0x008C	ae_dcg_exposure_low_reg (R/W)		
	Integration time below which AE (if enabled) switches to DCG lo gain.				
12566 R0x3116	15:0	0x02CA	ae_dcg_gain_factor_reg (R/W)		
	Ratio gain between DCG Hi and DCG Lo (multiplied by 256). Tuned to match the DCG gain characteristics of the sensor.				
12568 R0x3118	15:0	0x005B	ae_dcg_gain_factor_inv_reg (R/W)		
	Inverse of gain ratio between DCG Hi and DCG Lo (multiplied by 256). Tuned to match the DCG gain characteristics of the sensor.				
12572 R0x311C	15:0	0x03C0	ae_max_exposure_reg (R/W)	N	N
	Maximum integration (exposure) time in rows to be used by AE.				
12574 R0x311E	15:0	0x0001	ae_min_exposure_reg (R/W)	N	N
	Minimum integration (exposure) time in rows to be used by AE.				
12576 R0x3120	15:0	0x0064	ae_low_mean_target_reg (R/W)	N	N
	Target value for low end mean (LEM). A means to specify how much of the dark region may be sacrificed and at what point the dark region is considered sacrificed. The chosen point at which the dark region is considered sacrificed will vary based on the user's desired minimum SNR. This choice is set using the LEM_min parameter. The perc_lowEnd_thresh parameter specifies what percentage of pixels may be ignored in the histogram low end. If the percentage of low end pixels exceeds perc_lowEnd_thresh, the minimum acceptable low end mean parameter (Lemming) is applied. This forces the histogram to increase exposure until the minimum low end mean is met.				
12578 R0x3122	15:0	0x0F5C	ae_hist_low_thresh_reg (R/W)	N	N
	Percentage of pixels that must be in the histogram low end before low end mean limiting is applied. Percentage * 65536. Default: 6% * 65536 = 3932 = 0x0F5C				
12580 R0x3124	15:0	0x7FFF	ae_dark_cur_thresh_reg (R/W)	N	N
	The dark current level that stops AE from increasing integration time. Note that increased integration time would increase dark current as well and signal level (SNR) would drop because photo diode well capacity is limited.				
12582 R0x3126	15:0	0x0080	ae_alpha_v1_reg (R/W)		
	Alpha V1 coefficient weighting of mean and hist end targets.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12584 R0x3128	15:0	0x04EC	ae_alpha_coef_reg (R/W)	N	N
	Slope ratio for alpha calculation [1/(v2-v1)]*128 Alpha coefficient is a weighting of mean and hist end targets.				
12586 R0x312A	15:0	0x0020	ae_current_gains (RO)		
	15:11	X	Reserved		
	10	RO	ae_conv_gain The gain decided by AE, when it is enabled and can control the conversion gain.	N	N
	9:8	RO	ae_ana_gain The gain decided by AE, when it is enabled and can control the analogue gain.	N	N
	7:0	RO	ae_dig_gain The gain decided by AE, when it is enabled and can control the digital gain.	N	N
	Shows the gain settings decided by AE.				
12608 R0x3140	15:0	0x0000	ae_roi_x_start_offset (R/W)	N	N
	Number of pixels into each row before the ROI starts NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels				
12610 R0x3142	15:0	0x0000	ae_roi_y_start_offset (R/W)	N	N
	Number of rows into each frame before the ROI starts				
12612 R0x3144	15:0	0x0504	ae_roi_x_size (R/W)	N	N
	Number of columns in the ROI				
12614 R0x3146	15:0	0x03C4	ae_roi_y_size (R/W)	N	N
	Number of rows in the ROI				
12616 R0x3148	15:0	0x0290	ae_hist_begin_perc (R/W)	N	N
	Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx				
12618 R0x314A	15:0	0xFFF8	ae_hist_end_perc (R/W)		
	Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)				
12620 R0x314C	15:0	0x0100	ae_hist_div (R/W)	N	N
	Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16				
12622 R0x314E	15:0	0x0020	ae_norm_width_min (R/W)	N	N
	Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option ie. all absolute deviation is normalized by hist_end - hist_begin				
12624 R0x3150	15:0	0x0000	ae_mean_h (RO)	N	N
	The true mean of all Gr pixels in the ROI (higher bits)				
12626 R0x3152	15:0	0x0000	ae_mean_l (RO)		
	The true mean of all Gr pixels in the ROI (16 least significant bits)				
12628 R0x3154	15:0	0x0000	ae_hist_begin_h (RO)		
	Code value corresponding to the histogram bin below which(hist_begin_perc*100)% of pixels exist (higher bits)				
12630 R0x3156	15:0	0x0000	ae_hist_begin_l (RO)	N	N
	Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower 16 bits)				
12632 R0x3158	15:0	0x0000	ae_hist_end_h (RO)		
	Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (higher bits)				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12634 R0x315A	15:0	0x0000	ae_hist_end_l (RO)	N	N
	Code value corresponding to the histogram bin below which(hist_end_perc*100)% of pixels exist (lower 16 bits)				
12636 R0x315C	15:0	0x0000	ae_hist_end_mean_h (RO)	N	N
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (higher bits)				
12638 R0x315E	15:0	0x0000	ae_hist_end_mean_l (RO)	N	N
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (lower 16 bits)				
12640 R0x3160	15:0	0x0000	ae_perc_low_end (RO)	N	N
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				
12642 R0x3162	15:0	0x0000	ae_norm_abs_dev (RO)	N	N
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				
12644 R0x3164	15:0	0x0001	ae_coarse_integration_time (RO)	N	N
	The integration time decided by AE.				
12646 R0x3166	15:0	0x029F	ae_ag_exposure_hi (R/W)	N	N
	At this integration time, the analog gain is increased (when AE is enabled to control also the analog gain).				
12648 R0x3168	15:0	0x0118	ae_ag_exposure_lo (R/W)	N	N
	At this integration time, the AE is reduced (when AE is enabled to control the analog gain also),				
12650 R0x316A	15:0	0x0200	ae_ag_gain1 (R/W)	N	N
	Real gain ratio between analog gain 0 and 1.				
12652 R0x316C	15:0	0x0200	ae_ag_gain2 (R/W)	N	N
	The real gain ratio between analog gain 2 and 1.				
12654 R0x316E	15:0	0x0200	ae_ag_gain3 (R/W)	N	N
	The real gain ratio between analog gain2 and gain3.				
12656 R0x3170	15:0	0x0080	ae_inv_ag_gain1 (R/W)	N	N
	The real inverse gain ratio between analog gain 0 and 1.				
12658 R0x3172	15:0	0x0080	ae_inv_ag_gain2 (R/W)		
	The real inverse gain ratio (1 to 2).				
12660 R0x3174	15:0	0x0080	ae_inv_ag_gain3 (R/W)	N	N
	The real inverse gain ratio (2 to 3).				
12672 R0x3180	15:0	0x8000	delta_dk_control (R/W)		
	15	0x0001	delta_dk_sub_en Enabling the delta dark correction.	N	N
	14	0x0000	delta_dk_every_frame Running the delta dark algorithm every frame or when gain, integration time is changing.	N	N
	13	0x0000	delta_dk_clip_en Enables the clipping of dark current. If the measured dark current is higher than clip level, only the clip level is used. See register 0x3182.	N	N
	12	0x0000	Reserved		
	11:0	X	Reserved		
12674 R0x3182	15:0	0x7FFF	delta_dk_clip (R/W)		
	Clip level for measured dark level.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12676 R0x3184	15:0	0x0000	delta_dk_t1 (RO)	N	N
	Measured dark current for exposure T1				
12678 R0x3186	15:0	0x0000	delta_dk_t2 (RO)	N	N
	Measured dark current for exposure T2				
12680 R0x3188	15:0	0x0000	delta_dk_t3 (RO)	N	N
	Measured dark current for exposure T3				
12682 R0x318A	15:0	0x0FA0	hdr_mc_ctrl1 (R/W)	N	N
	15:12	X	Reserved		
	11:0	0x0FA0	s2_threshold	N	N
12684 R0x318C	15:0	0x0040	hdr_mc_ctrl2 (R/W)	N	N
	15	0x0000	mc_noise_filter_en	N	N
	14	0x0000	motion_correction_en 0: Disable motion detection and correction 1: Enable motion detection and correction	N	N
	13:12	0x0000	bypass_pix_comb 00: Smooth combination of three components. 01: T1 data 10: T2 data 11 : T3 data	N	N
	11:0	0x0040	mc_diff_threshold	N	N
12686 R0x318E	15:0	0x0110	hdr_mc_ctrl3 (R/W)	N	N
	15:14	0x0000	pixel_build_mode_cb 00 : Normal hdr pixel build 01: Discard t3_data i.e. region 4 or 5 data treated as region 3 10: Discard t2_data and t3_data i.e. all data treated as region 1 11 : Discard t1_data and t2_data i.e. all data treated as region 5	N	N
	13:12	0x0000	pixel_build_mode 00 : Normal hdr pixel build 01: Discard t3_data i.e. region 4 or 5 data treated as region 3 10 : Discard t2_data and t3_data i.e. all data treated as region 1 11: Discard t1_data and t2_data i.e. all data treated as region 5	N	N
	11:10	X	Reserved		
	9	0x0000	motion2_en 0: Motion type 2 is ignored when detecting motion 1: Motion type 2 is considered when detecting motion	N	N
	8	0x0001	motion_correct_2d_en 0 : Perform 1D motion detection and correction (if motion_correction_en = 1: Perform 2D motion detection and correction (if motion_correction_en = 1)	N	N
	7:0	0x0010	mc_count_threshold	N	N

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12688 R0x3190	15:0	0x0BA0	hdr_mc_ctrl4 (R/W)	N	N
	15	0x0000	noise_filter_dlo_quad 0: Linear weighting function for the digital lateral overflow noise filter. 1: Quadratic weighting function for the digital lateral overflow noise filter.	N	N
	14	0x0000	noise_filter_dlo_en Enable noise filtering in the digital lateral overflow pixel combination.	N	N
	13	0x0000	pixel_build_dlo 0: Use the smooth combination method for combining t1, t2 and t3 data. 1: Use the digital lateral overflow method for combining t1, t2 and t3 data. This also overrides R0x318c[14], MOTION_CORRECTION_EN which gets disabled.	Y	N
	12	0x0000	mc_t1_sel 0: Regular motion correction 1: Motion corrupted pixels forced to use T1 data	N	N
	11:0	0x0BA0	t2_no_corr_threshold	N	N
12690 R0x3192	15:0	0x0400	hdr_mc_ctrl5 (R/W)	N	N
	15:13	X	Reserved		
	12:0	0x0400	s12_range	N	N
12692 R0x3194	15:0	0x0BB8	hdr_mc_ctrl6 (R/W)	Y	N
	15:12	X	Reserved		
	11:0	0x0BB8	t1_barrier Barrier for clipping T1 data in the digital lateral overflow combination method.	Y	N
12694 R0x3196	15:0	0x0DAC	hdr_mc_ctrl7 (R/W)		
	15:12	X	Reserved		
	11:0	0x0DAC	t2_barrier Barrier for clipping T2 data in the digital lateral overflow combination method.	Y	N
12696 R0x3198	15:0	0x0FA0	hdr_mc_ctrl8 (R/W)	Y	N
	15:12	X	Reserved		
	11:0	0x0FA0	t3_barrier Barrier for clipping T3 data in the digital lateral overflow combination method.	Y	N
12698 R0x319A	15:0	0x100B	hdr_comp_knee1 (RO)	N	N
	15:13	X	Reserved		
	12:8	RO	p2_comp_knee	N	N
	7:5	X	Reserved		
	4:0	RO	p1_comp_knee	N	N
12700 R0x319C	15:0	0x0014	hdr_comp_knee2 (RO)	N	N
	15:5	X	Reserved		
	4:0	RO	pmax_comp_knee	N	N

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12702 R0x319E	15:0	0x5040	hdr_mc_ctrl9 (R/W)	Y	N
	15:12	0x0005	s12_dlo_range Range of code values for the noise filter weighting transfer function for digital lateral overflow defined by s2_dlo - s1_dlo 4'b0000 = 1 4'b0001 = 2 4'b0010 = 4 4'b0011 = 8 4'b0100 = 16 4'b0101 = 32 4'b0110 = 64 4'b0111 = 128 4'b1000 = 256 4'b1001 = 512 4'b1010 = 1024 4'b1011 = 2048 4'b1100 = 4096 >= 4'b1101 = 8192 Setting the range to 8192 effectively sets s1 to -4095 and s2 to 4095.	Y	N
	11:0	0x0040	s2_dlo_threshold Threshold level for end point of noise filter weighting transfer function for digital lateral overflow.	Y	N
12704 R0x31A0	15:0	0x0BA0	hdr_mc_ctrl10 (R/W)	N	N
	15:12	X	Reserved		
	11:0	0x0BA0	s1_mc_threshold Separate S1 threshold (start of weighting function for smooth HDR pixel combination) for motion compensation.	N	N
12706 R0x31A2	15:0	0x0BB8	hdr_mc_ctrl11 (R/W)	N	N
	15:12	X	Reserved		
	11:0	0x0BB8	noise_dlo_dis_threshold For the digital lateral overflow method, if either T1 data, T2 data or T3 data is greater than this threshold, noise filtering is turned off. Evaluated on a single pixel.	N	N
12736 R0x31C0	15:0	0x0000	hispi_timing (R/W)		
	Bits (2:0) = DLL delay setting for data lane 0 Bits (5:3) = DLL delay setting for data lane 1 Bits (8:6) = DLL delay setting for data lane 2 Bits (11:9) = DLL delay setting for data lane 3 Bits (14:12) = DLL delay setting for clock lane The delay setting selects a tap along a delay element. Each stage is 1/8 of a symbol period. When the delay is set to zero, the delay element is powered down.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)		
	15:14	RO	hispi_status	N	N
	13:10	X	Reserved		
	9:2	0x0000	hispi_control bit[0] : Stream mode enable. bit[1]: Enable 3 lanes for compressed data bit[2:4]: Test mode defined as: 000 => transmit constant 0 on all enabled data lanes. 001 => transmit constant 1 on all enabled data lanes. 010 => transmit square wave at the half the potential serial data rate on all the enabled lanes. 011=> transmit square wave at the pixel data rate on all the enabled lanes. 100 => transmit a continuous, repeated, sequence of pseudo random data, with no SAV code, copied on all enabled data lanes. 101 => replace pixel data with a known sequence (PN9), copied on all the enabled data lanes. bit[5] : Test mode enable bit[6]: IO test enable bit[7] : Frame wide checksum test enable	N	N
	1:0	X	Reserved		
	See descriptions in the bit fields.				
12744 R0x31C8	15:0	0xFFFF	hispi_crc_0 (RO)		
12746 R0x31CA	15:0	0xFFFF	hispi_crc_1 (RO)	N	N
12748 R0x31CC	15:0	0xFFFF	hispi_crc_2 (RO)	N	N
12750 R0x31CE	15:0	0xFFFF	hispi_crc_3 (RO)	N	N
12752 R0x31D0	15:0	0x0001	hdr_comp (R/W)	N	N
	15:2	X	Reserved		
	1	0x0000	compand_14bits 0: Compand to 12 bits. 1: Compand to 14 bits	N	N
	0	0x0001	compand_en Enables companding	N	N
12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)	N	N
12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)	N	N
	Checksum of I^2C write operations.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12768 R0x31E0	15:0	0x0000	pix_def_id (R/W)	N	N
	15	0x0000	test When set, the pixel defect ID block is set in test mode. The contents of the defect RAMS can then be read at registers 0x31e2-3 and 0x31e4-5. To move to next entry, it is necessary to write to register bits 0x31e0-1[14:13]. This bit needs to be set to 0 before streaming.	N	Y
	14:2	X	Reserved		
	1	0x0000	correction_mode Mode of pixel defect correction. 0: Tag bad pixels with the reserved value 0. 1: Correct bad pixels, using Micron's traditional 1D correction scheme.	N	Y
	0	0x0000	enable Enable pixel defect correction.	N	Y
12770 R0x31E2	15:0	0x0000	pix_def_id_base_ram (R/W)		
	Data to be written to or read from the BASE RAM must be written to or read from this register.				
12772 R0x31E4	15:0	0x0000	pix_def_id_stream_ram (R/W)	N	N
	Data to be read from the STREAM RAM must be read from this register.				
12774 R0x31E6	15:0	0x0000	pix_def_ram_rd_addr (R/W)	N	N
	15	0x0000	Reserved		
	14:8	X	Reserved		
	7:0	0x0000	Reserved		
	The content of this register points to location in the BASE and/or STREAM RAM to be read by I2C transaction. There is no auto increment on read, This register must be updated before read. Bit [15] indicate if base_ram_end_addr should be updated with the address in bits [7]:[0]. No data will be written to BASE RAM when bit [15] is activated.				
12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)	N	N
	Specify the start row for the test cursor.				
12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)	N	N
	Specify the start column for the test cursor.				
12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)	N	N
	Specify the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.				
12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)	N	N
	Specify the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.				
12788 R0x31F4	15:0	0x0000	fuse_id1 (R/W)	N	N
	Bits 15:0 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset)				
12790 R0x31F6	15:0	0x0000	fuse_id2 (R/W)	N	N
	Bits 31:16 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset)				
12792 R0x31F8	15:0	0x0000	fuse_id3 (R/W)	N	N
	Bits 47:32 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset)				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12794 R0x31FA	15:0	0x0000	fuse_id4 (R/W)	N	N
	Bits 63:48 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/Write (the programmed value can be over-written and will be restored on reset)				
12796 R0x31FC	15:0	0x3020	i2c_ids (R/W)	N	N
	I2C addresses.				
16100 R0x3EE4	15:0	0xD208	dac_ld_24_25 (R/W)	N	N
	15:14	0x0003	Reserved		
	13	0x0000	Reserved		
	12	0x0001	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9:8	0x0002	ana_sreg_col_amp_gabs Absolute gain programming of column amplifier	N	N
	7:6	X	Reserved		
	5	0x0000	Reserved		
	4	0x0000	Reserved		
	3:0	0x0008	Reserved		
16336 R0x3FD0	15:0	0x0F00	bist_buffers_control1 (R/W)	N	N
	15:12	X	Reserved		
	11	0x0001	diag_whole When set, In diagnosis mode, test until find the first error in the unit. When reset, In diagnosis mode, test only the mentioned address and word.	N	N
	10	0x0001	test_en_s3 enables bist for S3 group of buffers	N	N
	9	0x0001	test_en_s2 enables bist for s2 group of buffers	N	N
	8	0x0001	test_en_s1 enables bist for s1 group of buffers	N	N
	7:2	0x0000	diag_unit_nr Unit number for the memory that is to be tested by buffers BIST in diagnostic mode. The values are: 0 : 47 for S1 48 : 51 for S2 52: 53 for S3.	N	N
	1	0x0000	diagnostic_mode When this bit and the bit bist_mode (bit 00, this address) are set, the BIST will only check the memory unit defined by the bits 7:2 (this address).	N	N
	0	0x0000	bist_mode When set, it start the BIST in streaming mode. IT must be reset after reading the results of the BIST. For a new BIST test to start, it must be toggled.	N	N
	Controls the operation of the special BISt for testing the delay buffers.				

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
16338 R0x3FD2	15:0	0x0000	bist_buffers_control2 (R/W)	N	N
	15:11	X	Reserved		
	10:2	0x0000	diag_addr The address to be diagnosed (0 to 351). Other values will not be found, therefore BIST will finish even many failures exist.	N	N
	1:0	0x0000	diag_word The word to be diagnosed (0 to 3). 0: Bits [12:0] of memory word 1: Bits [25:13] of memory word 2: Bits [38:26] of memory word 3: Bits [51:39] of memory word	N	N
16340 R0x3FD4	15:0	0x0000	bist_buffers_status1 (RO)	N	N
	15	X	Reserved		
	14:11	RO	test_progress Test pattern number currently running. At the end of a complete and failure free test, these bits must read 10.	N	N
	10:5	RO	unit_failed_nr The unit number for the first (first encountered) failed memory unit.	N	N
	4:1	RO	test_seq When test failed, these bits show the detecting sequence number.	N	N
	0	RO	test_failed TEST_FAILED.	N	N
	Status data from BIST run.				
16342 R0x3FD6	15:0	0x0000	bist_buffers_status2 (RO)	N	N
	15:11	X	Reserved		
	10:2	RO	failed_addr The address to the (first encountered) failed location in the memory. Values between 0 to 351.	N	N
	1:0	RO	failed_word The failed word number. Each address in the memory is 52 bits, which is divided to 4 words of 13 bits. Word_sel = 00 => bits 12:0. Word_sel = 01 => bits 25:13. Word_sel = 10 => bits 38:26. Word_sel = 11 => bits 51:29.	N	N
	Status from BIST run				
16344 R0x3FD8	15:0	0x0000	bist_buffers_data1 (RO)	N	N
	Data read from memory.				
16346 R0x3FDA	15:0	0x0000	bist_buffers_data2 (RO)	N	N
	The expected data from the memory.				

Revision History

Rev. B 11/26/12

- Updated to Production
- Updated to Rev 4 register Database

Rev. A 1/6/11

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com