1/4-Inch 1.3-Megapixel SOC CMOS Digital Image Sensor

MT9M112 Data Sheet

Features

- Aptina™ CMOS imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, low cost, progressive scan CMOS image sensor
- On-die phase lock loop (PLL)
- Superior low-light performance
- On-die image flow processor (IFP) performs sophisticated processing: Color recovery and correction, sharpening, gamma correction, lens shading correction, and on-the-fly defect correction
- Programmable I/O slew rate
- 2 x 2 pixel binning
- Mechanical shutter support
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Fully automatic Xenon- and LED-type flash support
- Automatic Features:
  Auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Multiple parameter contexts, easy/fast mode switching
- Camera control sequencer automates snapshots, snapshots with flash, and video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats
- VDD power disable switch for reduced standby current
- Four general purpose input bond pads

Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch (5:4)
Active imager size		3.58mm(H) x 2.87mm(V) 4.59mm diagonal
Active pixels		1280H x 1024V
Pixel size		2.8µm x 2.8µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		27 MPS/54 MHz
Frame rate		15 fps at full resolution, 30 fps in preview mode (640 x 512)
ADC resolution		10-bit, on-chip
Responsivity		1.0V/lux-sec (550nm)
Dynamic range		68dB
SNR_{MAX}		44dB
Supply voltage	I/O digital	1.7V–3.1V
	Core digital	1.7V–1.9V (1.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power consumption		170mW at 15 fps, full resolution 100mW at 30fps, preview mode
Operating junction temperature		-30°C to +70°C
Packaging		Die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9M112D00STC	Die

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General Description

The Aptina MT9M112 is an SXGA-format, single-chip camera CMOS active-pixel digital image sensor. This device combines the 2.8µm image sensor core with fourth-generation digital image flow processor technology from Aptina. It captures high-quality color images at SXGA resolution.

The SXGA CMOS image sensor features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity), while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M112 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations, special camera effects such as sepia tone and solarization, and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes. The device also has an on-board PLL, and supports pixel binning as an enhanced form of image size reduction.

The MT9M112 can be programmed to output progressive-scan images up to 30 fps. The image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated signals, along with a pixel clock that is synchronous with valid data.

Functional Overview

The MT9M112 is a fully-automatic, single-chip camera that requires only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8-bit DOUT port as shown in Figure 1 on page 8. The output pixel clock is used to latch data, while FRAME_VALID and LINE_VALID signals indicate the active video. The MT9M112 internal registers are configured using a two-wire serial interface.

The device can be put in a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry in standby mode also can be achieved through the two-wire serial interface register writes.

The MT9M112 accepts input clocks up to 54 MHz, delivering up to 30 fps for VGA resolution images.

Internal Architecture

Internally, the MT9M112 consists of a sensor core and an image flow processor (IFP). The IFP is divided in two sections: the colorpipe (CP) and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance and to support snapshot modes. The sensor core, CP, and CC registers are grouped in three separate address spaces as shown in Figure 2 on page 8.

When accessing internal registers through the two-wire serial interface, select the desired address space by programming the R0xF0 (R240) register.

The MT9M112 accelerates mode-switching with hardware-assisted context switching and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9M112 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FRAME_VALID/LINE_VALID video interface with gated pixel clocks
- ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocks

Register Notation

The following register address notations are used in this document:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register (register 9) in the sensor page (page 0). Used to uniquely specify a register.
- R0x<3 digit hex address>
  Example: 0x106 —Mode control in Page 1 register 0x6; leading digit signifies page number.
- Data Format (Binary) Column Key in the Register Summary tables. The following key is used to indicate data format:
  ? = Read Only
  d = Read/Write
  0 = Reserved; read 0; must write 0
  1 = Reserved; read 1; must write 1
  r = Reserved; must write back value read
- The following key is used to indicate default value
  X = Indeterminate Register Default Values

Register Definition Table

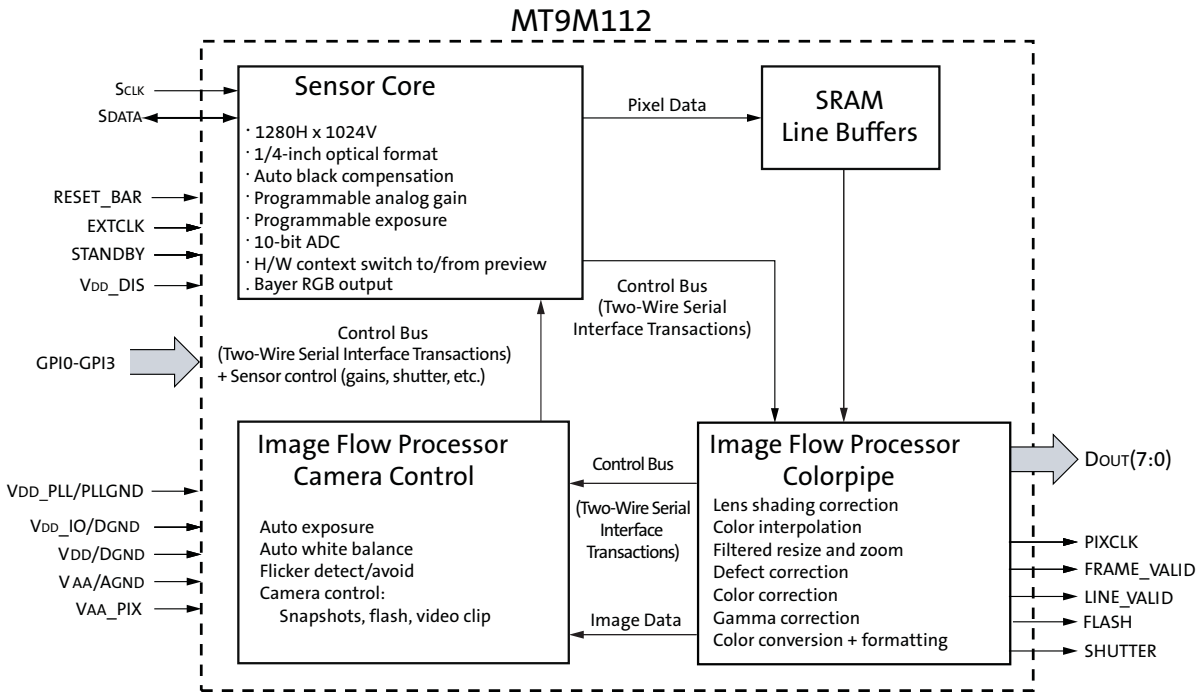
The register definition tables contain the power-on default values for the bit fields and registers of the MT9M112. Modifying these values may [affect or degrade] the performance of the MT9M112. See the individual register descriptions for more detail.

Reserved Registers

Do not alter the reserved registers. If some bits or bit patterns (that is, bit field values) in a register are reserved, they cannot be used. Do not set bit fields to reserved or undefined bit patterns as Aptina will not guarantee operation.

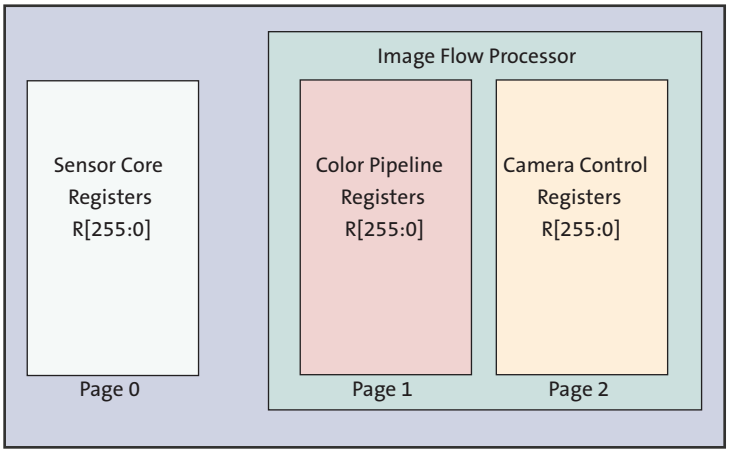
For more detail on registers, see the MT9M112 Register Reference.

Figure 1: Functional Block Diagram



Note: Each of the general purpose input only signals (GPI0–GPI3) must be connected to either DGND or VDD_IO for low-power consumption and reliable operation

Figure 2: Internal Registers Grouping



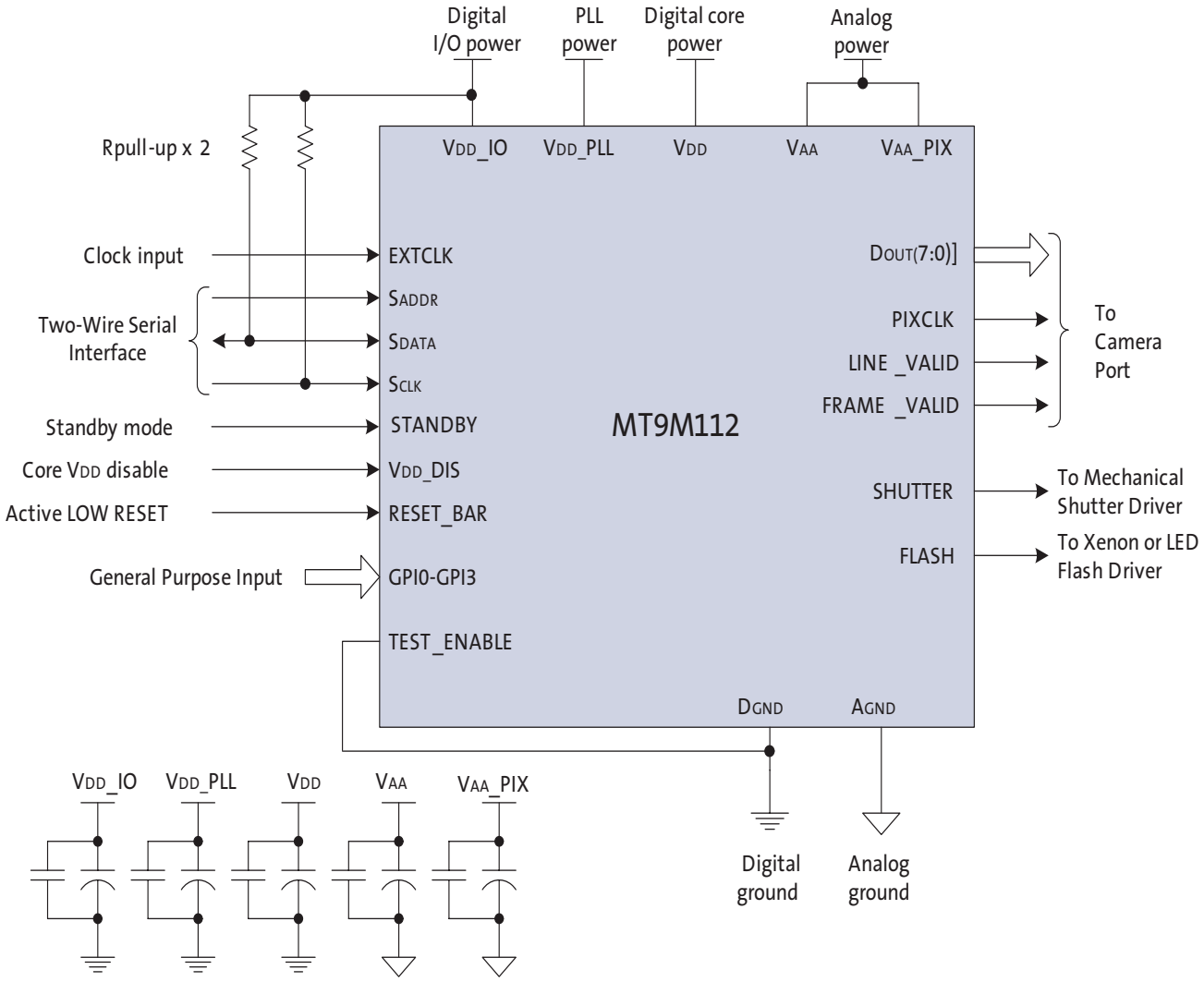
Note: Internal registers are grouped in three address spaces. Register R0xF0 (R240) in each page selects the desired address space.

Typical Connections

Figure 3 shows typical MT9M112 device connections. For low-noise operation, the MT9M112 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails must be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9M112 also supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGND) power domains that can be at different voltages. PLL requires a clean power source (VDD_PLL).

Figure 3: Typical Configuration (Connection)



Note:
1. 1. A 1.5KΩ resistor value is recommended for the two-wire serial interface $R_{pull-up}$; however, greater values may be used for slower transmission speeds.
2. MT9M112 STANDBY can be connected to the customer's ASIC controller directly, or to digital GND, depending on the capability of the controller.
3. The PLL bypass capacitor should be connected to VDD_PLL and DGND.
4. Do not leave General Purpose Input only signals, GPI0-GPI3, floating. Must terminate to DGND or VDD_IO.

Signal Descriptions: Inputs, Outputs, and Supply

Table 3: Signal Description

Name	Type	Supply Reference	Description
EXTCLK	Input	VDD_IO/DGND	Master clock in sensor.
RESET_BAR	Input	VDD_IO/DGND	Active LOW: asynchronous reset.
SADDR	Input	VDD_IO/DGND	Two-wire serial interface device ID selection 1:0xBA, 0:0x90.
TEST_ENABLE	Input	VDD_IO/DGND	Tie to DGND for normal operation (manufacturing use only).
SCLK	Input	VDD_IO/DGND	Two-wire serial interface clock.
STANDBY	Input	VDD_IO/DGND	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
VDD_DIS	Input	VDD_IO/DGND	Disable core digital VDD for low power operation.
GPI0-GPI3	Input	VDD_IO/DGND	General purpose Inputs, do not leave floating; must terminate to either VDD_IO or DGND.
SDATA	Bidirectional	VDD_IO/DGND	Two-wire serial interface data I/O.
DOUT7-DOUT0	Output	VDD_IO/DGND	In normal mode, pixel data output: DOUT7 is the most significant bit (MSB), DOUT0 is the least significant bit (LSB). In 10-bit, SOC bypass mode, DOUT0 is bit 2, DOUTLSB1 is bit 1, and DOUTLSB0 is bit 0.
DOUTLSB1, DOUTLSB0	Output	VDD_IO/DGND	Data out bit 1 and 0 in 10-bit SOC bypass mode.
FRAME_VALID	Output	VDD_IO/DGND	Active HIGH: FRAME_VALID; indicates active frame.
LINE_VALID	Output	VDD_IO/DGND	Active HIGH: LINE_VALID; indicates active pixel.
PIXCLK	Output	VDD_IO/DGND	Pixel clock output.
FLASH	Output	VDD_IO/DGND	Active HIGH: control external LED or Xenon flash devices.
SHUTTER	Output	VDD_IO/DGND	Active HIGH: controls external mechanical shutter.
AGND	Supply	VAA, VAA_PIX	Analog ground.
DGND	Supply	VDD, VDD_IO	Common digital core ground and digital I/O ground.
VAA	Supply	AGND	Analog power.
VAA_PIX	Supply	AGND	Pixel array analog power supply.
VDD	Supply	DGND	Core digital power.
VDD_IO	Supply	DGND	I/O digital power.
VDD_PLL	Supply	DGND	PLL power.
DNU	–	–	Factory test signal. Do not connect.

All inputs and outputs are implemented with bidirectional buffers. Care must be taken that all inputs are driven to avoid floating nodes.

Refer to the MT9M112 die data sheet (1/4-inch 1.3-Megapixel SOC Digital Image Sensor Die Features) document for pad number information.

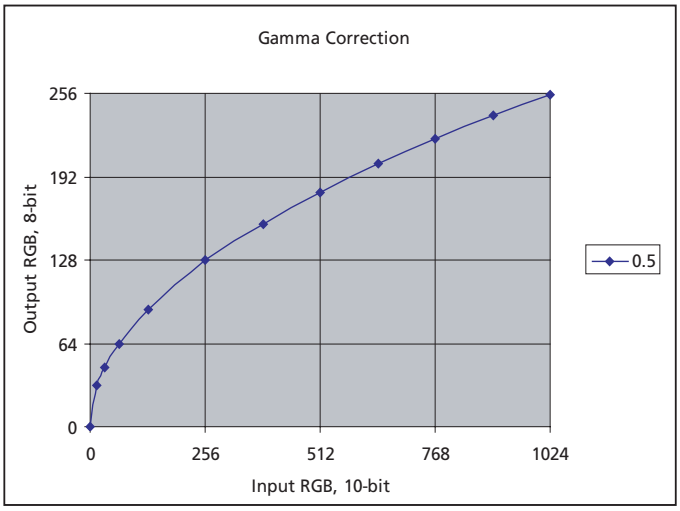
General Purpose Inputs

Logic levels of four general purpose inputs GPI0-GPI3 may be read through the two-wire serial interface facilitating packaging identification. These signals must be terminated to either VDD_IO or DGND to ensure that they are not floating.

The resulting interpolated RGB data passes through the current color correction matrix (CCM), saturation, and gamma corrections and is formatted for final output.Reducer and zoom window changes are synchronized so the reducer and zoom programming do not have to be coordinated with video frame timing.

The MT9M112 has 2D defect correction where pixels with values different from their neighbors by a programmable threshold are considered defects and are replaced.To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. Optimum values for the color correction coefficients depend on the spectrum of the incident illumination and can either be programmed by the user, or automatically selected by the AWB algorithm.

Figure 4: Gamma Correction Curve



The MT9M112 supports gradual color saturation reduction in the brightest areas of the image, helping eliminate color artifacts related to clipped pixel values. For noise reduction, both color saturation and sharpness enhancement can be set by the user or adjusted automatically by tracking the magnitude of the gains used by the auto exposure algorithm. Color saturation may be scaled by a constant value of either 0 percent (black and white), 25 percent (1/4), 37.5 percent (3/8), 50 percent (1/2), 75 percent (3/4), 100 percent (1/1), 112.5 percent (9/8), 125 percent (5/4), 137.5 percent (11/8), and 150 percent (3/2).

Output Data Ordering

The following tables describe the output data order depending on the mode selected.

Table 4: Data Ordering in YCbCr Mode

Mode	Byte	Byte+1	Byte+2	Byte+3
Default	Cb_i	Y_i	Cr_i	Y_{i+1}
Swap Red and Blue	Cr_i	Y_i	Cb_i	Y_{i+1}
Swap bytes	Y_i	Cb_i	Y_{i+1}	Cr_i
Swap Red and Blue, Swap bytes	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 5: Output Data Ordering in Processed Bayer Mode

Mode	Line	Byte	Byte+1	Byte+2	Byte+3
Default	First	G_i	R_{i+1}	G_{i+2}	R_{i+3}
	Second	B_i	G_{i+1}	B_{i+2}	G_{i+3}
Flip Bayer column	First	R_i	G_{i+1}	R_{i+2}	G_{i+3}
	Second	G_i	B_{i+1}	G_{i+2}	B_{i+3}
Flip Bayer row	First	B_i	G_{i+1}	B_{i+2}	G_{i+3}
	Second	G_i	R_{i+1}	G_{i+2}	R_{i+3}
Flip Bayer column Flip Bayer row	First	G_i	B_{i+1}	G_{i+2}	B_{i+3}
	Second	R_i	G_{i+1}	R_{i+2}	G_{i+3}

Table 6: Output Data Ordering in RGB Mode

Mode (Swap disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
RGB444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGBx444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Table 7: Output Data Ordering in (8 + 2) Bypass Mode

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
8 + 2 bypass	First	B9	B8	B7	B6	B5	B4	B3	B2
	Second	0	0	0	0	0	0	B1	B0

Table 8: Bayer Output Order R0x108[1:0] = 00

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
0	0	First	G	R	G	R
		Second	B	G	B	G

Table 9: Bayer Output Order R0x108[1:0] = 01

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
0	1	First	R	G	R	G
		Second	G	B	G	B

Table 10: Bayer Output Order R0x108[1:0] = 10

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
1	0	First	B	G	B	G
		Second	G	R	G	R

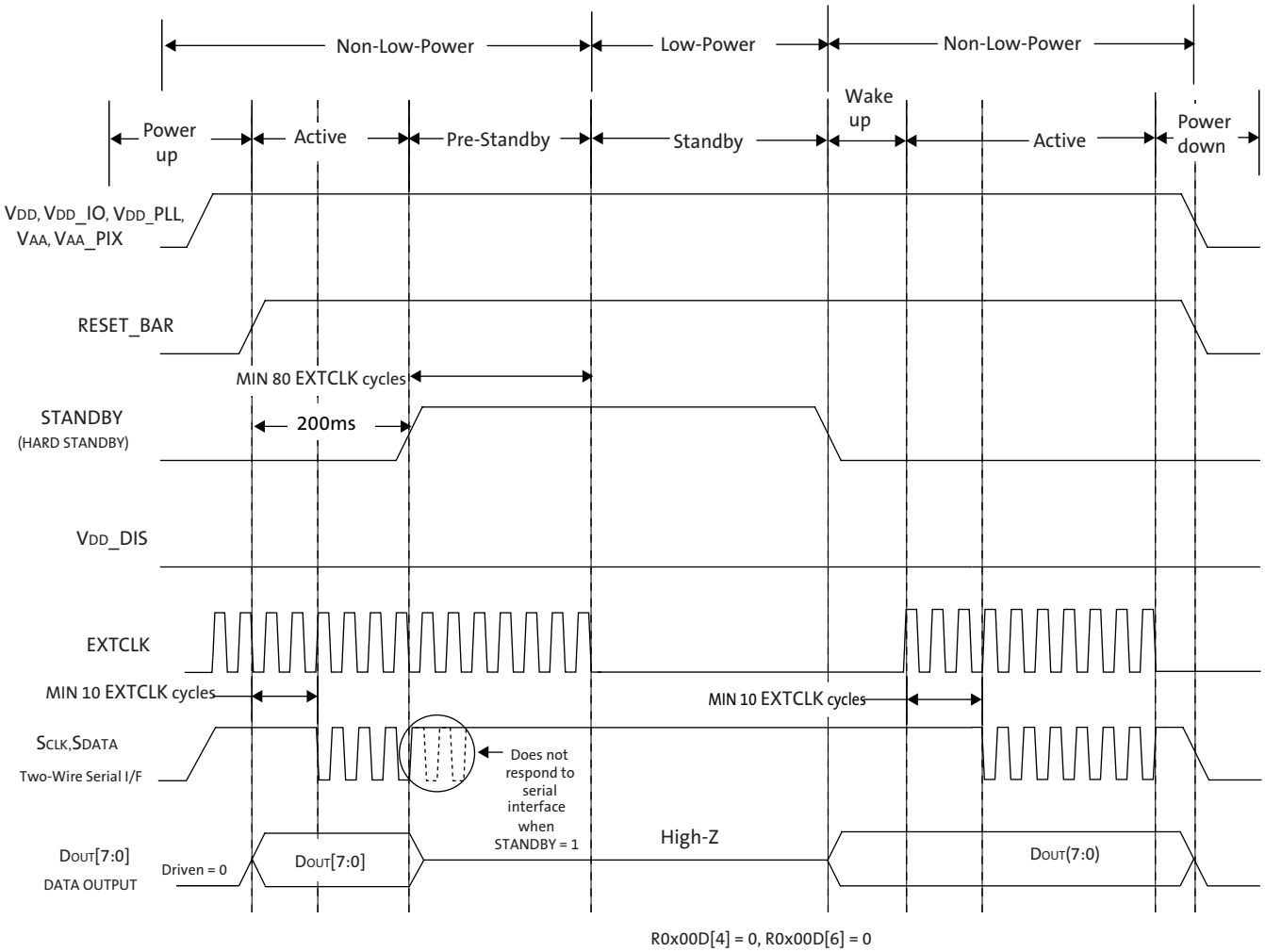
Table 11: Bayer Output Order R0x108[1:0] = 11

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
1	1	First	G	B	G	B
		Second	R	G	R	G

Reset, Clocks, and Low Power Modes

There are no constraints concerning the order in which the various power supplies are applied; however, the MT9M112 requires reset in order to operate properly at power-up. Refer to the Figure 5 for the power-up, reset, and standby sequences.

Figure 5: Power-Up, Reset, Clock, and Standby Sequence



Note:
1. All output signals are defined during initial power-up with RESET_BAR = 0 without EXTCLK being active. For a proper reset sequence for the rest of the sensor, during initial powerup, assert RESET_BAR = 0 for at least 1µS after all power supplies have stabilized and EXTCLK is active (being clocked). Driving RESET_BAR = 0 does not put the part in a low power state.
2. In Hard standby the output signals are high impedance by default. The output state is controlled by register R0x00D settings.
3. Soft standby is asserted or deasserted by a two-wire serial interface to R0x00D[2]. In this mode, the analog clock and the internal clocks are shut off. The output signals are not high impedance by default. The total leakage currents can be lowered if the two-wire serial interface and the EXTCLK are turned OFF after 80 EXTCLK cycles after issuing soft standby.
4. Wait for 10 EXTCLK rising edges after RESET_BAR is deasserted before using two-wire serial interface.
5. Illustration not drawn to scale (do not count number of clock pulses).

Power Supply Skew During Power Up

There are no constraints concerning the order in which the various power supplies are applied to the part. As long as a hardware reset is asserted following the stabilization of supplies, the part will be properly initialized. However, to minimize power consumption, all power supplies must be simultaneously applied with no more than 1ms of skew. See Figure 6 for more details.

Figure 6: Power Supply Skew

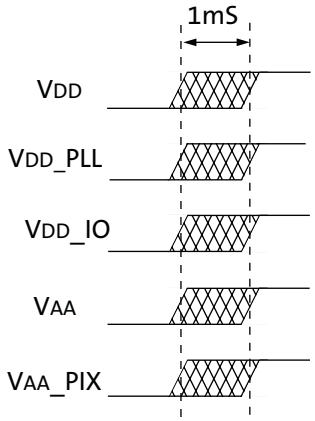
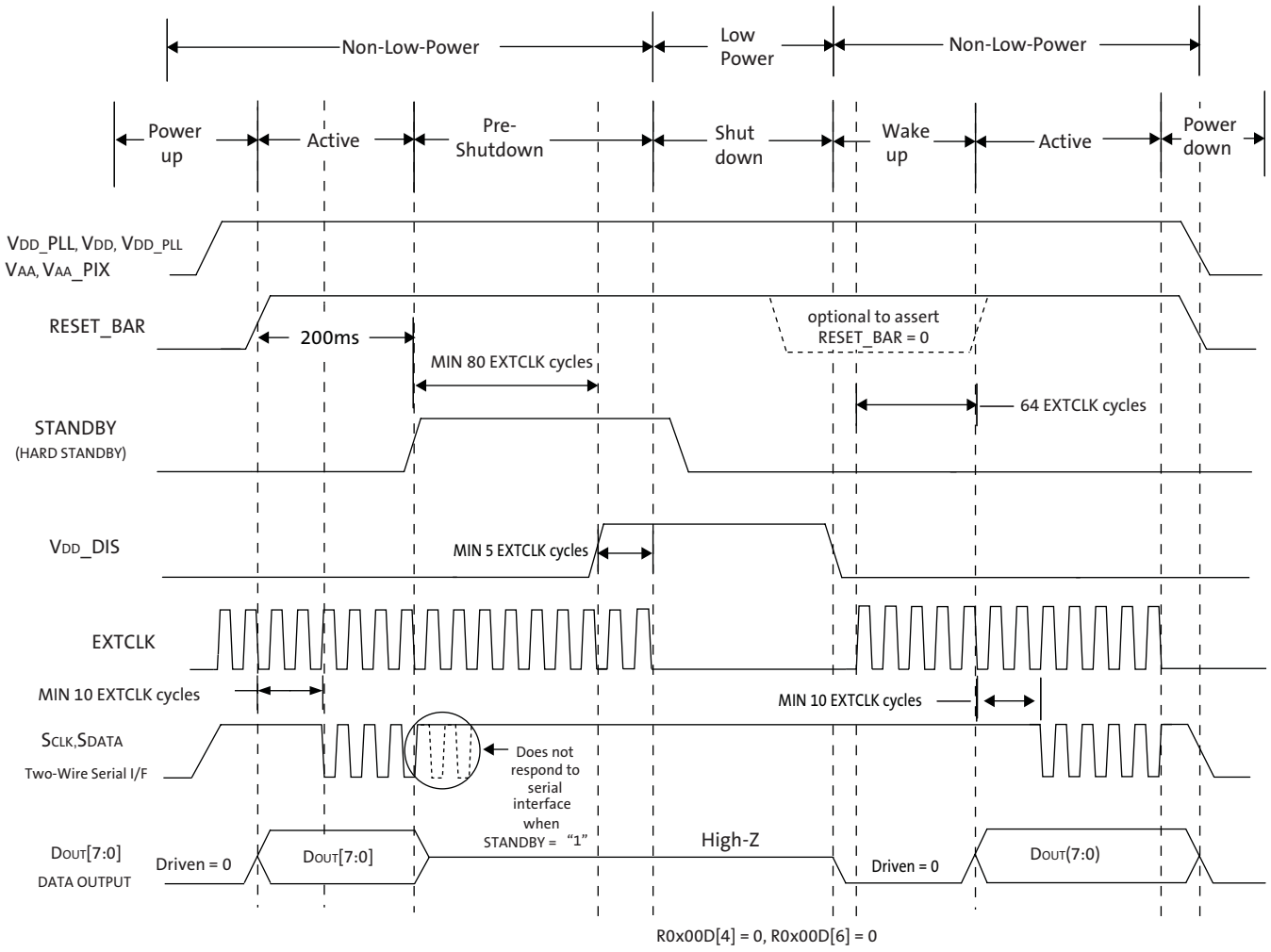


Figure 7: VDD_DIS Shutdown Sequence



Note: Illustration not drawn to scale (do not count number of clock pulses).

VDD Disable Feature

The VDD_DIS signal is used to shut down digital core VDD reducing the power consumption significantly during standby. All register settings are lost. However, the output signal states are maintained as long as VDD_IO is maintained. Output signals must be configured appropriately during the standby sequence. Input signal transitions (including RESET_BAR) during VDD_DIS = 1 are ignored.

Proper shutdown and recovery sequences must be followed for minimum power consumption.

Disable and enable the core VDD using the VDD_DIS signal with the following sequences.

To Enter Low Power State

1. PLL bypass R0x065[15] = 1
2. PLL into standby/power down
3. Enter standby mode (hardware or software)
4. Assert VDD_DIS
5. Stop EXTCLK
6. Deassert STANDBY if asserted
7. The part is now in a core VDD shutdown low power state

To Exit Low Power State

1. Assert RESET_BAR (optional)
2. Assert STANDBY if the output must be high impedance during start-up
3. Deassert VDD_DIS
4. Start EXTCLK
5. De-assert RESET_BAR (if asserted in step 1 above) and start up the sensor

PLL Operation

The sequence to turn on PLL is:

1. After the chip power on reset, PLL is in bypass mode by default.
2. Program PLL parameters M, N, and P in R0x066 and R0x067 depending on the external clock frequency and target clock frequency. PLL output clock frequency (f_{OUT}) is calculated with the following equation:

$$f_{OUT} = f_{EXTCLK} \times M \times \left(\frac{1}{2 \times (N + 1) \times (P + 1)} \right) \quad \text{(EQ 1)}$$

   Where f_{EXTCLK} is external clock frequency, N is pre-divider and P is post-divider. Both registers have a default value of "1."
3. Wake up PLL by programming R0x065[14] = 0.
4. Wait at least 1ms for PLL to stabilize.
5. Program R0x065[15] = 0 to enable PLL output to clock core and release PLL bypass.

Electrical Specifications

DC Electrical Specification

Table 12 defines the main power supply voltages and operating conditions of the MT9M112.

Table 12: DC Electrical Characteristics and Operating Conditions
Setup conditions: T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.9	V
V_{DD_IO}	I/O digital voltage		1.7	1.8V or 2.8V	3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL analog voltage		2.5	2.8	3.1	V
	Leakage current	STANDBY = V_{DD_IO} (asserted) V_{DD_DIS} = V_{DD_IO} (asserted) EXTCLK = 0V (no clocks running)	–	–	10	µA
		STANDBY = V_{DD_IO} (asserted) V_{DD_DIS} = 0V (deasserted) EXTCLK = 0V (no clocks running)	–	–	300	µA
	Operating power consumption[1]	SXGA at 15 fps	–	170	–	mW
		VGA at 30 fps, binning enabled	–	100	–	
T_J	Operating junction temperature		-30	–	+70	°C

Note: 1. Power consumption numbers do not include power from V_{DD_IO}.

I/O Parameters

Table 13 and Table 14 define threshold parameters for voltage and current on input and output signals.

Table 13: I/O Min/Max Parameters (V_{DD_IO} = 1.8V)

Setup conditions: V_{DD} = 1.8V, V_{DD_IO} = 1.8V, V_{AA} = 2.8V, V_{AA_PIX} = 2.8V, V_{DD_PLL} = 2.8V, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	Min	Max	Unit
V_{IH}	Input high voltage	I_{IH} = -10 µA	1.7	–	V
V_{IL}	Input low voltage	I_{IL} = 10 µA	–	0.3	V
V_{OH}	Output high voltage	I_{OH} = -9mA	V_{DD_IO} - 0.4	–	
V_{OL}	Output low voltage	I_{OL} = 9mA	–	0.4	
I_{OH}	Output high current	V_{OH} = 1.5V	–	-6	mA
I_{OL}	Output low current	V_{OL} = 0.3V	–	6	mA
I_L	Input leakage current	V_{IN} = 0V or V_{DD_IO} all signals including output pins in high impedance state	–	±5	µA
		V_{IN} = 3.1V; V_{DD} = 0V, V_{DD_IO} = 0V, V_{AA} = 0V, V_{AA_PIX} = 0V, V_{DD_PLL} = 0V SDATA and SCLK signals only	–	±5	µA

Table 14: I/O Min/Max Parameters (V_{DD_IO} = 2.8V)

Setup conditions: V_{DD} = 2.8V, V_{DD_IO} = 2.8V, V_{AA} = 2.8V, V_{AA_PIX} = 2.8V, V_{DD_PLL} = 2.8V, T_J = -30°C to +70°C, unless specified otherwise

Symbol	Definition	Condition	Min	Max	Unit
V_{IH}	Input high voltage	I_{IH} = -10 µA	2.5	–	V
V_{IL}	Input low voltage	I_{IL} = 10 µA	–	0.3	V
V_{OH}	Output high voltage	I_{OH} = -15mA	V_{DD_IO} - 0.4	–	V
V_{OL}	Output low voltage	I_{OL} = 15mA	–	0.4	V
I_{OH}	Output high current	V_{OH} = 2.5V	–	-11	mA
I_{OL}	Output low current	V_{OL} = 0.3V	–	11	mA
I_L	Input leakage current	V_{IN} = 0V or V_{DD_IO} all signals including output pins in high impedance state	–	±5	µA
		V_{IN} = 3.1V; V_{DD} = 0V, V_{DD_IO} = 0V, V_{AA} = 0V, V_{AA_PIX} = 0V, V_{DD_PLL} = 0V SDATA and SCLK signals only	–	±5	µA

AC Electrical Specification

Figure 8 and Figure 9 illustrate clock and I/O timing and show the timing relationships that are defined in Table 15 on page 22.

Figure 8: Clock Rise and Fall Timing

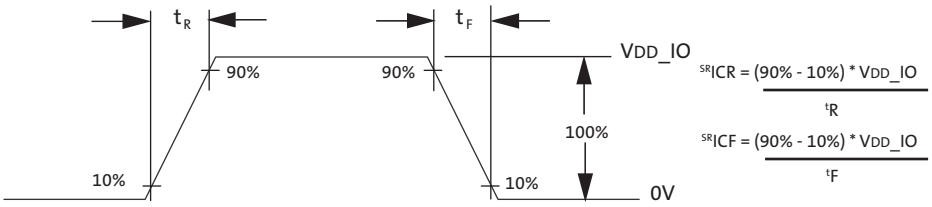
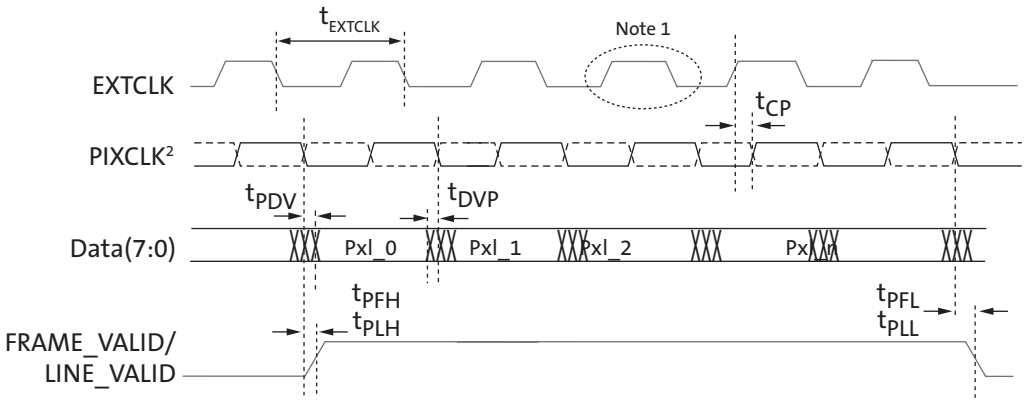


Figure 9: I/O Timing Diagram



Note: 1. See Figure 8 for Rise and Fall Timing details.
2. PLL disabled for tCP. PIXCLK is in phase with EXTCLK with propagation delay of tCP by default (solid line) and could be inverted (dashed line).

Timing Parameters (1.8V)

Table 15 defines timing parameters for the main clocks and the timing relationship between clocks and valid data.

Table 15: I/O Timing Parameters (V_{DD}_IO = 1.8V)[1]

AC Setup Conditions: f_{EXTCLK} = 48 MHz, V_{DD} = 1.8V, V_{DD}_IO = 1.8V, V_{AA} = 2.8V, V_{AA}_PIX = 2.8V, V_{DD}_PLL = 2.8V, Output Load = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL enabled	6	48	54	MHz
$t_{EXTCLK1}$	Input clock period	PLL enabled	18.5	20.8	166.6	ns
$f_{EXTCLK2}$	Input clock frequency	PLL disabled	6	48	54	MHz
$t_{EXTCLK2}$	Input clock period	PLL disabled	18.5	20.8	166.6	ns
$^{SR}ICR^3$	Input clock rising edge slew rate	EXTCLK = 54 MHz	0.70	–	–	V/ns
		EXTCLK = 27 MHz	0.40	–	–	V/ns
		EXTCLK = 13.5 MHz	0.23	–	–	V/ns
$^{SR}ICF^3$	Input clock falling edge slew rate	EXTCLK = 54 MHz	0.70	–	–	V/ns
		EXTCLK = 27MHz	0.40	–	–	V/ns
		EXTCLK = 13.5MHz	0.23	–	–	V/ns
D_{EXTCLK}	Input clock duty cycle	EXTCLK = 54 MHz	45	50	55	%
t_{JITTER}	Input clock jitter	EXTCLK = 54 MHz	–	–	0.15	ns
t_{CP}	EXTCLK to PIXCLK propagation delay	PLL disabled	–	12	–	ns
f_{PIXCLK}	PIXCLK frequency	PLL enabled or disabled	6	48	54	MHz
D_{PIXCLK}	PIXCLK output duty cycle	PLL enabled or disabled	40	50	60	%
t_{PDV}	PIXCLK to data valid		-2	–	2	ns
t_{DVP}	Data valid to PIXCLK		-2	–	2	ns
t_{PFH}	PIXCLK to FV HIGH		-2	–	2	ns
t_{PLH}	PIXCLK to LV HIGH		-2	–	2	ns
t_{PFL}	PIXCLK to FV LOW		-2	–	2	ns
t_{PLL}^2	PIXCLK falling edge to LV falling edge		39.7	–	43.7	ns
f_{VCO}	VCO Frequency		110	–	240	MHz
f_{PFD}	Phase Frequency Detector		2	–	13.75	MHz
C_{IN}	Input signal capacitance		–	3.5	–	pF
C_{LOAD}	Load capacitance		–	–	30	pF

Note:
1. Output signals D_{OUT}(7:0), LINE_VALID (LV), and FRAME_VALID (FV) are not synchronized with PIXCLK and thus may lag or lead PIXCLK. Therefore, t_{PDV}, t_{DVP}, t_{PFH}, t_{PLH}, and t_{PFL} may be positive or negative.
2. Two PIXCLK cycles are missing prior to falling edge of LV. t_{PLL} for PIXCLK = 48 MHz.
3. Slew rates for input clock rising edge (^{SR}ICR) and falling edge (^{SR}ICF) should not differ by more than 10%.

Timing Parameters (2.8V)

Table 16: I/O Timing Parameters (V_{DD}_IO = 2.8V)[1]

AC Setup Conditions: ^{f}EXTCLK = 48 MHz, V_{DD} = 1.8V, V_{DD}_IO = 2.8V, V_{AA} = 2.8V, V_{AA}_PIX = 2.8V, V_{DD}_PLL = 2.8V, Output Load = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}EXTCLK1	Input clock frequency	PLL enabled	6	48	54	MHz
^{t}EXTCLK1	Input clock period	PLL enabled	18.5	20.8	166.6	ns
^{f}EXTCLK2	Input clock frequency	PLL disabled	6	48	54	MHz
^{t}EXTCLK2	Input clock period	PLL disabled	18.5	20.8	166.6	ns
^{SR}ICR[3]	Input clock rising edge slew rate	EXTCLK = 54 MHz	1.10	–	–	V/ns
		EXTCLK = 27 MHz	0.62	–	–	V/ns
		EXTCLK = 13.5 MHz	0.36	–	–	V/ns
^{SR}ICF[3]	Input clock falling edge slew rate	EXTCLK = 54 MHz	1.10	–	–	V/ns
		EXTCLK = 27MHz	0.62	–	–	V/ns
		EXTCLK = 13.5MHz	0.36	–	–	V/ns
^{D}EXTCLK	Input clock duty cycle	EXTCLK = 54 MHz	45	50	55	%
^{t}JITTER	Input clock jitter	EXTCLK = 54 MHz	–	–	0.15	ns
^{t}CP	EXTCLK to PIXCLK propagation delay	PLL disabled	–	12	–	ns
^{f}PIXCLK	PIXCLK frequency	PLL enabled or disabled	6	48	54	MHz
^{D}PIXCLK	PIXCLK output duty cycle	PLL enabled or disabled	40	50	60	%
^{t}PDV	PIXCLK to data valid		-2	–	2	ns
^{t}DVP	Data valid to PIXCLK		-2	–	2	ns
^{t}PFH	PIXCLK to FV HIGH		-2	–	2	ns
^{t}PLH	PIXCLK to LV HIGH		-2	–	2	ns
^{t}PFL	PIXCLK to FV LOW		-2	–	2	ns
^{t}PLL[2]	PIXCLK falling edge to LV falling edge		39.7	–	43.7	ns
^{f}VCO	VCO Frequency		110	–	240	MHz
^{f}PFD	Phase Frequency Detector		2	–	13.75	MHz
C_{IN}	Input signal capacitance		–	3.5	–	pF
C_{LOAD}	Load capacitance		–	–	30	pF

Note:
1. Output signals D_{OUT}(7:0), LINE_VALID (LV), and FRAME_VALID (FV) are not synchronized with PIXCLK and thus may lag or lead PIXCLK. Therefore, ^{t}PDV, ^{t}DVP, ^{t}PFH, ^{t}PLH, and ^{t}PFL may be positive or negative.
2. Two PIXCLK cycles are missing prior to falling edge of LV. ^{t}PLL for PIXCLK = 48 MHz.
3. Slew rates for input clock rising edge (^{SR}ICR) and falling edge (^{SR}ICF) should not differ by more than 10%.

Output Signal Slew Rate Control (1.8V)

Table 17 and Table 18 show the codes for adjusting the slew rate of output signals.

Table 17: Output Signal Slew Rate (1.8V)
Setup conditions: V_{DD}_IO = 1.8V, Output Load C_{LOAD} = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Signals	Parameter	Definition	Min	Typ	Max	Unit
DOUT[7:0], FV, LV, FLASH, SHUTTER, PIXCLK, SDATA	SRHL, SRLH	Output slew rate, code 0, Slowest	0.12	–	0.14	V/ns
		Code 1	0.13	–	0.16	
		Code 2	0.14	–	0.17	
		Code 3	0.16	–	0.19	
		Code 4	0.18	–	0.22	
		Code 5	0.20	–	0.25	
		Code 6	0.24	–	0.29	
		Code 7, Fastest	0.30	–	0.35	

Output Signal Slew Rate Control (2.8V)

Table 18: Output Signal Slew Rate (2.8V)
Setup conditions: V_{DD}_IO = 2.8V, Output Load C_{LOAD} = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Signals	Parameter	Definition	Min	Typ	Max	Unit
DOUT[7:0], FV, LV, FLASH, SHUTTER, PIXCLK, SDATA	SRHL, SRLH	Output slew rate, code 0, Slowest	0.32	–	0.35	V/ns
		Code 1	0.37	–	0.41	
		Code 2	0.42	–	0.46	
		Code 3	0.48	–	0.52	
		Code 4	0.58	–	0.63	
		Code 5	0.73	–	0.78	
		Code 6	0.97	–	1.05	
		Code 7, Fastest	1.65	–	1.73	

Two-Wire Serial Interface Specification

The following diagrams illustrates the Two-Wire Serial Interface bus timing.

Figure 10: Two-Wire Serial Interface Timing Diagram

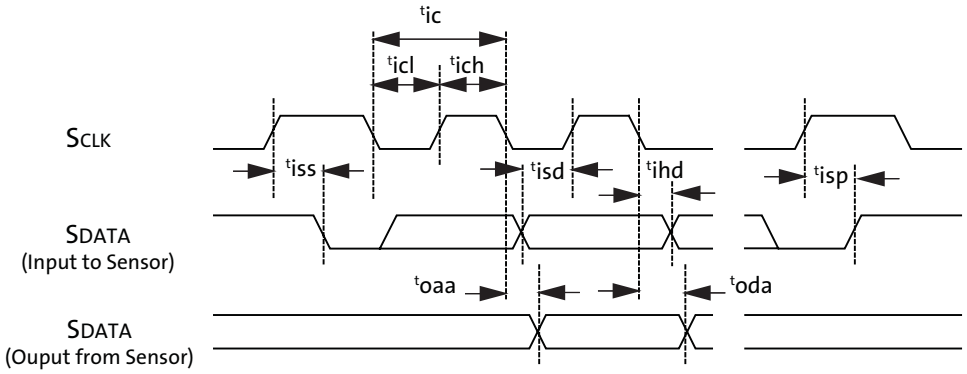


Figure 11: Two-Wire Serial Interface Start and Stop Condition Timing

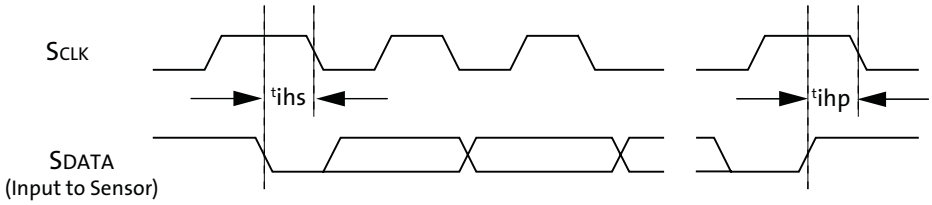


Table 19: Two-Wire Serial Interface Timing

^{f}SCLK = 400 KHz, V_{DD} = 1.8V, V_{AA} = 2.8V, V_{AA_PIX} = 2.8V, V_{DD_IO} = 2.8V, T_J = -30°C to +70°C, unless otherwise specified.

SYMBOL	DEFINITION	Min	Typ	Max	Unit
^{f}SCLK	Two-Wire Serial Interface Input clock frequency			400	KHz
^{t}ic	Two-Wire Serial Interface Clock period	2500			ns
^{t}ich	Two-Wire Serial Interface Clock period High		1250		ns
^{t}icl	Two-Wire Serial Interface Clock period Low		1250		ns
^{t}iss	Setup time for start condition	625			ns
^{t}ihs	Hold time for start condition	416.7			ns
^{t}isd	Setup time for input data	625			ns
^{t}ihd	Hold time for input data	625			ns
^{t}oaa	Output data acknowledge time			1250	ns
^{t}oda	Output data delay time	1250			ns
^{t}isp	Setup time for stop condition	625			ns
^{t}ihp	Hold time for stop condition	625			ns
^{C}INSI	Serial interface input pin capacitance		3.5		pF
^{C}LOADSD	SDATA max load capacitance			30	pF
^{R}SD	SDATA pull-up resistor		1.5		KΩ

Absolute Maximum Ratings

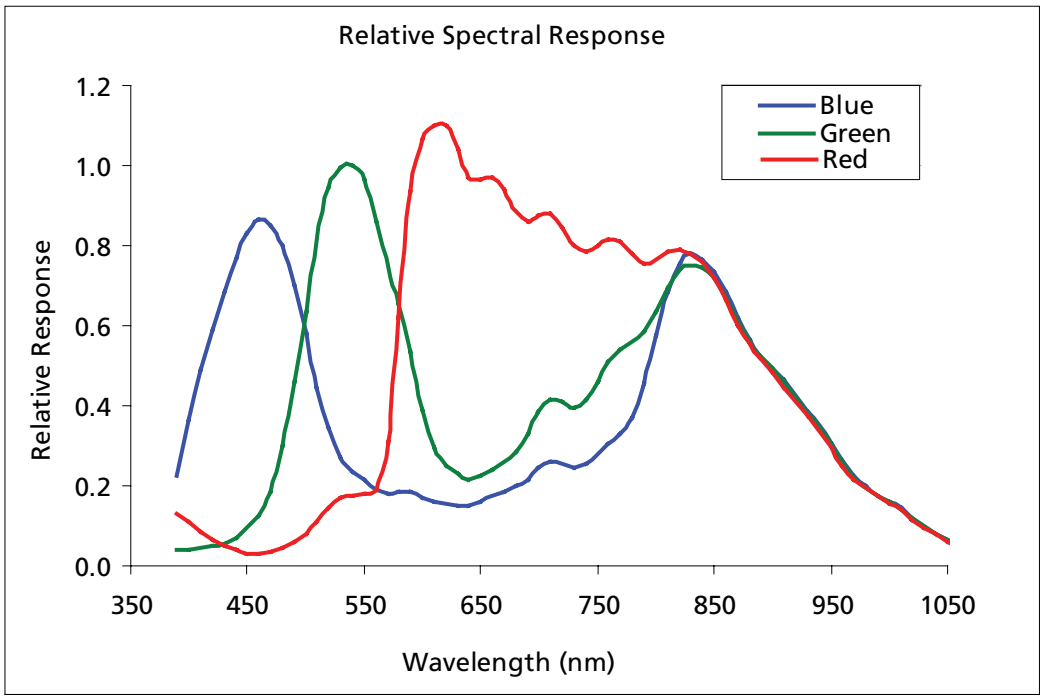
Caution **Stresses greater than those listed in Table 20 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.**

Table 20: Absolute Maximum Ratings

Symbol	Definition	Condition	Min	Max	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	D_{GND} = 0V, A_{GND} = 0V	-0.3	4.0	V
I_{SUPPLY}	Total power supply current		–	150	mA
I_{GND}	Total GND current		–	150	mA
V_{IN}	DC Input voltage	All signals except S_{DATA} and S_{CLK}	-0.3	V_{DD}_IO + 0.3	V
		S_{DATA} and S_{CLK} signals, V_{DD}_IO = 0V	-0.3	3.6	V
V_{OUT}	DC output voltage		-0.3	V_{DD}_IO + 0.3	V
T_{STG}	Storage temperature		-40	+85	°C

Spectral Characteristics

Figure 12: Typical Spectral Characteristics



Revision History

Rev. G 2/8/12

- Updated signal names to conform to current Aptina conventions:
  - changed VDDQ to VDD_IO, RESET# to RESET_BAR, CLKIN to EXTCLK, VDDPLL to VDD_PLL, VAAPIX to VAA_PIX
- Updated trademarks
- Corrected errors in formatting that were introduced in the process of converting the document to non-confidential.

Rev. F 5/10/11

- Updated trademarks
- Applied updated template

Rev. E 5/10

- Updated to non-confidential

Rev. D 5/10

- Updated to Aptina template

Rev. C, Production 5/06

- Added Power Supply Skew, Figure 6 on page 15.
- Added Register R0x2CA (Context Control Program Status and Debug).
- Upgraded Data Sheet to Production.
- Updated power consumption numbers in Table 12 on page 19 from MAX to TYP.
- Update to FLASH description Table 3 on page 10.
- Changed Resize/Zoom to Resize on various pages.
- Added new data (^{f}VCO and ^{f}PFD) to Table 15 on page 22 and Table 16 on page 23.
- Updated Figure 10 on page 25 and Figure 11 on page 25.
- Updated ^{t}oaa to MAX column.
- Updated R0x2C8[13] to Reserved.
- Removed unused registers.

Rev. B, Preliminary 12/05

- Updated register summary, see "Sensor Core Registers – Summary" on page 1
- Updated detailed register tables, see "Page 0: Sensor Core Register Descriptions" on page 1, "Page 1: Image Processing Register Descriptions" on page 1 and "Page 2: Camera Control Register Descriptions" on page 1
- Updated electrical specifications, see "Electrical Specifications" on page 19

Rev. A, Advance 4/05

- Initial release

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