1/6-Inch System-on-a-Chip (SOC) CMOS Digital Image Sensor Die

MT9M113 Die Data Sheet

For the product data sheets, refer to Aptina's Web site: www.aptina.com

Features

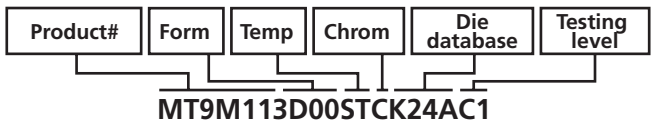
- Superior low-light performance
- Ultra low-power, low-cost sensor
- Internal master clock generated by on-die phase lock loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single die camera module
- Automatic image correction and enhancement, including four-channel lens shading correction
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, 565RGB, 555RGB, 444RGB, processed Bayer, RAW8-bit, and RAW10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate
- Parallel and serial MIPI data output
- Xenon and LED flash support with fast exposure adaptation
- Independently configurable gamma correction

Applications

- Cellular phones
- PC cameras
- PDAs

Order Information

Die: MT9M113D00STCK24AC1



Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database

- Die outline, see Figure 2 on page 10
- Singulated die size (nominal dimension): 4,807µm ±25µm x 5,307µm ±25µm
- Bond Pad Location and Identification Tables, see 6–9

Options

- Form
  - Die — D
- Testing
  - Standard (level 1) probe — C1

General Physical Specifications

- Die thickness: 200µm ±12µm *(Consult factory for other die thickness)*
- Back side die surface of bare silicon
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 3.1kÅ
- Typical metal 4 thickness: 4.15kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Key Performance Parameters

- Optical format: 1/6-inch (5:4)
- Full resolution: 1280 x 1024 pixels (SXGA)
- Pixel size: 1.75µm x 1.75µm
- Dynamic range: 66dB
- SNR MAX: 38.5dB
- Responsivity: 0.54 V/lux-sec
- Chief ray angle: 24.63° maximum at 90 percent image height
- Color filter array: RGB Bayer pattern

Key Performance Parameters (continued)

- Active pixel array area: 2.28mm x 1.83mm, 2.92mm diagonal
- Shutter type: electronic rolling shutter (ERS)
- Input clock frequency: 8–48 MHz
- Maximum frame rate
  - 15 fps at full resolution
  - 30 fps in preview mode
  - 30 fps in video mode
- Maximum pixel data output: 30 Mp/s
- Maximum pixel clock frequency: 60 MHz
- Supply voltage
  - Analog: 2.5–3.1V
  - Digital: 1.7–1.95V
  - I/O: 1.7–3.1V
  - PLL: 2.5–3.1V
  - MIPI: 1.7–1.95V
- ADC resolution: 10-bit, on-die
- Power consumption
  - 222mW at 15 fps, full resolution
  - 156mW at 30 fps, video mode
  - 112mW at 20 fps, preview mode
  - 50µW standby
- Operating temperature: –30°C to +70°C (at junction)

General Description

The Aptina® MT9M113 is a 1/6-inch 1.3Mp CMOS image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), and both parallel and serial MIPI interfaces. It also includes a one-time programmable (OTP) memory for storing module specific information for identification purposes. The microcontroller manages all components of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1324 x 1068 pixels (full resolution is 1280 x 1024 pixels), programmable timing and control circuitry, including a PLL and external flash support, analog signal chain with automatic offset correction and programmable gain, and a 10-bit analog-to-digital converter (ADC). The entire system-on-a-chip (SOC) has ultra low-power requirements and superior low-light performance that is particularly suitable for mobile applications. The MT9M113 is based on Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, power consumption, and integration advantages of CMOS.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's characterization package. Because the package environment is not within Aptina's control, the user must determine the necessary heat-sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9M113 die has 60 bond pads. Refer to Table 1 and Table 2 on pages 6–9 for a complete list of bond pads and coordinates.

The MT9M113 die does not require the user to determine bond option features. The die also has several pads defined as "do not use." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

All DGND pads must be tied together, as must all AGND pads, all GND_IO pads, all VDD pads, all VDD_IO pads, all VAA pads, and all VAA_PIX pads. VDDIO_TX must be tied to VDD.

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connections

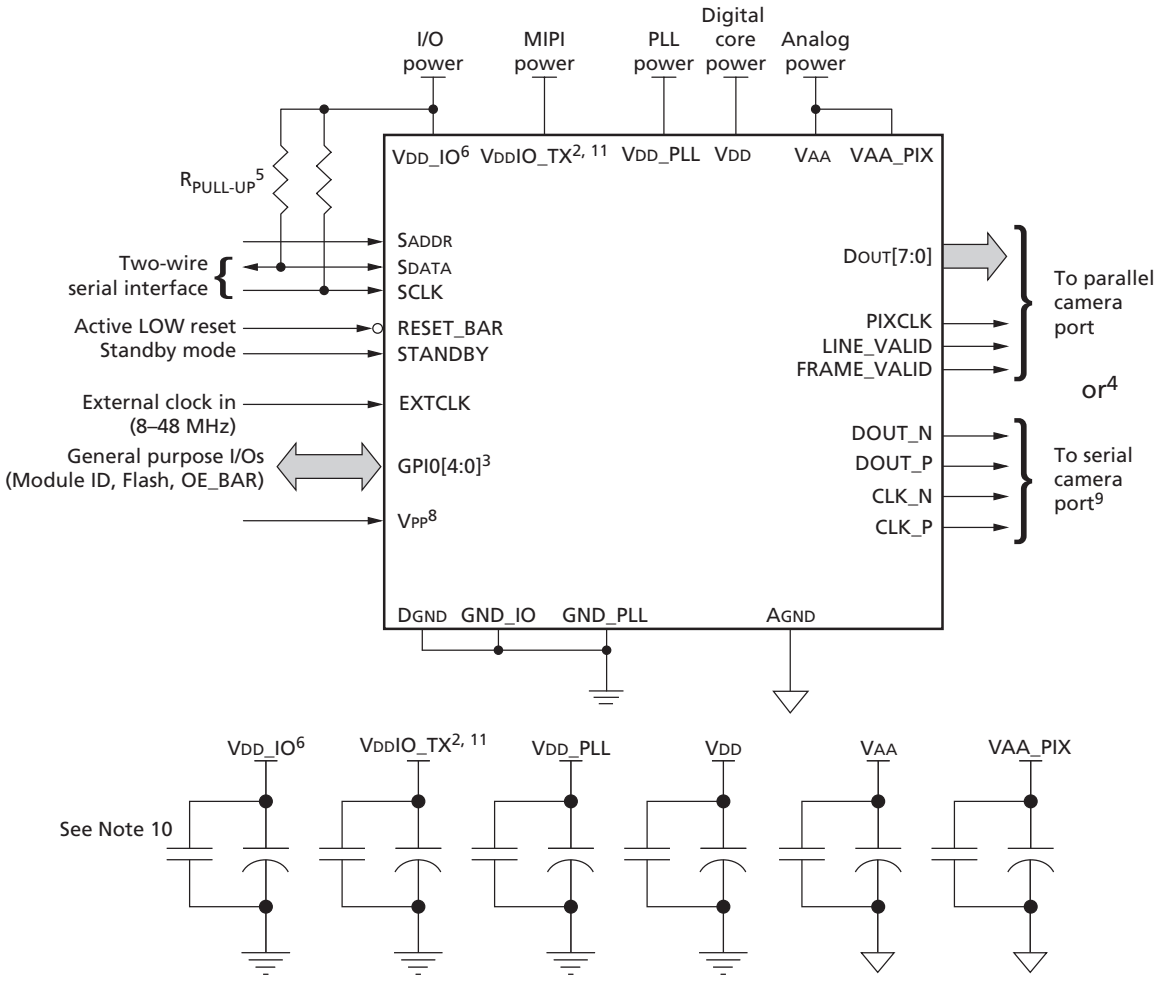
Figure 1 on page 5 shows typical MT9M113 device connections. For low-noise operation, the MT9M113 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9M113 also supports different digital core power (VDD/DGND), MIPI power (VDDIO_TX), and I/O power (VDD_IO/GND_IO). These are power domains that can be at different voltages. PLL requires a clean power source (VDD_PLL/GND_PLL).

Whether the MIPI output is used, Aptina recommends connecting the power supply for the MIPI interface, VDDIO_TX, to the VDD power supply.

AGND and DGND are not connected internally (inside the die).

Figure 1: Typical Configuration (Connection)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI interface is not required, the following pads must be left floating: DOUT_P, DOUT_N, CLK_P, and CLK_N.
3. The GPIO pads can serve multiple features that can be reconfigured. The function and direction will vary by applications.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface $R_{PULL-UP}$; however, greater values may be used for slower transmission speed. $R_{PULL-UP}$ refers to both resistors.
6. All inputs must be configured with VDD_IO.
7. VAA and VAA_PIX must be tied together.
8. VPP is the one-time programmable (OTP) memory signal and should be left floating during normal operation.
9. Compatible with MIPI specifications only.
10. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
11. Whether the MIPI output is used, Aptina recommends connecting the power supply for the MIPI interface, VDDIO_TX, to the VDD power supply.

Bond Pad Location and Identification Tables

Table 1: Bond Pad Location From Center of Pad 1

Pad	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD1	0.00	0.00	0.0000000	0.0000000
2	FRAME_VALID	340.99	0.00	0.0134246	0.0000000
3	LINE_VALID	547.47	0.00	0.0215537	0.0000000
4	GND_IO4	717.47	0.00	0.0282467	0.0000000
5	VDD_IO5	887.99	0.00	0.0349600	0.0000000
6	DOUT0	1058.51	0.00	0.0416734	0.0000000
7	DOUT1	1264.99	0.00	0.0498026	0.0000000
8	DOUT2	1471.47	0.00	0.0579317	0.0000000
9	DOUT3	1677.95	0.00	0.0660608	0.0000000
10	GND_IO3	1848.47	0.00	0.0727742	0.0000000
11	PIXCLK	2018.93	0.00	0.0794852	0.0000000
12	VDD_IO4	2225.99	0.00	0.0876372	0.0000000
13	DOUT4	2396.51	0.00	0.0943506	0.0000000
14	DOUT5	2602.99	0.00	0.1024797	0.0000000
15	DOUT6	2809.47	0.00	0.1106089	0.0000000
16	DOUT7	3015.95	0.00	0.1187380	0.0000000
17	VDD_IO3	3186.47	0.00	0.1254514	0.0000000
18	GND_IO2	3356.99	0.00	0.1321648	0.0000000
19	GPIO_0	3528.09	0.00	0.1389010	0.0000000
20	GPIO_1	3734.57	0.00	0.1470301	0.0000000
21	GPIO_2	3941.05	0.00	0.1551593	0.0000000
22	DGND4	4299.17	–157.17	0.1692585	–0.0061878
23	VDD4	4299.17	–484.83	0.1692585	–0.0190876
24	VDD_IO2	4299.17	–667.81	0.1692585	–0.0262917
25	GPIO_3	4299.17	–838.33	0.1692585	–0.0330051
26	GPIO_4	4299.17	–1044.81	0.1692585	–0.0411343
27	SADDR	4299.17	–1228.67	0.1692585	–0.0483728
28	RESET_BAR	4299.17	–1398.70	0.1692585	–0.0550669
29	DNU[2]	4299.17	–1566.79	0.1692585	–0.0616846
30	VAA1	4299.17	–1676.99	0.1692585	–0.0660232
31	DNU	4299.17	–1787.19	0.1692585	–0.0703618
32	AGND1	4299.17	–1897.39	0.1692585	–0.0747004
33	DNU	4299.17	–2007.59	0.1692585	–0.0790390
34	VAA2	4299.17	–2129.39	0.1692585	–0.0838343
35	AGND2	4299.17	–2299.39	0.1692585	–0.0905272
36	VAA_PIX1	4299.17	–2469.39	0.1692585	–0.0972201
37	VAA_PIX2	4299.17	–2639.39	0.1692585	–0.1039130

Table 1: Bond Pad Location From Center of Pad 1 (continued)

Pad	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
38	AGND3	4299.17	–2809.39	0.1692585	–0.1106059
39	VAA3	4299.17	–2979.39	0.1692585	–0.1172988
40	VPP	4299.17	–3165.26	0.1692585	–0.1246165
41	SDATA	4299.17	–3506.38	0.1692585	–0.1380465
42	SCLK	4299.17	–3676.90	0.1692585	–0.1447598
43	GND_IO1	4299.17	–3848.52	0.1692585	–0.1515165
44	VDD_IO1	4299.17	–4019.62	0.1692585	–0.1582528
45	STANDBY	4299.17	–4191.30	0.1692585	–0.1650118
46	EXTCLK	4299.17	–4365.30	0.1692585	–0.1718622
47	VDD3	4299.17	–4738.77	0.1692585	–0.1865656
48	DGND3	4299.17	–4909.43	0.1692585	–0.1932846
49	DNU	4012.07	–5066.60	0.1579553	–0.1994724
50	DNU	3862.43	–5066.60	0.1520640	–0.1994724
51	DGND2	–267.44	–4909.43	–0.0105289	–0.1932846
52	VDD2	–267.44	–4729.57	–0.0105289	–0.1862033
53	VDD_PLL	–267.44	–4442.52	–0.0105289	–0.1749024
54	VDDIO_TX	–267.44	–4272.51	–0.0105289	–0.1682091
55	CLK_N	–267.44	–4010.90	–0.0105289	–0.1579093
56	CLK_P	–267.44	–3780.90	–0.0105289	–0.1488541
57	DOUT_N	–267.44	–3550.89	–0.0105289	–0.1397988
58	DOUT_P	–267.44	–3320.89	–0.0105289	–0.1307437
59	GND_PLL	–267.44	–3092.79	–0.0105289	–0.1217634
60	DGND1	–267.44	–157.17	–0.0105289	–0.0061878

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

Table 2: Bond Pad Location From Center of Die (0, 0)

Pad	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD1	–2015.87	2533.30	–0.0793648	0.0997362
2	FRAME_VALID	–1674.88	2533.30	–0.0659402	0.0997362
3	LINE_VALID	–1468.40	2533.30	–0.0578110	0.0997362
4	GND_IO4	–1298.40	2533.30	–0.0511181	0.0997362
5	VDD_IO5	–1127.88	2533.30	–0.0444047	0.0997362
6	DOUT0	–957.36	2533.30	–0.0376913	0.0997362
7	DOUT1	–750.88	2533.30	–0.0295622	0.0997362
8	DOUT2	–544.40	2533.30	–0.0214331	0.0997362
9	DOUT3	–337.92	2533.30	–0.0133039	0.0997362
10	GND_IO3	–167.40	2533.30	–0.0065906	0.0997362
11	PIXCLK	3.06	2533.30	0.0001205	0.0997362
12	VDD_IO4	210.12	2533.30	0.0082724	0.0997362
13	DOUT4	380.64	2533.30	0.0149858	0.0997362
14	DOUT5	587.12	2533.30	0.0231150	0.0997362
15	DOUT6	793.60	2533.30	0.0312441	0.0997362
16	DOUT7	1000.08	2533.30	0.0393732	0.0997362
17	VDD_IO3	1170.60	2533.30	0.0460866	0.0997362
18	GND_IO2	1341.12	2533.30	0.0528000	0.0997362
19	GPIO_0	1512.22	2533.30	0.0595362	0.0997362
20	GPIO_1	1718.70	2533.30	0.0676654	0.0997362
21	GPIO_2	1925.18	2533.30	0.0757945	0.0997362
22	DGND4	2283.30	2376.13	0.0898937	0.0935484
23	VDD4	2283.30	2048.48	0.0898937	0.0806486
24	VDD_IO2	2283.30	1865.49	0.0898937	0.0734445
25	GPIO_3	2283.30	1694.97	0.0898937	0.0667311
26	GPIO_4	2283.30	1488.49	0.0898937	0.0586020
27	SADDR	2283.30	1304.63	0.0898937	0.0513634
28	RESET_BAR	2283.30	1134.60	0.0898937	0.0446693
29	DNU[2]	2283.30	966.51	0.0898937	0.0380516
30	VAA1	2283.30	856.31	0.0898937	0.0337130
31	DNU	2283.30	746.11	0.0898937	0.0293744
32	AGND1	2283.30	635.91	0.0898937	0.0250358
33	DNU	2283.30	525.71	0.0898937	0.0206972
34	VAA2	2283.30	403.91	0.0898937	0.0159020
35	AGND2	2283.30	233.91	0.0898937	0.0092091
36	VAA_PIX1	2283.30	63.91	0.0898937	0.0025161
37	VAA_PIX2	2283.30	–106.09	0.0898937	–0.0041768
38	AGND3	2283.30	–276.09	0.0898937	–0.0108697
39	VAA3	2283.30	–446.09	0.0898937	–0.0175626

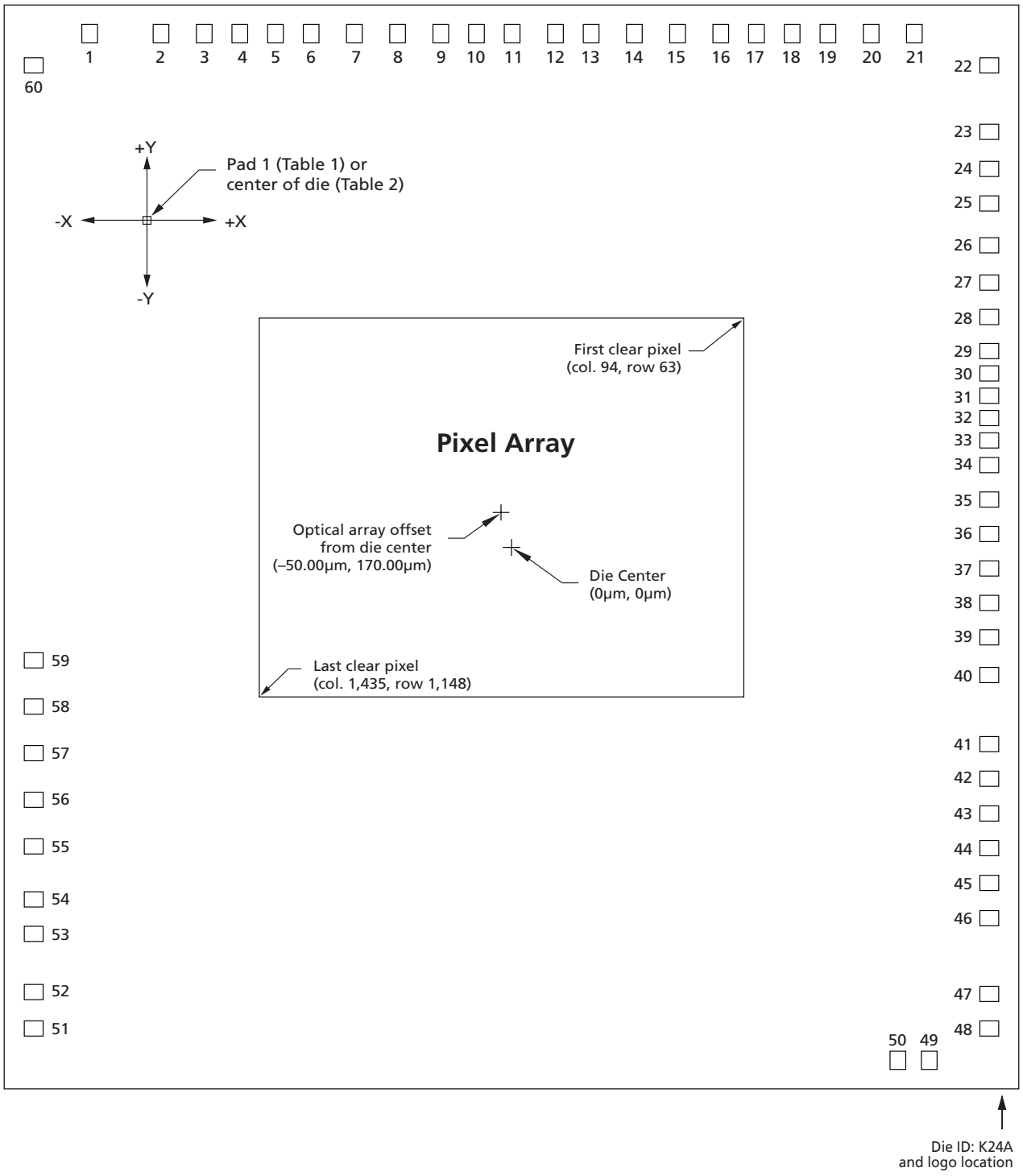
Table 2: Bond Pad Location From Center of Die (0, 0) (continued)

Pad	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
40	VPP	2283.30	–631.96	0.0898937	–0.0248803
41	SDATA	2283.30	–973.08	0.0898937	–0.0383102
42	SCLK	2283.30	–1143.60	0.0898937	–0.0450236
43	GND_IO1	2283.30	–1315.22	0.0898937	–0.0517803
44	VDD_IO1	2283.30	–1486.32	0.0898937	–0.0585165
45	STANDBY	2283.30	–1658.00	0.0898937	–0.0652756
46	EXTCLK	2283.30	–1832.00	0.0898937	–0.0721260
47	VDD3	2283.30	–2205.47	0.0898937	–0.0868293
48	DGND3	2283.30	–2376.13	0.0898937	–0.0935484
49	DNU	1996.20	–2533.30	0.0785906	–0.0997362
50	DNU	1846.56	–2533.30	0.0726992	–0.0997362
51	DGND2	–2283.30	–2376.13	–0.0898937	–0.0935484
52	VDD2	–2283.30	–2196.27	–0.0898937	–0.0864671
53	VDD_PLL	–2283.30	–1909.22	–0.0898937	–0.0751661
54	VDDIO_TX	–2283.30	–1739.21	–0.0898937	–0.0684728
55	CLK_N	–2283.30	–1477.60	–0.0898937	–0.0581730
56	CLK_P	–2283.30	–1247.60	–0.0898937	–0.0491179
57	DOUT_N	–2283.30	–1017.59	–0.0898937	–0.0400626
58	DOUT_P	–2283.30	–787.59	–0.0898937	–0.0310075
59	GND_PLL	–2283.30	–559.49	–0.0898937	–0.0220272
60	DGND1	–2283.30	2376.13	–0.0898937	0.0935484

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use. See "Bonding Instructions" on page 3.
3. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 2: Die Outline (Top View)



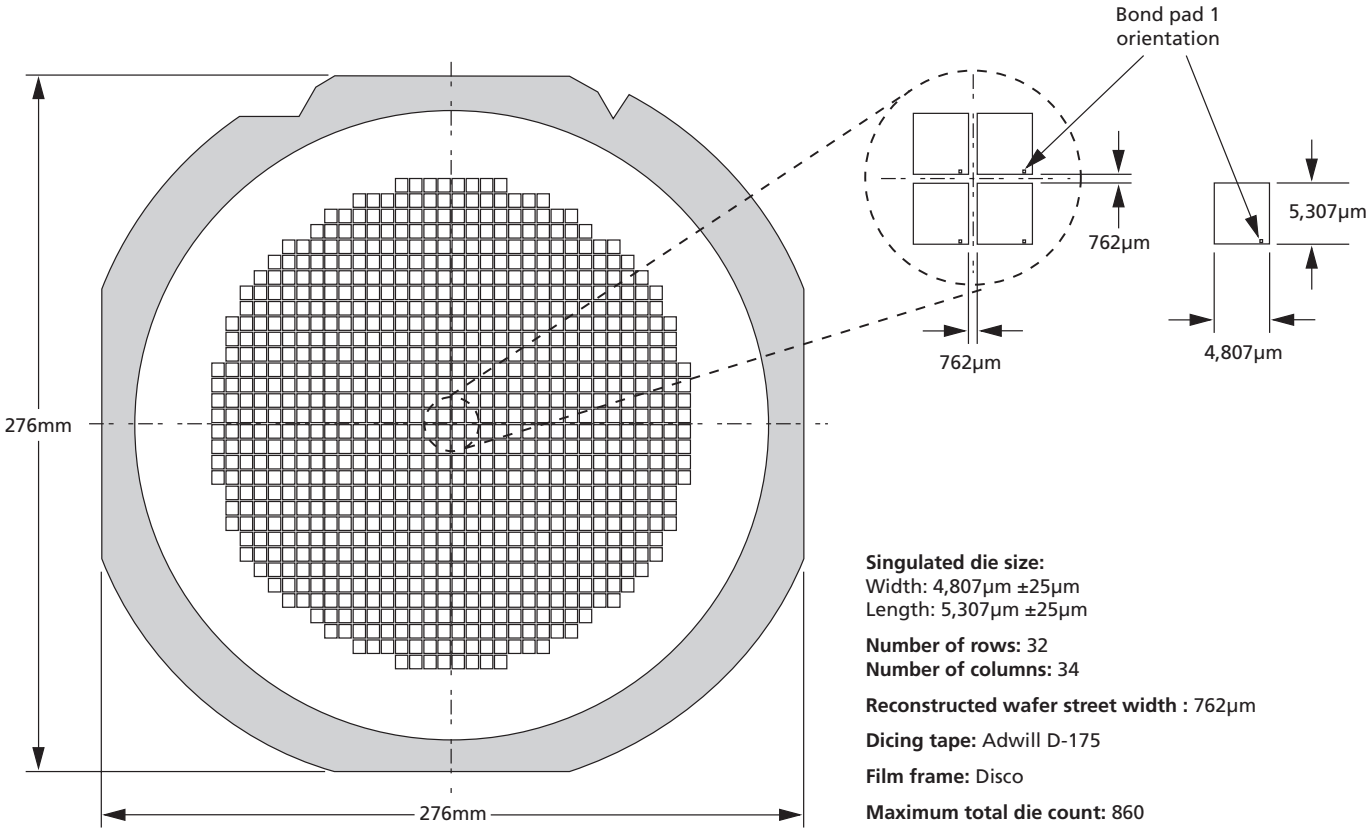
Notes: 1. Figure 2 represents physical orientation of the die only. The image projected is flipped horizontally and vertically by the lens.

Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Die thickness	200µm ±12µm
Singulated die size (after wafer saw) Width (X dimension): Length (Y dimension):	 4,807µm ±25µm 5,307µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch Between any two bond pads:	 110.2µm (4.339 mil)
Clear pixel offset Clear pixel center from die center: Clear pixel center from center of pad 1:	 X = –48.00µm, Y = 170.00µm X = 1,967.87µm, Y = –2,363.30µm
Optical array offset Optical center offset from die center: Optical center offset from center of pad 1:	 X = –50.00µm, Y = 170.00µm X = 1,965.87µm, Y = –2,363.30µm
First clear pixel (col. 94, row 63) From die center: From center of pad 1:	 X = 1,124.63µm, Y = 1,118.90µm X = 3,140.50µm, Y = –1,414.40?m
Last clear pixel (col. 1,435, row 1,148) From die center: From center of pad 1:	 X = –1,220.95µm, Y = –778.90µm X = 794.92µm, Y = –3,312.20µm

Figure 3: MT9M113 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 4,807µm ±25µm
Length: 5,307µm ±25µm

Number of rows: 32
Number of columns: 34

Reconstructed wafer street width : 762µm

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 860

Revision History

Rev. F **5/15/12**

- Updated trademarks

Rev. E **6/10**

- Updated to Aptina template

Rev. D, Preliminary **11/07**

- Updated Figure 1 on page 5
- Added note 11 on connection of VDDIO_TX to Figure 1 on page 5
- Added power consumption numbers to "Key Performance Parameters (continued)" on page 2
- Added wording on connection of VDDIO_TX to "Bonding Instructions" on page 3
- Updated Figure 2 on page 10
- Updated Table 3 on page 11
- Changed designation from Advance to Preliminary
- Updated formats

Rev. C, Advance **4/07**

- Reorganized sections on page 1
- Added DigitalClarity to trademarks

Rev. B, Advance **11/06**

- Added Figure 3 on page 12

Rev. A, Advance **11/06**

- Initial release

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