1/6-Inch 720P High-Definition (HD) System-on-A-Chip (SOC) Digital Image Sensor Die

MT9M114 Die Data Sheet

For the product data sheet, refer to Aptina's Web site: www.aptina.com

Features

- System-on-a-chip (SOC)—Completely integrated camera system
- Ultra low-power, low-cost CMOS image sensor
- Superior low-light performance
- Electronic rolling shutter (ERS)
- Up to 36.7 fps progressive scan for high-quality video at 720p resolution
- On-die image flow processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, zoom
- Image decimation to arbitrary size with smooth, continuous zoom and pan
- Automatic exposure, white balance and black compensation, color saturation, and defect identification and correction, aperture correction
- Two-wire serial programming interface
- Progressive ITU-R BT.656 (YCbCr), YUV, 565RGB, 555RGB, or 444RGB output data formats
- Adaptive Polynominal lens shading correction
- UVC interface
- Perspective correction
- Multi-camera sync

General Physical Specifications

- Die thickness: 200 µm ±12 µm
  (Consult factory for other die thickness)
- Back side die surface of polished bare silicon
- Typical metal 1 thickness: 3.1 kÅ
- Typical metal 2 thickness: 3.1 kÅ
- Typical metal 3 thickness: 3.1 kÅ
- Typical metal 4 thickness: 4.15 kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.2 kÅ nitride over 5.0 kÅ of undoped oxide
- Passivation openings (MIN): 75 µm x 90 µm

Die Database

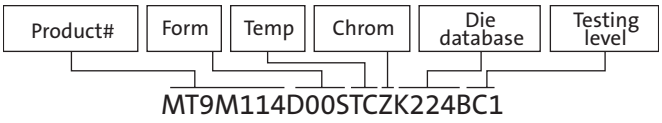
- Die outline, see Figure 2 on page 10
- Singulated die size (nominal dimension):
  3858 µm ±25 µm x 4658 µm ±25 µm
- "Bond Pad Location and Identification Tables", see page 6–8

Order Information

Die: MT9M114D00STCZK24BC1

Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

Options	Designator
• Form	
– Die	D
• Testing	
– Standard (level 1) probe	C1



Key Performance Parameters

- Optical format: 1/6-inch (4:3)
- Active imager size: 2.46 mm(H) x 1.85 mm(V), 3.08 mm diagonal
- Active pixels: 1296 H x 976 V (1.26Mp)
- Pixel size:1.9 µm x 1.9 µm
- Color filter array: RGB Bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Maximum data rate/master clock: 48 MPS/96 MHz
- ADC resolution: 10-bit, on die
- Responsivity: 2.24 V/lux-sec (550 nm)
- Pixel dynamic range: 70.8 dB
- SNR MAX: 37 dB
- Supply voltage:
  - I/O digital: 1.8 V or 2.8 V
  - Core digital: 1.8 V
  - Analog: 2.8 V
  – PLL voltage:2.8V
  – MIPI voltage:1.8V
- Typical power consumption: 135 mW
  (This number excludes power from V_{DD_IO}.)
- Operating temperature: –30°C to +70°C
- Chief ray angle (CRA): 27.7°

General Description

The Aptina MT9M114 die is a 1.26 Mp format 1/6-inch CMOS active-pixel digital image sensor using Aptina's latest digital image flow processor (IFP) technology. The MT9M114 has an active imaging pixel array of 1296 x 976, capturing high-quality color images at 1.26 Mp resolution. The sensor is a complete camera system-on-a-chip solution and is designed specifically to meet the demands of products in PC and Notebook camera applications. It incorporates multiple sophisticated on-die camera functions and is programmable through a simple two-wire serial interface.

This SOC (system-on-a-chip) 1.26 Mp CMOS image sensor die features Aptina's break-through, low-noise CMOS imaging technology that achieves near- CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The MT9M114 die is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed through a parallel 8-bit DOUT or MIPI port as shown in Figure 1 on page 4. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. Output pads can also be tri-stated by de-asserting the OE_BAR signal. The MT9M114 die internal registers can be configured using a two-wire serial interface.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test. Wafer probe is performed at an elevated temperature to test product functionality in Aptina's standard package. Because the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die A/D converter, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9M114 Imager die has 55 bond pads. Refer to Table 1 on page 5 and Table 2 on page 7 for a complete list of bond pads and coordinates.

The MT9M114 Imager die does not require the user to determine bond option features.

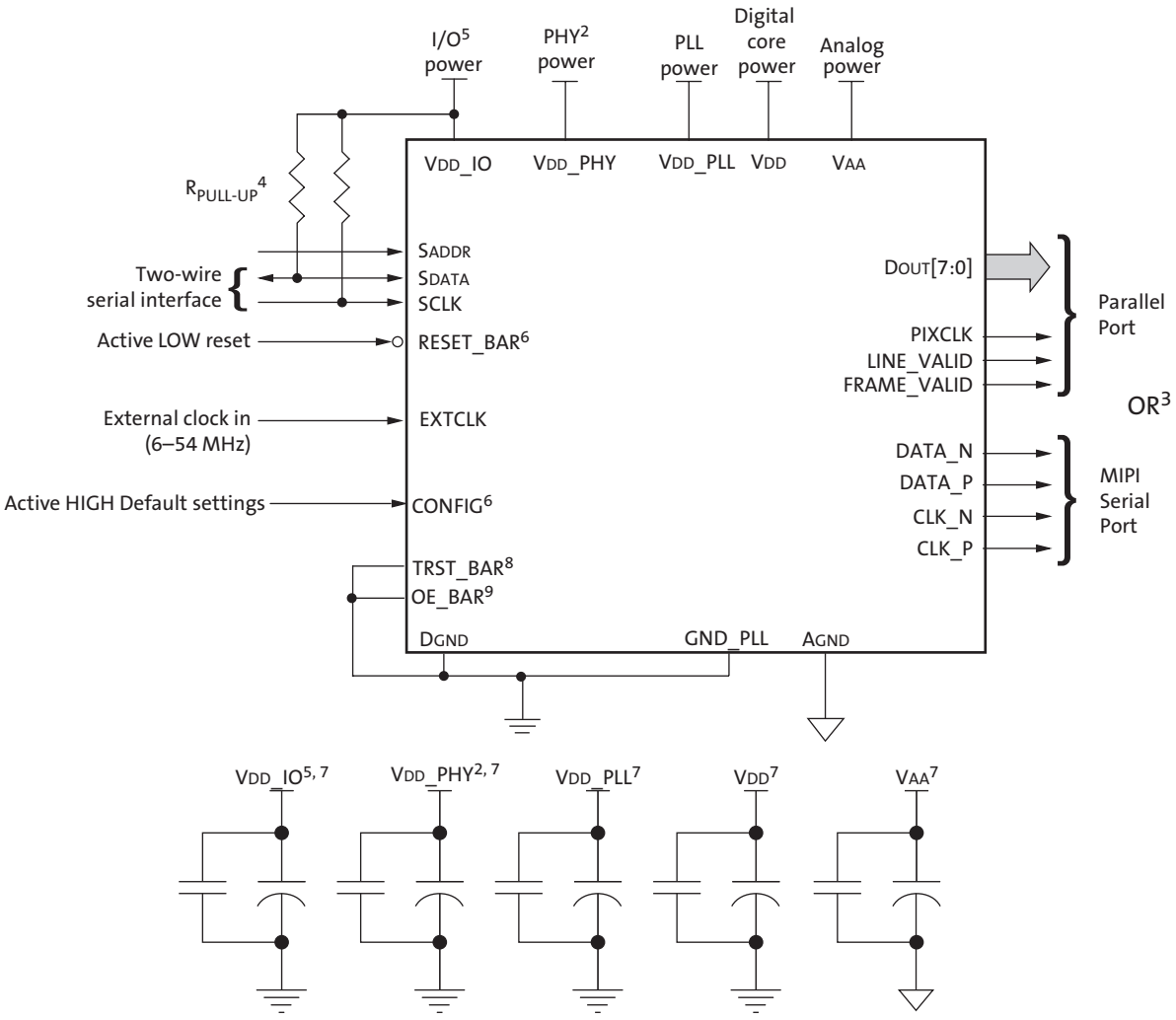
The MT9M114 Imager die also has several pads defined as “do not use.” These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows the MT9M114 typical die connections. For low-noise operation, the MT9M114 die requires separate supplies for analog and digital power.

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Figure 1: Typical Configuration (Connection)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI Interface is not required, the following signals must be left floating: DATA_P, DATA_N, CLK_P, and CLK_N. The VDD_PHY power signal must always be connected to the 1.8V supply.
3. Only one of the output modes (serial or parallel) can be used at any time.
4. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
5. All inputs must be configured with VDD_IO.
6. RESET_BAR and CONFIG both have internal pull-up resistors and can be left floating.
7. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and numbers may vary depending on layout and design considerations.
8. TRST_BAR connects to GND for normal operation.
9. OE_BAR should be connected HIGH when using MIPI interface.

Decoupling Capacitor Recommendations

It is important to provide clean, well-regulated power to each power supply. The customer is ultimately responsible for ensuring that clean power is provided for their own designs because hardware design is influenced by many factors, such as layout, operating conditions, and component selection.

The recommendations for capacitor placement and values listed below are based on our internal demo camera design and verified in hardware.

In order of preference, Aptina recommends:

1. Mount 0.1µF and 1µF decoupling capacitors for each power supply as close as possible to the pad and place a 10 µF capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design (V_{DD}_PLL tied to V_{AA}), use a 0.1µF and 1µF capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 µF capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, use a 1µF capacitor (preferred) or a 0.1 µF capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 µF capacitor for each supply off-module but close to each supply.
4. Give priority to the V_{AA} supply for additional decoupling capacitors.

Inductive filtering components are not recommended.

Follow best practices when performing physical layout. Refer to technical note TN-09-131.

Bond Pad Location and Identification Tables

Table 1: Bond Pad Location and Identification From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	GND_PLL0	0	0	0	0
2	FLASH	4496.98	–129.775	0.177046457	–0.005109252
3	VDD3	4496.98	–279.775	0.177046457	–0.011014764
4	PIXCLK	4496.98	–429.775	0.177046457	–0.016920276
5	EXTCLK	4496.98	–579.775	0.177046457	–0.022825787
6	GND7	4496.98	–729.775	0.177046457	–0.028731299
7	GND6	4496.98	–879.775	0.177046457	–0.034636811
8	Reserved[2]	4496.98	–1029.775	0.177046457	–0.040542323
9	VDD_IO4	4496.98	–1179.775	0.177046457	–0.046447835
10	CHAIN	4496.98	–1329.775	0.177046457	–0.052353346
11	TRST_BAR	4496.98	–1488.28	0.177046457	–0.058593701
12	CONFIG	4496.98	–1642.13	0.177046457	–0.064650787
13	SADDR	4496.98	–1792.13	0.177046457	–0.070556299
14	SCLK	4496.98	–1942.13	0.177046457	–0.076461811
15	VDD2	4496.98	–2092.13	0.177046457	–0.082367323
16	SDATA	4496.98	–2242.13	0.177046457	–0.088272835
17	OE_BAR	4496.98	–2392.13	0.177046457	–0.094178346
18	GND5	4496.98	–2542.13	0.177046457	–0.100083858
19	RESET_BAR	4496.98	–2692.13	0.177046457	–0.10598937
20	Reserved[2]	4153.505	–3464.74	0.163523819	–0.136407087
21	VAA0	3986.4	–3464.74	0.156944882	–0.136407087
22	VAA1	3876	–3464.74	0.152598425	–0.136407087
23	AGND0	3726	–3464.74	0.146692913	–0.136407087
24	AGND1	3615.6	–3464.74	0.142346457	–0.136407087
25	Reserved[2]	3465.6	–3464.74	0.136440945	–0.136407087
26	DOUT7	3248.505	–3464.74	0.127893898	–0.136407087
27	VDD_IO0	3098.505	–3464.74	0.121988386	–0.136407087
28	DOUT6	2948.505	–3464.74	0.116082874	–0.136407087
29	GND0	2798.505	–3464.74	0.110177362	–0.136407087
30	DOUT5	2648.505	–3464.74	0.10427185	–0.136407087
31	DOUT4	2483.975	–3464.74	0.097794291	–0.136407087
32	VDD_IO1	2334.345	–3464.74	0.091903346	–0.136407087
33	DOUT3	2184.345	–3464.74	0.085997835	–0.136407087
34	DOUT2	2019.815	–3464.74	0.079520276	–0.136407087
35	GND1	1870.185	–3464.74	0.073629331	–0.136407087
36	DOUT1	386.21	–3464.74	0.015205118	–0.136407087
37	VDD0	236.21	–3464.74	0.009299606	–0.136407087
38	GND2	0	–3234	0	–0.127322835
39	DOUT0	0	–3076.8	0	–0.121133858
40	VDD_IO2	0	–2919.6	0	–0.114944882
41	FRAME_VALID	0	–2762.4	0	–0.108755906
42	GND8	0	–2605.2	0	–0.102566929
43	LINE_VALID	0	–2448	0	–0.096377953

Table 1: Bond Pad Location and Identification From Center of Pad 1 (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	VDD_IO3	0	–2290.8	0	–0.090188976
45	DOUT_LSB1	0	–2133.6	0	–0.084
46	GND3	0	–1976.4	0	–0.077811024
47	DOUT_LSB0	0	–1819.2	0	–0.071622047
48	VDD1	0	–1662	0	–0.065433071
49	GND4	0	–1504.8	0	–0.059244094
50	VDD_PHY0	0	–1347.6	0	–0.053055118
51	DATA_P	0	–1166.24	0	–0.045914961
52	DATA_N	0	–946.24	0	–0.037253543
53	CLK_N	0	–558.56	0	–0.021990551
54	CLK_P	0	–338.56	0	–0.013329134
55	VDD_PLL0	0	–157.2	0	–0.006188976

Notes: 1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 3.

Table 2: Bond Pad Location and Identification From Center of Die (0,0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	GND_PLL0	–2248.49	1616.45	–0.088523228	0.063639764
2	FLASH	2248.49	1486.675	0.088523228	0.058530512
3	VDD3	2248.49	1336.675	0.088523228	0.052625
4	PIXCLK	2248.49	1186.675	0.088523228	0.046719488
5	EXTCLK	2248.49	1036.675	0.088523228	0.040813976
6	GND7	2248.49	886.675	0.088523228	0.034908465
7	GND6	2248.49	736.675	0.088523228	0.029002953
8	Reserved[2]	2248.49	586.675	0.088523228	0.023097441
9	VDD_IO4	2248.49	436.675	0.088523228	0.017191929
10	CHAIN	2248.49	286.675	0.088523228	0.011286417
11	TRST_BAR	2248.49	128.17	0.088523228	0.005046063
12	CONFIG	2248.49	–25.68	0.088523228	–0.001011024
13	SADDR	2248.49	–175.68	0.088523228	–0.006916535
14	SCLK	2248.49	–325.68	0.088523228	–0.012822047
15	VDD2	2248.49	–475.68	0.088523228	–0.018727559
16	SDATA	2248.49	–625.68	0.088523228	–0.024633071
17	OE_BAR	2248.49	–775.68	0.088523228	–0.030538583
18	GND5	2248.49	–925.68	0.088523228	–0.036444094
19	RESET_BAR	2248.49	–1075.68	0.088523228	–0.042349606
20	Reserved[2]	1905.015	–1848.29	0.075000591	–0.072767323
21	VAA0	1737.91	–1848.29	0.068421654	–0.072767323
22	VAA1	1627.51	–1848.29	0.064075197	–0.072767323
23	AGND0	1477.51	–1848.29	0.058169685	–0.072767323
24	AGND1	1367.11	–1848.29	0.053823228	–0.072767323
25	Reserved[2]	1217.11	–1848.29	0.047917717	–0.072767323
26	DOUT7	1000.015	–1848.29	0.039370669	–0.072767323
27	VDD_IO0	850.015	–1848.29	0.033465157	–0.072767323
28	DOUT6	700.015	–1848.29	0.027559646	–0.072767323
29	GND0	550.015	–1848.29	0.021654134	–0.072767323
30	DOUT5	400.015	–1848.29	0.015748622	–0.072767323
31	DOUT4	235.485	–1848.29	0.009271063	–0.072767323
32	VDD_IO1	85.855	–1848.29	0.003380118	–0.072767323
33	DOUT3	–64.145	–1848.29	–0.002525394	–0.072767323
34	DOUT2	–228.675	–1848.29	–0.009002953	–0.072767323
35	GND1	–378.305	–1848.29	–0.014893898	–0.072767323
36	DOUT1	–1862.28	–1848.29	–0.07331811	–0.072767323
37	VDD0	–2012.28	–1848.29	–0.079223622	–0.072767323
38	GND2	–2248.49	–1617.55	–0.088523228	–0.063683071
39	DOUT0	–2248.49	–1460.35	–0.088523228	–0.057494094
40	VDD_IO2	–2248.49	–1303.15	–0.088523228	–0.051305118
41	FRAME_VALID	–2248.49	–1145.95	–0.088523228	–0.045116142
42	GND8	–2248.49	–988.75	–0.088523228	–0.038927165
43	LINE_VALID	–2248.49	–831.55	–0.088523228	–0.032738189
44	VDD_IO3	–2248.49	–674.35	–0.088523228	–0.026549213

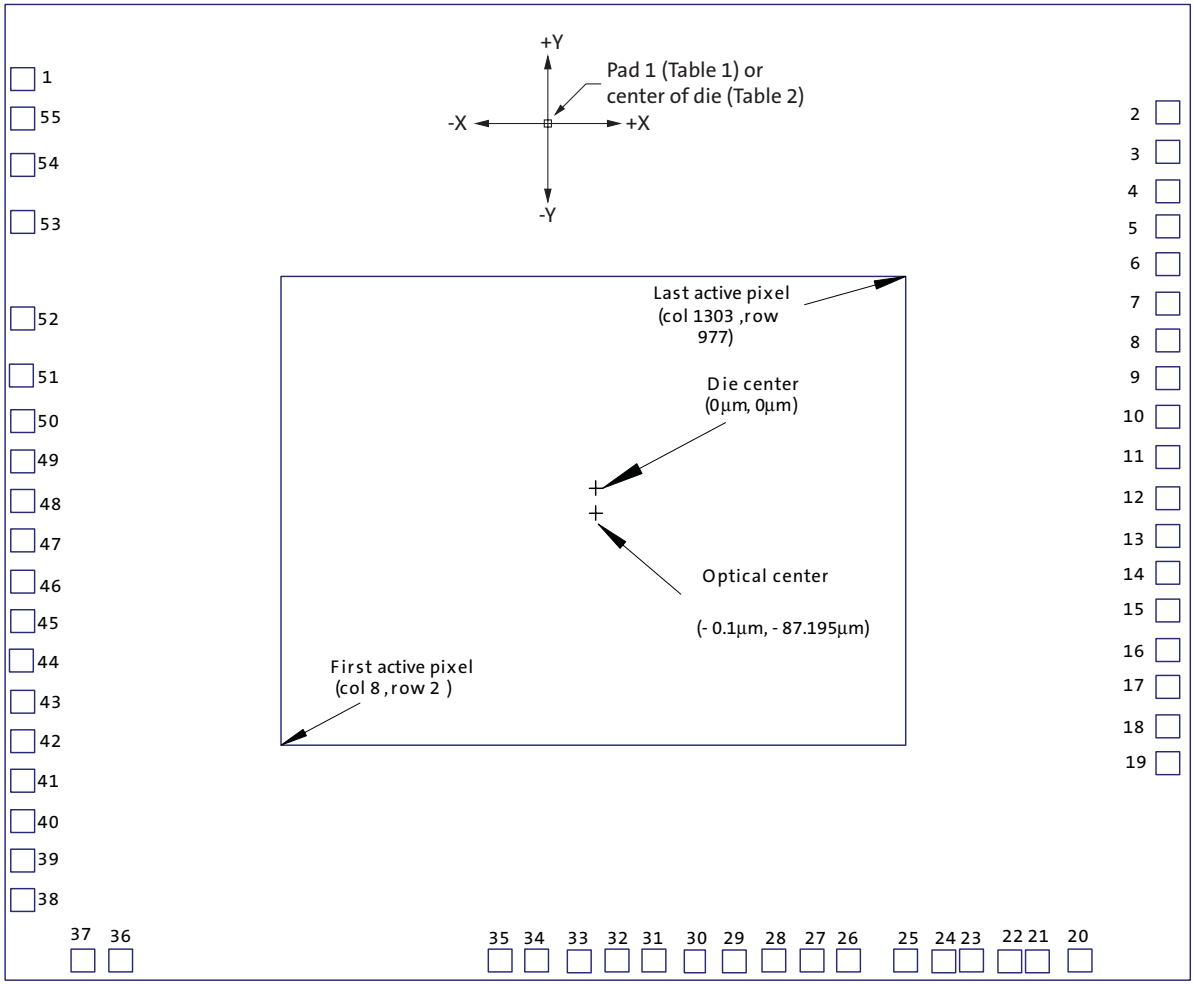
Table 2: Bond Pad Location and Identification From Center of Die (0,0) (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
45	DOUT_LSB1	–2248.49	–517.15	–0.088523228	–0.020360236
46	GND3	–2248.49	–359.95	–0.088523228	–0.01417126
47	DOUT_LSB0	–2248.49	–202.75	–0.088523228	–0.007982283
48	VDD1	–2248.49	–45.55	–0.088523228	–0.001793307
49	GND4	–2248.49	111.65	–0.088523228	0.004395669
50	VDD_PHY0	–2248.49	268.85	–0.088523228	0.010584646
51	DATA_P	–2248.49	450.21	–0.088523228	0.017724803
52	DATA_N	–2248.49	670.21	–0.088523228	0.02638622
53	CLK_N	–2248.49	1057.89	–0.088523228	0.041649213
54	CLK_P	–2248.49	1277.89	–0.088523228	0.05031063
55	VDD_PLL0	–2248.49	1459.25	–0.088523228	0.057450787

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use." See "Bonding Instructions" on page 3.

Die Features

Figure 2: Die Outline (Top View)



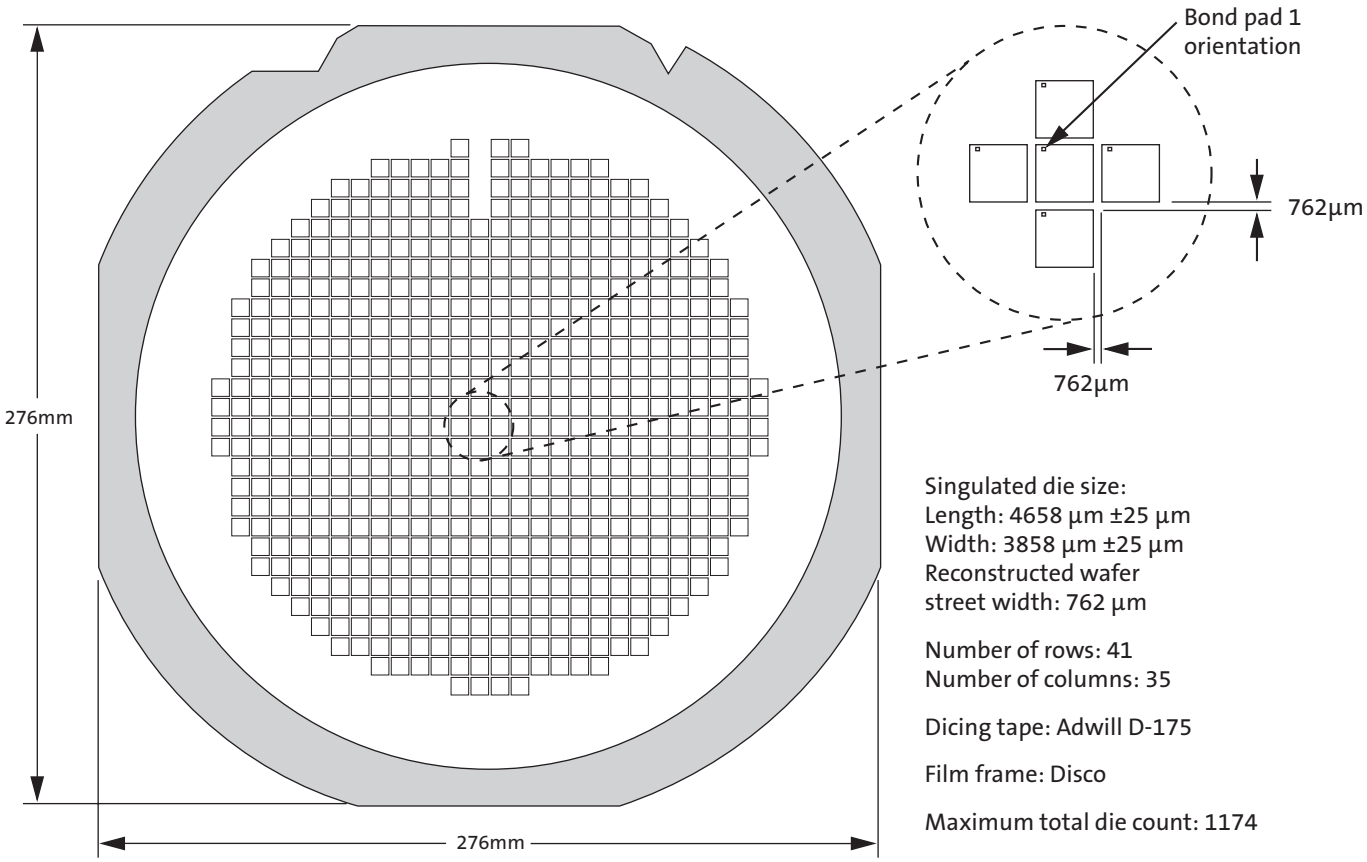
Notes: 1. This figure is not drawn to scale.

Physical Specifications

Table 3: Die Dimensions

Features	Dimensions
Die thickness	200µm ±12µm
Singulated die size Length (X dimension): Width(Y dimension):	 4658 µm ±25 µm 3858 µm ±25 µm
Bond pad size (MIN)	85 µm x 100 µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75 µm x 90 µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	110.4 µm (4.34203 mil)
Optical array Optical center from die center:	 X = –0.1 µm, Y = -87.195 µm
First active pixel (col. 8, row 2) From die center:	 X = –1231.30 µm, Y = –1014.395µm
Last active pixel (col. 1303, row 977) From die center:	 X = 1231.10 µm, Y = 840.005 µm

Figure 3: Die Orientation in Reconstructed Wafer



Singulated die size:
Length: 4658 µm ±25 µm
Width: 3858 µm ±25 µm
Reconstructed wafer
street width: 762 µm

Number of rows: 41
Number of columns: 35

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 1174

Revision History

Rev. F 4/29/11

- Replaced Figure 1 on page 4 and notes with Figure 2 from the data sheet
- Updated Figure 3 on page 11
- Updated Table 3 on page 11

Rev. E 12/10/10

- Updated typical power consumption in “Key Performance Parameters” on page 1
- Updated Figure 2: “ Die Outline (Top View),” on page 10

Rev. D, Production 11/22/10

- Updated to Production
- Applied updated Aptina template
- Updated “Features” on page 1
- Updated “Key Performance Parameters” on page 1
- Updated “Order Information” on page 1
- Updated resolution from 1.2 Mp to 1.26 Mp
- Updated Figure 1: “Typical Configuration (Connection),” on page 4
- Updated Figure 2: “ Die Outline (Top View),” on page 10

Rev. C 11/12/10

- Updated “Key Performance Parameters” on page 1
- • Updated Table 3, “Die Dimensions,” on page 11

Rev. B 8/18/10

- Updated “Key Performance Parameters” on page 1
- • Updated Table 3, “Die Dimensions,” on page 11

Rev. A 9/25/09

- Initial release

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