Electrical Characteristics Data Sheet Addendum

MT9P012

For more information, refer to the data sheet on Micron's Web site: www.micron.com/imaging

Introduction

This document supplements Micron's MT9P012 CMOS digital image sensor preliminary data sheet (Revision B, 07/09/2007) with the register list and default values, and the register descriptions tables. The standard CMOS image sensor data sheet should be referenced for a complete description of this 1/3.2-inch 5Mp digital image sensor.

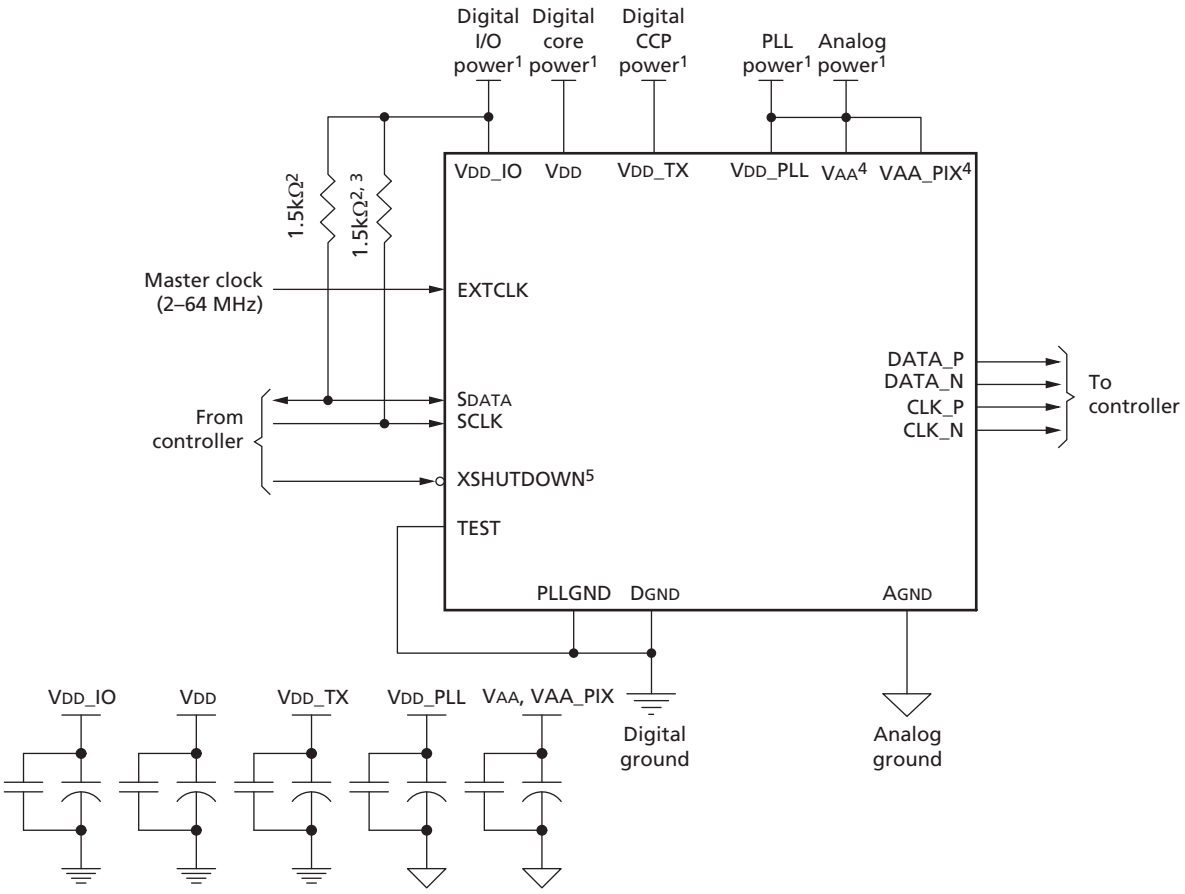
Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/3.2-inch (4:3)
Active imager size		4.54mm(H) x 3.40mm(V) 5.67mm diagonal
Active pixels		2592H x 1944V
Pixel size		1.75 x 1.75µm
Chief ray angle		6°, 15.3°, 22.7°, 25.0°
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS) with global reset release (GRR)
Input clock frequency		2–64 MHz
Maximum data rate	Parallel	96 Mp/s at 96 MHz PIXCLK
	CCP2	650 Mb/s
	MIPI	768 Mb/s per lane
Frame rate	Full resolution (2592 x 1944)	15 fps
	VGA (640 x 480)	640H x 480V with 2X skip and 2X bin: 70 fps
ADC resolution		12-bit, on-die
Responsivity		0.39 V/lux-sec (550nm)
Dynamic range		62.8dB
SNR_{MAX}		40.4dB
Supply voltage	I/O digital	1.7–1.9V (1.8V nominal), or 2.4–3.1V (2.8V nominal)
	Digital	1.7–1.9V (1.8V nominal)
	Analog	2.4–3.1V (2.8V nominal)
Power consumption	Full resolution	534mW at 55°C
	Standby	228µW at 55°C (TYP, EXTCLK disabled)
Package		Bare die
Operating temperature		–30°C to +70°C (at junction)

Typical Connections (CCP)

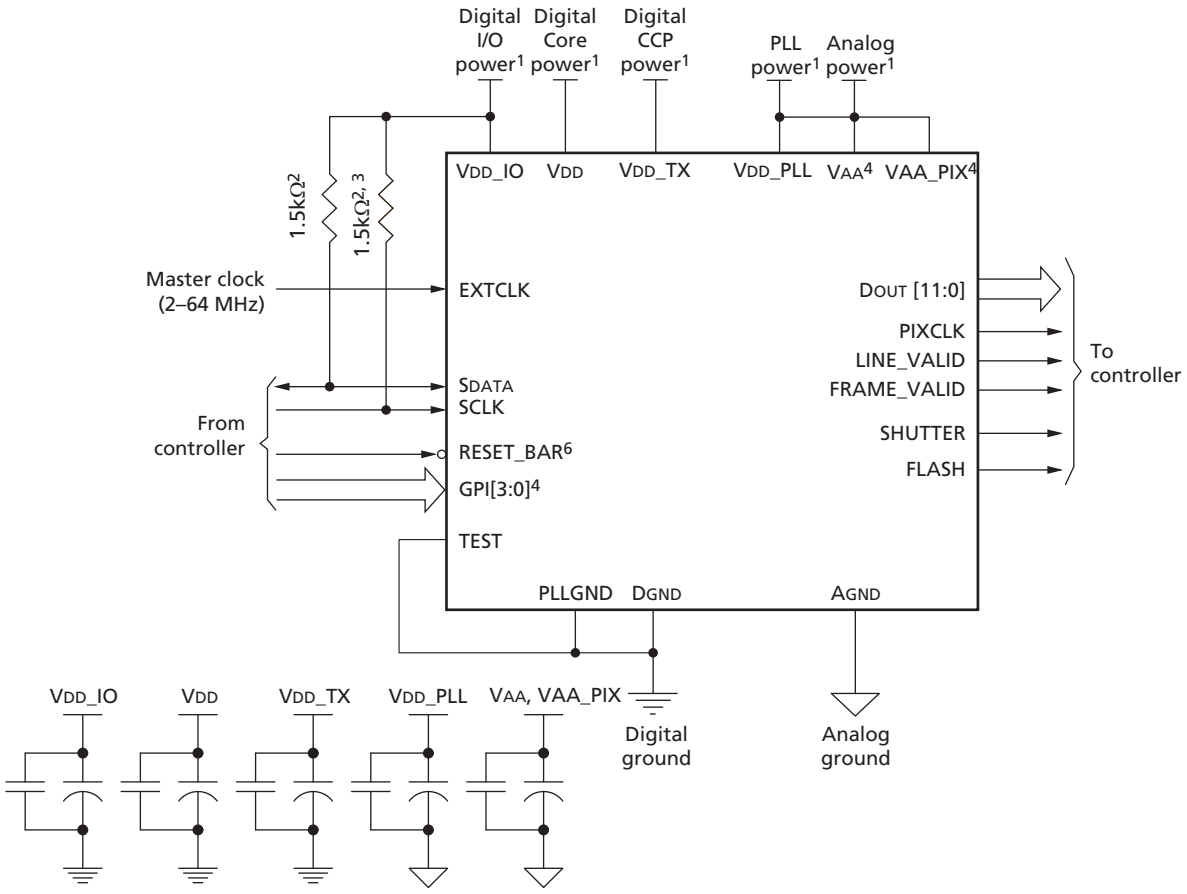
Figure 3 below and Figure 4 on page 3 show typical connection schematics for the MT9P012 die.

Figure 3: Typical Connection: Serial CCP2 Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. Micron recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. Also referred to as RESET_BAR.
6. VPP, which can be used during the module manufacturing process, is not shown in Figure 3. This pad is left unconnected during normal operation.
7. The parallel interface output pads can be left unconnected if the serial output interface is used.
8. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
9. TEST must be tied to DGND.
10. Micron recommends that PLLGND be tied to DGND.
11. VDD_TX must be tied to VDD.

Figure 4: Typical Connection: Parallel Pixel Data Interface (CCP2)

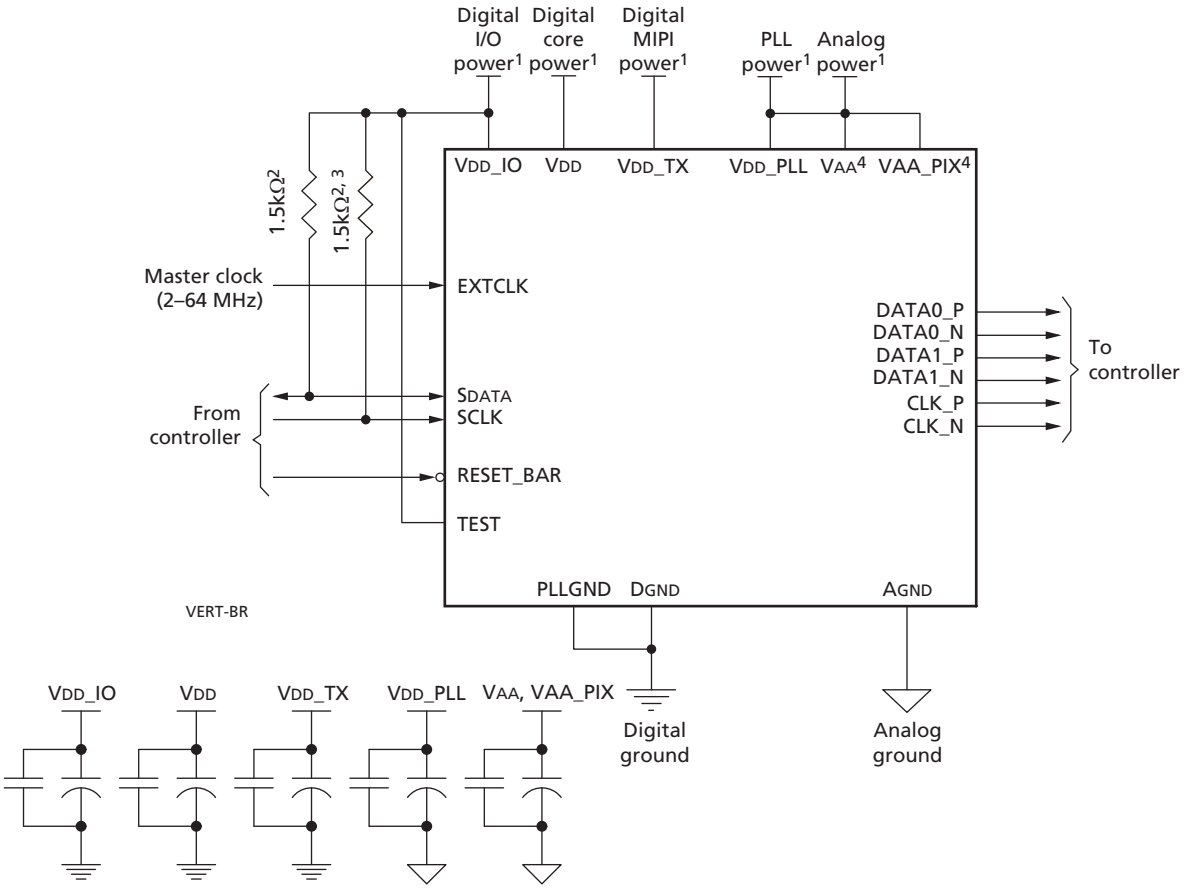


Notes:
1. All power supplies should be adequately decoupled.
2. Micron recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The GPI pins can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_N, SADDR, STANDBY) to be dynamically controlled.
5. VAA and VAA_PIX must be tied together.
6. Also referred to as XSHUTDOWN.
7. VPP, which can be used during the module manufacturing process, is not shown in Figure 4. This pad is left unconnected during normal operation.
8. The serial interface output pads can be left unconnected if the parallel output interface is used.
9. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
10. TEST must be tied to DGND.
11. Micron recommends that PLLGND be tied to DGND.
12. VDD_TX must be tied to VDD.

Typical Connections (MIPI)

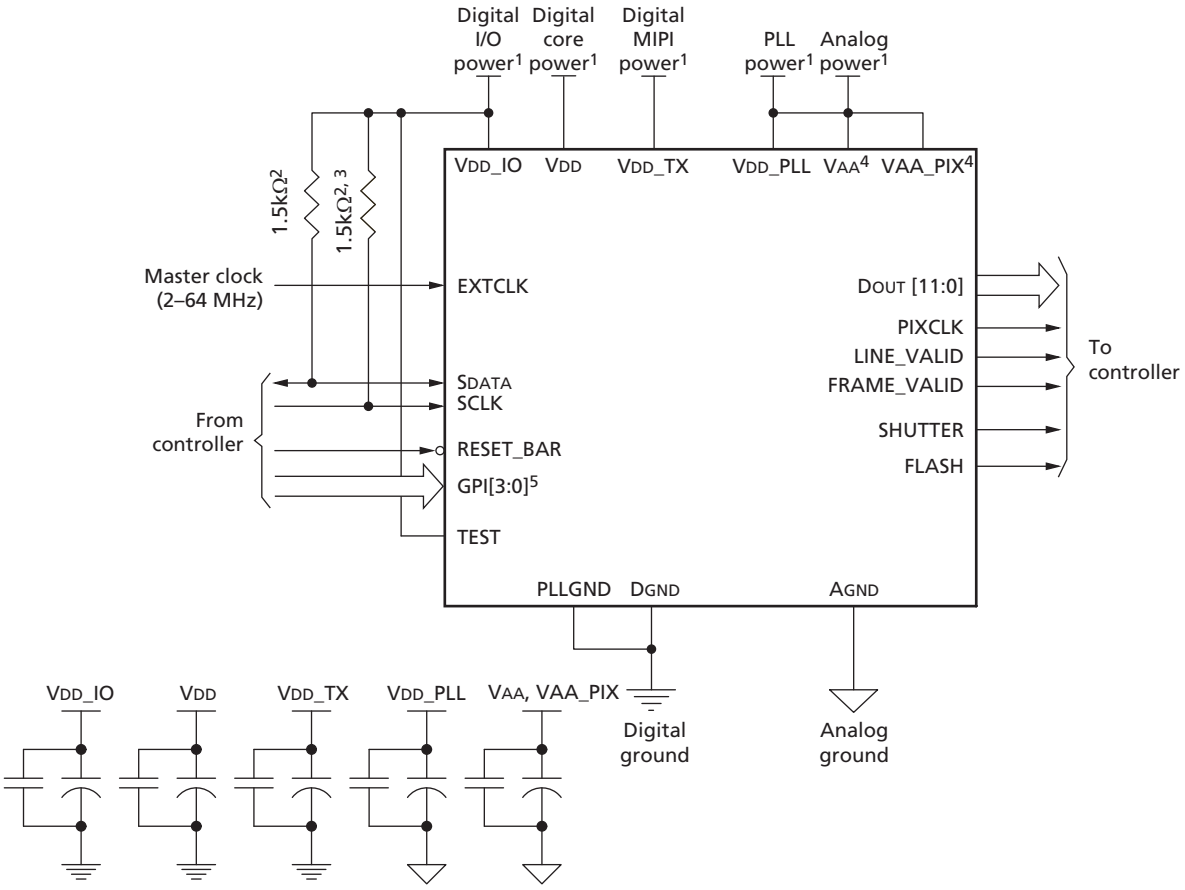
Figure 5 and Figure 6 on page 5 show typical connection schematics for the MT9P012 die.

Figure 5: Typical Connection: Serial MIPI Pixel Data Interface



Notes:
1. All power supplies should be adequately decoupled.
2. Micron recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 5. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
8. TEST must be tied to VDD_IO.
9. Micron recommends that PLLGND be tied to DGND.
10. VDD_TX must be tied to VDD.

Figure 6: Typical Connection: Parallel Pixel Data Interface (MIPI)



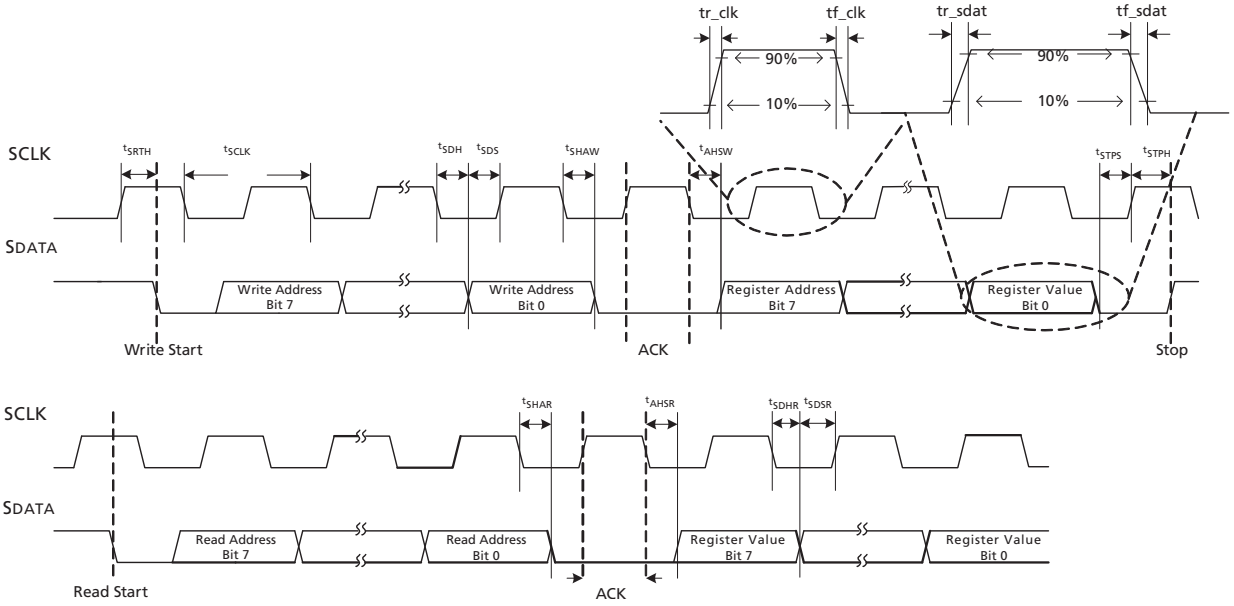
Notes:
1. All power supplies should be adequately decoupled.
2. Micron recommends a resistor value of 1.5kΩ, but a great value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. The GPI pins can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_N, SADDR, STANDBY) to be dynamically controlled.
6. VPP, which can be used during the module manufacturing process, is not shown in Figure 6. This pad is left unconnected during normal operation.
7. The serial interface output pads can be left unconnected if the parallel output interface is used.
8. Micron recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
9. TEST must be tied to VDD_IO.
10. Micron recommends that PLLGND be tied to DGND.
11. VDD_TX must be tied to VDD.

Electrical Characteristics

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 58 and Table 33. The SCLK and SDATA signals feature fail-safe input protection, Schmitt trigger input, and suppression of input pulses of less than 50ns.

Figure 58: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 33: Two-Wire Serial Register Interface Electrical Characteristics

f_{EXTCLK} = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output load = 68.5pF; T_J = 55°C

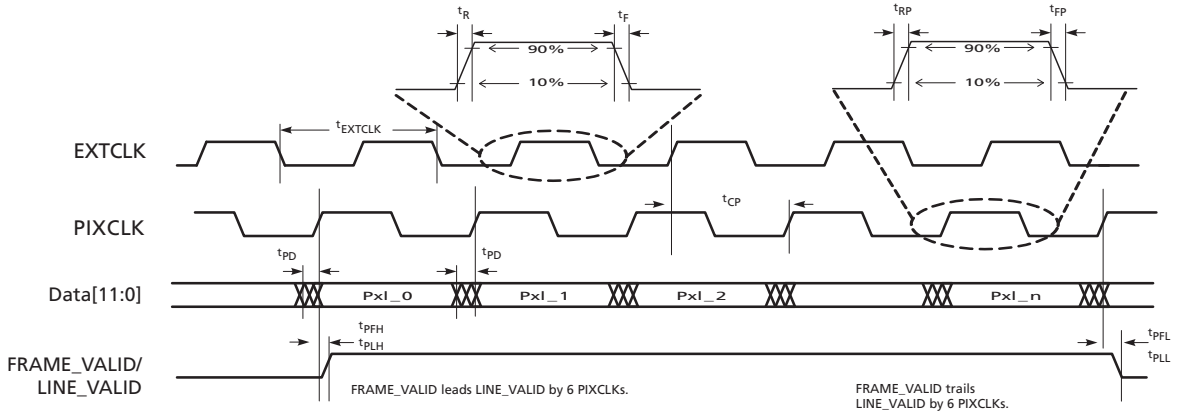
Definition	Condition	Symbol	Min	Typ	Max	Unit
Input LOW voltage		V_{IL}	0.73		0.3 x V_{DD_IO}	V
Input leakage current	No pull up resistor; V_{IN} = V_{DD_IO} or D_{GND}	I_{IN}	–2		2	µA
Output LOW voltage	At specified 3mA	V_{OL}	0.11	0.147	0.275	V
Output LOW current	At specified V_{OL} 0.1V	I_{OL}			3	mA
Input pad capacitance		C_{IN}			6	pF
Load capacitance		C_{LOAD}				pF

Table 34: Two-Wire Serial Register Interface Timing Specification

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output load = 68.5pF; T_J = 55°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock	–	100		400	kHz
^{t}SCLK	Serial interface input period	V_{CMF}	2.5		10	µsec
	SCLK duty cycle	V_{OD}	45	50	60	%
^{t}R	SCLK/SDATA rise time				300	µsec
^{t}SRTS	Start setup time	Master WRITE to slave	0.6			µsec
^{t}SRTH	Start hold time	Master WRITE to slave	0.3			µsec
^{t}SDH	SDATA hold	Master WRITE to slave	0.3		0.65	µsec
^{t}SDS	SDATA setup	Master WRITE to slave	0.3			µsec
^{t}SHAW	SDATA hold to ACK	Master READ to slave	0.15		0.65	µsec
^{t}AHSW	ACK hold to SDATA	Master WRITE to slave	0.15		0.65	µsec
^{t}STPS	Stop setup time	Master WRITE to slave	0.3			µsec
^{t}STPH	Stop hold time	Master WRITE to slave	0.6			µsec
^{t}SHAR	SDATA hold to ACK	Master WRITE to slave	0.3		0.65	µsec
^{t}AHSR	ACK hold to SDATA	Master WRITE to slave	0.3		0.65	µsec
^{t}SDHR	SDATA hold	Master READ from slave	0.3		0.65	µsec
^{t}SDSR	SDATA setup	Master READ from slave	0.3			µsec

Figure 59: Parallel Data Output Timing Diagram



Notes: 1. PLL disabled for ^{t}CP.

EXTCLK

The electrical characteristics of the EXTCLK input are shown in Table 35. The EXTCLK input supports an AC-coupled sine-wave input clock or a DC-coupled square-wave input clock.

If EXTCLK is AC-coupled to the MT9P012 and the clock is stopped, the EXTCLK input to the MT9P012 must be driven to ground or to V_{DD}_IO. Failure to do this will result in excessive current consumption within the EXTCLK input receiver.

Table 35: Electrical Characteristics (EXTCLK)

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD}_IO = 1.8V; V_{AA} = 2.8V; VAA_PIX = 2.8V; V_{DD}_PLL = 2.8V; Output load = 68.5pF; T_J = 55°C

Definition	Condition	Symbol	Min	Typ	Max	Unit
Input clock frequency	PLL enabled	^{f}EXTCLK1	6		48	MHz
Input clock period	PLL enabled	^{t}EXTCLK1	21		167	ns
Input clock rise slew rate		^{t}R	1			V/ns
Input clock fall slew rate		^{t}F	1			V/ns
Input clock minimum voltage swing (AC coupled)		V_{IN_AC}	0.5			V (p-p)
Input clock maximum voltage swing (DC coupled)		V_{IN_DC}			V_{DD}_IO + 0.5	V
Input clock signalling frequency (low amplitude)	V_{IN} = V_{IN_AC} (MIN)	^{t}CLKMAX(AC)			27	MHz
Input clock signalling frequency (full amplitude)	V_{IN} = V_{DD}_IO	^{t}CLKMAX(DC)			48	MHz
Clock duty cycle			45	50	55	%
Input clock jitter	cycle-to-cycle	^{t}JITTER	15.8	20.5	27.4	ps
PLL VCO lock time		^{t}LOCK				ms
Input pad capacitance		C_{IN}				pF
Input HIGH leakage current		I_{IH}	–10		10	µA
Input HIGH voltage		V_{IH}	V_{DD}_IO x 0.7		V_{DD}_IO + 0.5	V
Input LOW voltage		V_{IL}	–0.5		0.3 x V_{DD}_IO	V

Parallel Pixel Data Interface

The electrical characteristics of the parallel pixel data interface (FV, LV, DOUT[11:0], PIXCLK, SHUTTER, and FLASH outputs) are shown in Table 36.

Table 36: Electrical Characteristics (Parallel Pixel Data Interface)

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output Load = 68.5pF; T_J = 55°C

Definition	Condition	Symbol	Min	Typ	Max	Unit
Output HIGH voltage	At specified I_{OH} 8mA	V_{OH}	1.4	1.61	1.63	V
Output LOW voltage	At specified I_{OL} 8mA	V_{OL}	0.06	0.07	0.1	V
Output HIGH current	At specified V_{OH}, V_{DD_IO} = 1.8V	I_{OH}	–14		–12	mA
Output LOW current	At specified V_{OL} = 0.3V	I_{OL}	6		10	mA
Output LOW current	At specified V_{OL} = 0.4V	I_{OL}	8		13	mA
Tri-state output leakage current		I_{OZ}	0.1		0.2	µA
Output pin slew (rising)	Default slew rate register settings, C_{LOAD} = 35pF, 64 MHz PIXCLK			0.29		V/ns
Output pin slew (falling)	Default slew rate register settings, C_{LOAD} = 35pF, 64 MHz PIXCLK			0.4		V/ns
PIXCLK to data valid	60 MHz PIXCLK	^{t}PD		4	16	ns
PIXCLK frequency	Default	^{f}PIXCLK		60	96	MHz
PIXCLK to FV HIGH	60 MHz PIXCLK	^{t}PFH		4	6	ns
PIXCLK to LV HIGH	60 MHz PIXCLK	^{t}PLH		3	5	ns
PIXCLK to FV LOW	60 MHz PIXCLK	^{t}PFL		4	6	ns
PIXCLK to LV LOW	60 MHz PIXCLK	^{t}PLL		4	6	ns

Serial Pixel Data Interface

The electrical characteristics of the serial pixel data interface (CLK_P, CLK_N, DATA0_P, DATA1_P, DATA0_N, and DATA1_N) are shown in Table 37 and Table 38.

To operate the serial pixel data interface within the electrical limits of the CSI-2 and CCP2 specifications, V_{DD}_IO (I/O digital voltage) is restricted to operate in the range 1.7–1.9V.

Table 37: Electrical Characteristics (Serial CCP2 Pixel Data Interface)

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD}_IO = 1.8V; V_{AA} = 2.8V; VAA_PIX = 2.8V; V_{DD}_PLL = 2.8V; Output load = 68.5pF; T_J = 55°C

Definition	Condition	Symbol	Min	Typ	Max	Unit
Operating frequency					650	MHz
Fixed common mode voltage		V_{CMF}		0.85		V
Differential voltage swing		V_{OD}		142.7		mV
Differential current swing						mA
Drive current range						mA
Drive current variation						%
Output impedance				66.3		Ω
Output impedance mismatch				2.5		%
Clock Duty cycle at 416 MHz				51		%
Rise time (20–80%)		^{t}R		198.2		ps
Fall time (20–80%)		^{f}R		201.3		ps
Differential skew				26.2		ps
Channel to channel skew					100	ps
Maximum data rate Data/strobe mode Data/clock mode					 650 208	Mb/s
Power supply rejection ratio (0–100 MHz)						

Table 38: Electrical Characteristics (Serial MIPI Pixel Data Interface)

[f]EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output Load = 68.5pF; T_J = 55°C

Definition	Symbol	Min	Typ	Max	Unit
High speed transmit differential voltage	V_{OD}			152	mV
High speed transmit static common-mode voltage	V_{CMTX}			213.7	mV
V_{OD} mismatch when output is Differential-1 or Differential-0	ΔV_{OD}			0.63	mV
High speed output HIGH voltage	ΔV_{CMTX}			0.44	mV
Single ended output impedance	Z_{OS}			185.4	Ω
Single ended output impedance mismatch	ΔZ_{OS}			54.26	Ω
Common-level variation between 50–450 MHz	$\Delta V_{CMTX(L,F)}$			4.24	%
Rise time (20–80%)	^tR			363.7	ps
Fall time (20–80%)	^tF			346.5	ps
Output LOW level	V_{OL}			22.4	mV
Output HIGH level	V_{OH}			1.2	V
Output impedance of low power parameter	Z_{OLP}			104.7	Ω
15–85% rise time	T_{RLP}			3.8	ns
15–85% fall time	T_{FLP}			6.3	ns
Slew rate (C_{LOAD} = 5–20pF)	Δv/Δdtsr			293.5	mV/ns
Slew rate (C_{LOAD} = 20–70pF)	Δv/Δdtsr			148.1	mV/ns

Control Interface

The electrical characteristics of the control interface (RESET_BAR, TEST, GPI0, GPI1, GPI2, and GPI3) are shown in Table 39.

Table 39: DC Electrical Characteristics (Control Interface)

^{f}EXTCLK = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output load = 68.5pF; T_J = 55°C

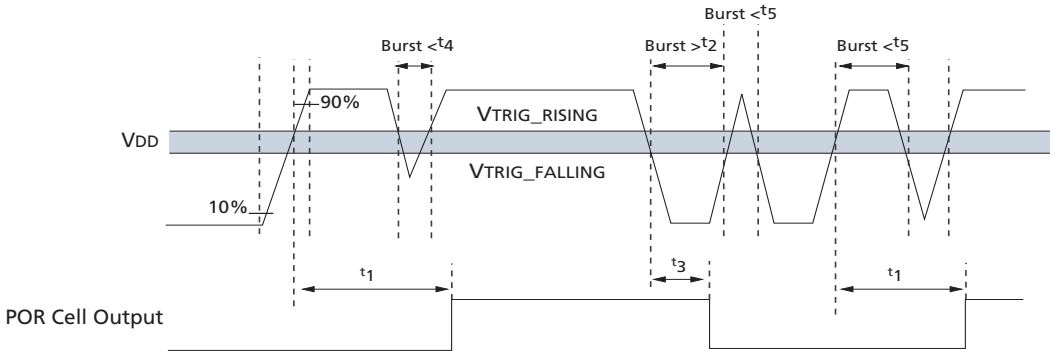
Definition	Condition	Symbol	Min	Typ	Max	Unit
Input HIGH voltage		V_{IH}	0.7 x V_{DD_IO}		V_{DD_IO} + 0.5	V
Input LOW voltage		V_{IL}	–0.5		0.3 x V_{DD_IO}	V
Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	I_{IN}	–10	0.147	10	µA
Input pad capacitance		C_{IN}				pF

Power-On Reset

Table 40: Power-On Reset Characteristics

Definition	Condition	Symbol	Min	Typ	Max	Unit
VDD rising, crossing VTRIG_RISING; Internal reset being released		t_1				µs
VDD falling, crossing VTRIG_FALLING; Internal reset active		t_2				µs
Minimum VDD spike width below VTRIG_FALLING; considered to be a reset when POR cell output is HIGH		t_3				µs
Minimum VDD spike width below VTRIG_FALLING; considered to be a reset when POR cell output is LOW		t_4				µs
Minimum VDD spike width above VTRIG_RISING; considered to be a stable supply when POR cell output is LOW	While the POR cell output is LOW, all VDD spikes above VTRIG_RISING less than t_5 must be ignored	t_5				ns
VDD rising trigger voltage		VTRIG_RISING				V
VDD falling trigger voltage		VTRIG_FALLING				V

Figure 60: Internal Power-On Reset



Operating Voltages

VAA and VAA_PIX must be at the same potential for correct operation of the MT9P012.

Table 41: DC Electrical Definitions and Characteristics

[f]EXTCLK = 24 MHz; VDD = 1.8V; VDD_IO = 1.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; Output Load = 68.5pF; TJ = 55°C

Definition	Condition	Symbol	Min	Typ	Max	Unit
Core digital voltage		VDD	1.7	1.8	1.9	V
I/O digital voltage	Parallel pixel data interface	VDD_IO	1.7/2.4	1.8/2.8	1.9/3.1	V
Analog voltage		VAA	2.4	2.8	3.1	V
Pixel supply voltage		VAA_PIX	2.4	2.8	3.1	V
PLL supply voltage		VDD_PLL	2.4	2.8	3.1	V
Digital operating current	Streaming, full resolution		55.98	59.58	59.92	mA
I/O digital operating current	Streaming, full resolution		10.23/24.21	11.65/25.69	12.66/26.69	mA
Analog operating current	Streaming, full resolution		121.06	124.98	127.24	mA
Pixel supply current	Streaming, full resolution		1.57	1.60	1.62	mA
PLL supply current	Streaming, full resolution		14.60	18.50	20.50	mA
Hard standby (clock on)	Analog			42		µA
	Digital			1240/1380		µA
Hard standby (clock off)	Analog			12		µA
	Digital			73/81		µA
Soft standby (clock on)	Analog			52		µA
	Digital			2140/2280		µA
Soft standby (clock off)	Analog			12		µA
	Digital			108/116		µA

Absolute Maximum Ratings

Caution Stresses greater than those listed in Table 42 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 42: Absolute Maximum Values

Definition	Condition	Symbol	Min	Typ	Max	Unit
Core digital voltage		V_{DD_MAX}			2.4	V
I/O digital voltage		$V_{DD\_IO\_MAX}$			2.4	V
Analog voltage		V_{AA}			4	V
Pixel supply voltage		VAA_PIX			4	V
PLL supply voltage		V_{DD_PLL}			4	V
Digital operating current	Worst case current	I_{DD}			90	mA
I/O digital operating current	Worst case current	I_{DD_IO}			18	mA
Analog operating current	Worst case current	I_{AA}			145	mA
Pixel supply current	Worst case current	I_{AA_PIX}			2	mA
PLL supply current	Worst case current	I_{DD_PLL}			35	mA
Operating temperature	Measure at junction	T_{OP}	–30		70	°C
Storage temperature		T_{STG}	–40		85	°C

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Revision History

Rev. B 12/07/2007

- Update Table 1, “Key Performance Parameters,” on page 1 (input clock frequency)
- Add Figure 3: “Typical Connection: Serial CCP2 Pixel Data Interface,” on page 2
- Add Figure 4: “Typical Connection: Parallel Pixel Data Interface (CCP2),” on page 3
- Add Figure 5: “Typical Connection: Serial MIPI Pixel Data Interface,” on page 4
- Add Figure 6: “Typical Connection: Parallel Pixel Data Interface (MIPI),” on page 5
- Update Table 41, “DC Electrical Definitions and Characteristics,” on page 14 (Standby data)
- Update Figure 60: “Internal Power-On Reset,” on page 13

Rev. A 08/14/2007

- Initial release