Technical Note

MT9T013

Skipping and Binning Modes for the MT9T013

Introduction

This technical note explains the skipping and binning modes of the Micron MT9T013 CMOS digital image sensor.

Skipping

The MT9T013 supports skipping, which reduces the amount of data processed by the analog signal chain in the MT9T013, allowing the frame rate to be increased. Skipping is enabled by setting x_odd_inc and/or y_odd_inc. Values of 1, 3, and 7 can be supported. Setting both of these variables to 3 reduces the amount of row and column data processed and is equivalent to the 2x2 skipping readout mode provided by the MT9T013.

Figure 1 shows a sequence of 8 columns being read out with x_odd_inc = 3 and y_odd_inc = 1.

Figure 1:   Effect of x_odd_inc = 3 on Readout Sequence
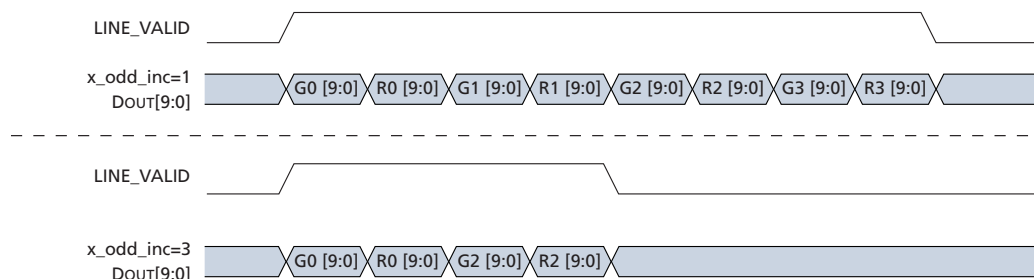
A 1/16 reduction in resolution is achieved by setting both x_odd_inc and y_odd_inc to 7. This is equivalent to 4x4 skipping readout mode provided by the MT9T013.
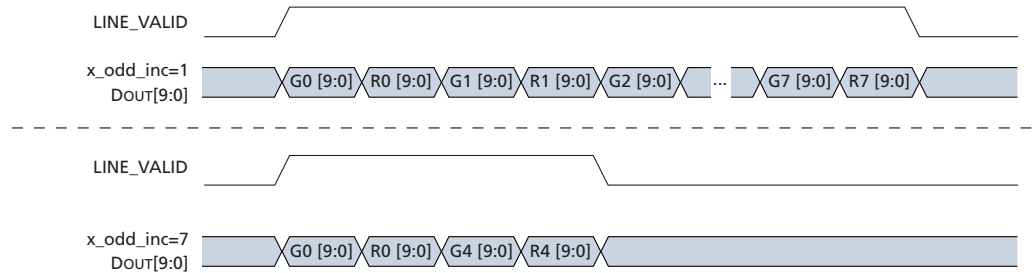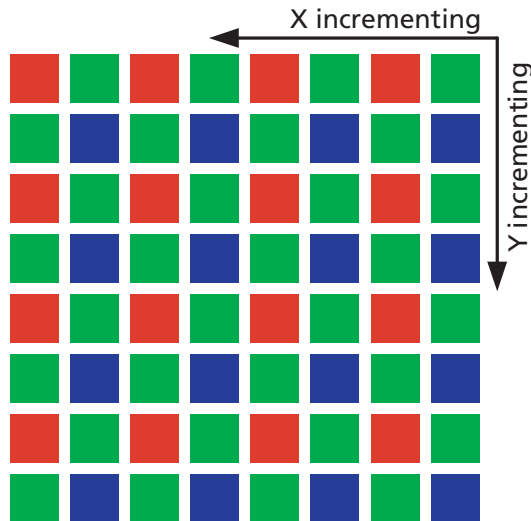
Draft 11/16/2006

Figure 2 shows a sequence of 16 columns being read out with x_odd_inc = 7 and y_odd_inc = 1.

Figure 2:   Effect of x_odd_inc = 7 on Readout Sequence

The effect of the different skipping settings on the pixel array readout is shown in Figure 3 through Figure 5 on page 3.

Figure 3:   Pixel Readout (no subsampling)

Draft 11/ 16/ 2006

Figure 4:   Pixel Readout (x_odd_inc = 3, y_odd_inc = 3)
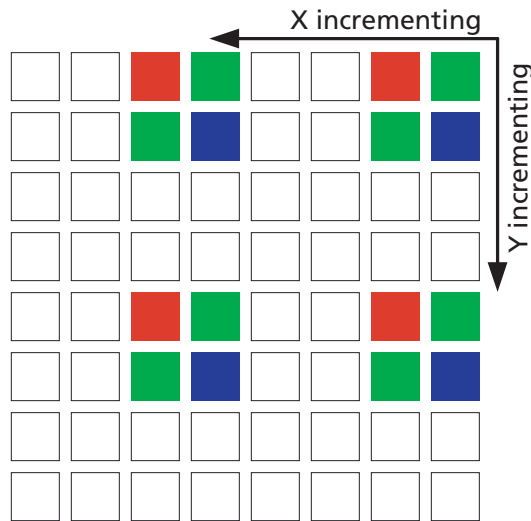
Figure 5:   Pixel Readout (x_odd_inc = 7, y_odd_inc = 7)

Draft 11/ 16/ 2006

Programming Restrictions when Skipping

When skipping is enabled in viewfinder mode and the sensor is switched back and forth between full resolution and skipping, we recommend keeping line_length_pck constant between the two modes. This allows the same integration times to be used in each mode.

When skipping is enabled it may be necessary to adjust the x_addr_end, x_addr_start, and y_addr_end, y_addr_start settings (the values for these registers are required to correspond with rows/columns that form part of the skipping sequence).

The adjustment should be made in accordance with the following rules:
- x_addr_start must be a multiple of 2
- for example, 0, 4, 6, 8, and x_addr_start=2 is not supported

When 2x2 skipping mode is enabled
- (x_addr_end - x_addr_start + x_odd_inc) should be a multiple of 4
- (y_addr_end - y_addr_start + y_odd_inc) should be a multiple of 4

When 4x4 skipping mode is enabled
- (x_addr_end - x_addr_start + x_odd_inc) should be a multiple of 8
- (y_addr_end - y_addr_start + y_odd_inc) should be a multiple of 8

The number of columns/rows read out with skipping can be found from the equation below:

When 2x2 skipping mode is enabled
- columns/rows = (addr_end - addr_start + odd_inc) / 2

When 4x4 skipping mode is enabled
- columns/rows = (addr_end - addr_start + odd_inc) / 4

Draft 11/ 16/ 2006

Sample Register Settings for Skipping

To get a 2048 x 1536 full resolution without skipping, the recommended register settings can be:

[full resolution starting address with (8,8)]

```
REG=0x0104, 1          // GROUPED_PARAMETER_HOLD
REG=0x0382, 1          // X_ODD_INC
REG=0x0386, 1          // Y_ODD_INC
REG=0x0344, 8          // X_ADDR_START
REG=0x0346, 8          // Y_ADDR_START
REG=0x0348, 2055       // X_ADDR_END
REG=0x034A, 1543       // Y_ADDR_END
REG=0x034C, 2048       // X_OUTPUT_SIZE
REG=0x034E, 1536       // Y_OUTPUT_SIZE
REG=0x0104, 0          // GROUPED_PARAMETER_HOLD
```

To achieve a 1024 x 786 resolution without 2x2 skipping, the recommended register settings can be:

[2x2 skipping starting address with (8,8)]

```
REG=0x0104, 1          // GROUPED_PARAMETER_HOLD
REG=0x0382, 3          // X_ODD_INC
REG=0x0386, 3          // Y_ODD_INC
REG=0x0344, 8          // X_ADDR_START
REG=0x0346, 8          // Y_ADDR_START
REG=0x0348, 2053       // X_ADDR_END
REG=0x034A, 1541       // Y_ADDR_END
REG=0x034C, 1024       // X_OUTPUT_SIZE
REG=0x034E, 768        // Y_OUTPUT_SIZE
REG=0x0104, 0          // GROUPED_PARAMETER_HOLD
```

To achieve a 512 x 384 resolution without 4x4 skipping, the recommended register settings can be:

[4x4 skipping starting address with (8,8)]

```
REG=0x0104, 1          // GROUPED_PARAMETER_HOLD
REG=0x0382, 7          // X_ODD_INC
REG=0x0386, 7          // Y_ODD_INC
REG=0x0344, 8          // X_ADDR_START
REG=0x0346, 8          // Y_ADDR_START
REG=0x0348, 2049       // X_ADDR_END
REG=0x034A, 1537       // Y_ADDR_END
REG=0x034C, 512        // X_OUTPUT_SIZE
REG=0x034E, 384        // Y_OUTPUT_SIZE
REG=0x0104, 0          // GROUPED_PARAMETER_HOLD
```
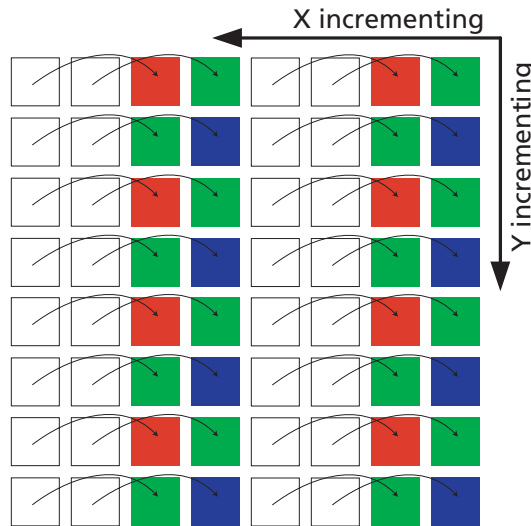
Draft 11/ 16/ 2006

Binning

The MT9T013 supports 2x1 and 2x2 analog binning (column binning, also called x-binning and row/column binning, also called xy-binning). Binning has many of the same characteristics as skipping, but because it gathers image data from all pixels in the active window rather than a subset of them, it achieves superior image quality and avoids the aliasing artifacts that can be a characteristic side effect of subsampling.

Binning is enabled by selecting the appropriate subsampling settings (x_odd_inc=3 and y_odd_inc = 1 for x-binning, x_odd_inc = 3 and y_odd_inc = 3 for xy-binning) and setting the appropriate binning bit in read_mode (R0x3040-1). As for subsampling, x_addr_end and y_addr_end may require adjustment when binning is enabled as described in "Programming Restrictions when Skipping" on page 4. Note that it is the first of the two columns/rows binned together that should be the end column/row in binning, so the requirements to the end address is exactly the same as skipping mode. The effect of the different binning settings is shown in Figure 6 and Figure 7 on page 7.

Figure 6:   Readout (x_odd_inc=3, y_odd_inc=1, x_bin=1)

Figure 7:   Readout (x_odd_inc=3, y_odd_inc=1, xy_bin=1)
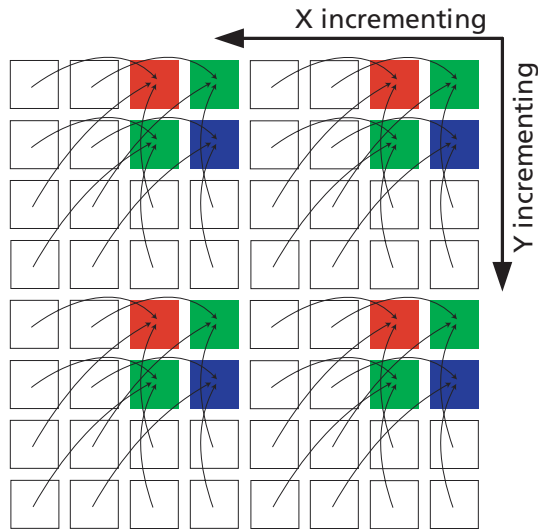
Binning can also be enabled when the 4X subsampling mode is enabled ($x\_odd\_inc = 7$ and $y\_odd\_inc = 1$ for x-binning, $x\_odd\_inc = 7$ and $y\_odd\_inc = 7$ for xy-binning). In this mode, however, not all pixels will be used so this is not a 4X binning implementation. An implementation providing a combination of skip2 and bin2 is used to achieve 4X subsampling with better image quality. The effect of this subsampling mode is shown in Figure 8 on page 7.

Figure 8:   Readout (x_odd_inc = 7, y_odd_inc = 7, xy_bin = 1)

8

Programming Restrictions when Binning

Binning requires different sequencing of the pixel array and imposes different timing limits on the operation of the sensor. In particular, xy-binning requires two read operations from the pixel array for each line of output data, which has the effect of increasing the minimum line blanking time.

As a result, when xy-binning is enabled, some of the programming limits declared in the Parameter Limit Registers are no longer valid. In addition, the default values for some of the Manufacturer Specific registers need to be reprogrammed. The recommended settings are shown in Table 1. None of these adjustments are required for binning.

Table 1:   Register Adjustments Required for Binning Mode

Register	Type	Default (normal readout)	Recommended Setting During Binning	Notes
min_line_blanking_pck	Read only	0x037a	0x0634	Read only register for control software; does not affect operation of sensor.
min_line_length_pck	Read only	0x0488	0x0900	Read only register for control software; does not affect operation of sensor.
fine_integration_time_min	Read only	0x02b5	0x058d	Read only register for control software; does not affect operation of sensor.
fine_integration_time_max_margin	Read only	0x01d3	0x0373	Read only register for control software; does not affect operation of sensor.
fine_correction	Read/write	0x0100	0x0238	Affects operation of sensor.
fine_integration_time	Read/write	0x02b5	0x058d	Normal default is minimum value.

Draft 11/ 16/ 2006

Sample Register Settings for Binning

To achieve a 1024 x 1536 resolution with x-binning, the recommended register settings can be:

```
[x-binning]
REG=0x0104, 1                    // GROUPED_PARAMETER_HOLD
REG=0x1148, 0x0634               // MIN_LINE_BLANKING_PCK
REG=0x1144, 0x0900               // MIN_LINE_LENGTH_PCK
REG=0x1008, 0x058D               // FINE_INTEGRATION_TIME_MIN
REG=0x100A, 0x0373               // FINE_INTEGRATION_TIME_MAX_MARGIN
REG=0x3010, 0x0238               // FINE_CORRECTION
REG=0x3014, 0x058D               // FINE_INTEGRATION_TIME_
REG=0x0344, 8                    // X_ADDR_START
REG=0x0346, 8                    // Y_ADDR_START
REG=0x0348, 2053                 // X_ADDR_END
REG=0x034A, 1543                 // Y_ADDR_END
REG=0x0382, 3                    // X_ODD_INC
REG=0x0386, 1                    // Y_ODD_INC

BITFIELD=0x3040, 0x0C00, 2       // Enable X binning
REG=0x034C, 1024                 // X_OUTPUT_SIZE
REG=0x034E, 1536                 // Y_OUTPUT_SIZE
REG=0x0104, 0                    // GROUPED_PARAMETER_HOLD
```

To achieve a 1024 x 768 resolution with xy-binning, the recommended register settings can be:

```
[xy-binning]
REG=0x0104, 1                    // GROUPED_PARAMETER_HOLD
REG=0x1148, 0x0634               // MIN_LINE_BLANKING_PCK
REG=0x1144, 0x0900               // MIN_LINE_LENGTH_PCK
REG=0x1008, 0x058D               // FINE_INTEGRATION_TIME_MIN
REG=0x100A, 0x0373               // FINE_INTEGRATION_TIME_MAX_MARGIN
REG=0x3010, 0x0238               // FINE_CORRECTION
REG=0x3014, 0x058D               // FINE_INTEGRATION_TIME_
REG=0x0344, 8                    // X_ADDR_START
REG=0x0346, 8                    // Y_ADDR_START
REG=0x0348, 2053                 // X_ADDR_END
REG=0x034A, 1541                 // Y_ADDR_END
REG=0x0382, 3                    // X_ODD_INC
REG=0x0386, 3                    // Y_ODD_INC

BITFIELD=0x3040, 0x0C00, 1       // Enable XY binning
REG=0x034C, 1024                 // X_OUTPUT_SIZE
REG=0x034E, 768                  // Y_OUTPUT_SIZE
REG=0x0104, 0                    // GROUPED_PARAMETER_HOLD
```

Draft 11/ 16/ 2006

Conclusion

This technical note highlights the skipping and binning features of the MT9T013. For more information on this and other features, refer to the MT9T013 1/4-inch 3.1Mp CMOS digital image sensor data sheet on Micron's Web site at www.micron.com/ imaging.

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Revision History

Rev. A 11//06
  • Initial release

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