1/4-Inch 3.1Mp CMOS Active-Pixel Digital Image Sensor Die with MIPI and Parallel Output Interface

MT9T013 Die Data Sheet

For the product data sheet, refer to Aptina's Web site: www.aptina.com

Features

- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Support for external mechanical shutter
- Support for external LED or xenon flash
- High frame-rate preview mode with arbitrary down-size scaling from maximum resolution
- Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning
- Data interfaces: parallel and MIPI interface
- On-die PLL
- Bayer-pattern down-size scaler
- One-time programmable (OTP) memory for storing module information
- Integrated lens shading correction

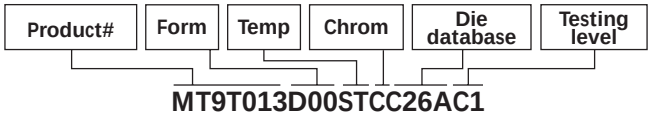
General Physical Specifications

- Die thickness: 200µm ±12µm
  (Consult factory for other die thickness)
- Back side wafer surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.2kÅ
- Typical metal 3 thickness: 3.2kÅ
- Typical metal 4 thickness: 4.0kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
  2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

MT9T013D00STCM C26AC1 - Z18 (25°) – MIPI

MT9T013D00STCZM C26AC1 - Z19 (23°) – MIPI



Die Database

- Die outline, see Figure 3 on page 10
- Singulated die size: 5,688 ±25 x 5,336 ±25µm
- Bond Pad Location and Identification Tables, see pages 6–8.

Option

- Form
  Die D
- Testing
  Standard (Level 1) probe C1

Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

General Description

The Aptina™ MT9T013 die is a QXGA-format 1/4-inch CMOS active-pixel digital image sensor, with a pixel array of 2064H x 1552V (2048H x 1536V with an 8-pixel border on each edge). It incorporates sophisticated on-die camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9T013 digital image sensor die features Aptina's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

When operated in its default mode, the sensor generates a QXGA image at 15 frames per second (fps). An on-die analog-to-digital converter (ADC) generates a 10-bit value for each pixel. The pixel data is either encoded with line and framing information in a MIPI serial data interface or is output on a 10-bit output bus and qualified by an output data clock (PIXCLK), together with LINE_VALID and FRAME_VALID signals. A flash output strobe is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time. Additional I/O signals support the provision of an external mechanical shutter. The sensor can be programmed by the user to control the frame size, exposure, gain setting, and other parameters.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in Aptina's standard package. Since the package environment is not within Aptina's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided here are for reference only. For target functional and parametric specifications, refer to the packaged product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9T013 imager die has 65 bond pads. Refer to Table 1 and Table 2 on pages 6–8 for a complete list of bond pads and coordinates.

The MT9T013 imager die does not require the user to determine bond option features.

The die also has several pads defined as “do not use.” These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows the MT9T013 typical die connections. For low-noise operation the MT9T013 die requires separate supplies for analog and digital power. Power supply rails should be decoupled from ground using capacitors. Use of inductance filters is not recommended.

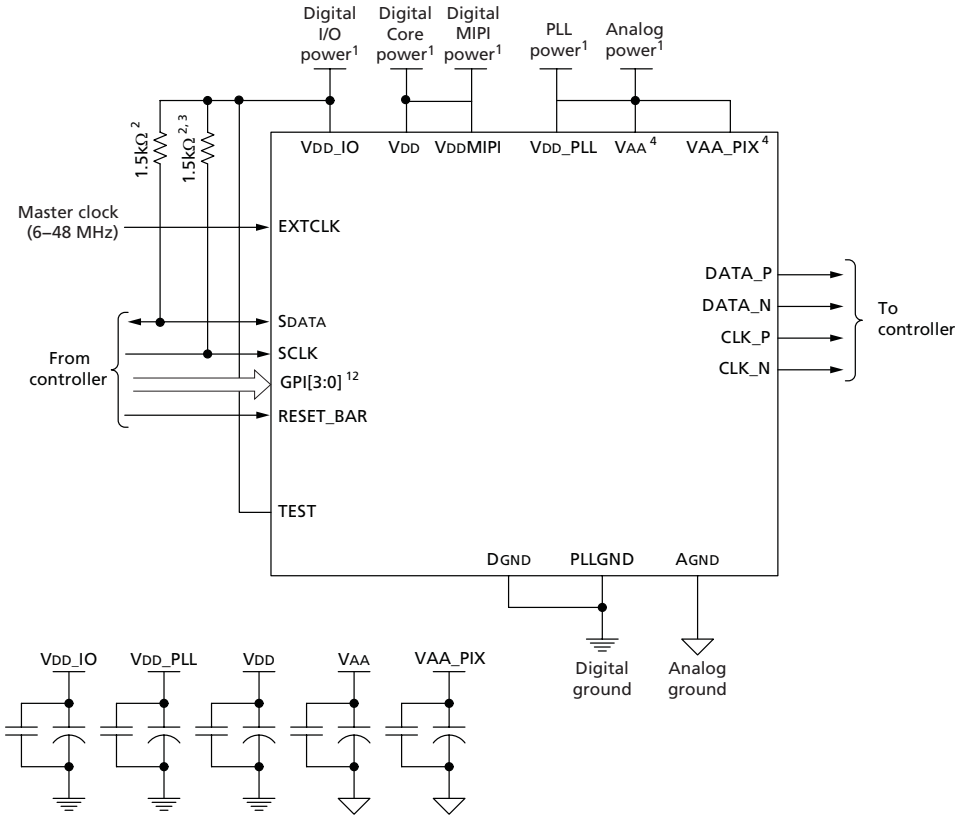
Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Aptina recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Output Modes

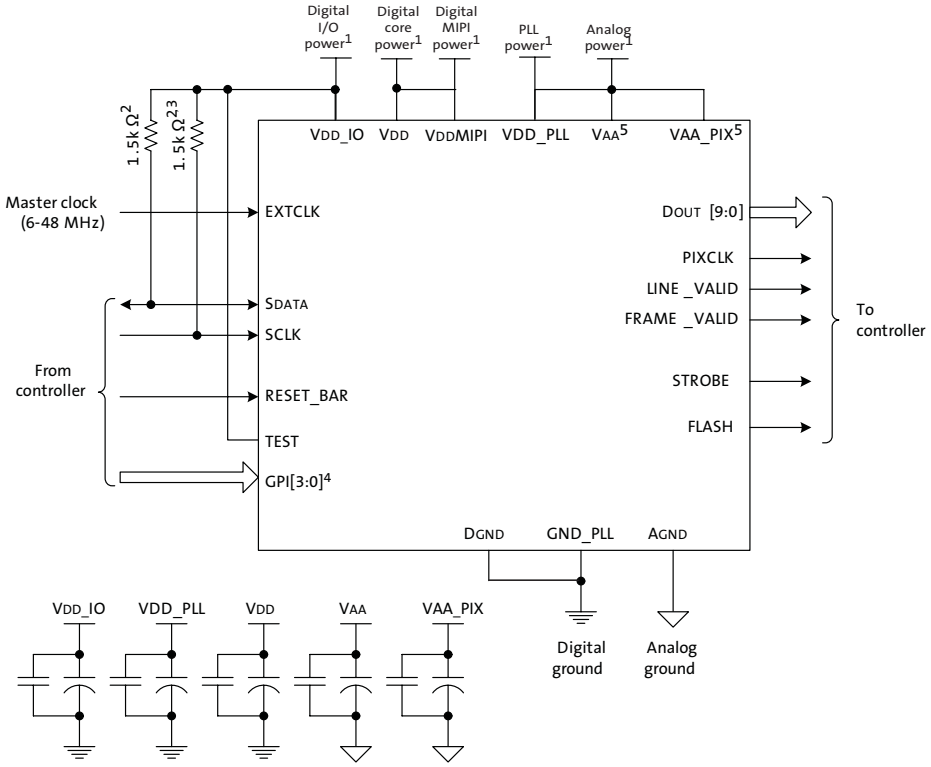
Figure 1 below and Figure 2 on page 5 show typical configuration schematics for the MT9T013 operating in serial and parallel modes.

Figure 1: Typical Configuration (Connection)–Serial Output Mode



Notes:
1. All power supplies should be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but this may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. VAA and VAA_PIX must be tied together.
5. VPP, which can be used during the module manufacturing process, is not shown in Figure 1. This pad is left unconnected during normal operation.
6. The parallel interface output pads can be left unconnected if the serial output interface is used.
7. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design consideration.
8. VDD_IO2, and VDD_IO3 can be left unconnected for a serial pixel data interface.
9. TEST must be tied to VDD_IO.
10. Aptina recommends that PLLGND be tied to DGND.
11. Aptina recommends that VDDMIPI be tied to VDD.
12. The GPI pins can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_N, SADDR, STANDBY) to be dynamically controlled.

Figure 2: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The GPI pins can be statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_N, SADDR, STANDBY) to be dynamically controlled.
5. VAA and VAA_PIX must be tied together.
6. VPP, which can be used during the module manufacturing process, is not shown in Figure 3. This pad is left unconnected during normal operation.
7. The serial interface output pads can be left unconnected if the parallel output interface is used.
8. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.
9. TEST must be tied to VDD_IO.
10. Aptina recommends that GND_PLL be tied to DGND.
11. Aptina recommends that VDDMIPI be tied to VDD.

Bond Pad Location and Identification Tables

Table 1: Bond Pad Location From Center of Pad 1

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_IO4	0.00	0.00	0.0000000	0.0000000
2	VDD3	170.53	0.00	0.0067138	0.0000000
3	DGND4	341.05	0.00	0.0134272	0.0000000
4	DATA_N	608.47	0.00	0.0239553	0.0000000
5	DATA_P	838.47	0.00	0.0330104	0.0000000
6	CLK_N	1068.47	0.00	0.0420657	0.0000000
7	CLK_P	1298.47	0.00	0.0511209	0.0000000
8	VDD_TX	1526.57	0.00	0.0601012	0.0000000
9	VDD_PLL	3087.93	0.00	0.1215720	0.0000000
10	GND_PLL	3258.46	0.00	0.1282858	0.0000000
11	RESET_BAR	3428.97	0.00	0.1349988	0.0000000
12	EXTCLK	3599.49	0.00	0.1417122	0.0000000
13	VDD4	3770.01	0.00	0.1484256	0.0000000
14	VDD_IO5	4083.21	0.00	0.1607563	0.0000000
15	DOUT0	4253.73	0.00	0.1674697	0.0000000
16	DGND5	4424.25	0.00	0.1741831	0.0000000
17	DOUT9	4594.77	0.00	0.1808965	0.0000000
18	DOUT1	4801.25	0.00	0.1890256	0.0000000
19	VDD_IO6	4986.28	0.00	0.1963102	0.0000000
20	DGND6	5217.11	–267.38	0.2053980	–0.0105268
21	TEST[2]	5217.11	–397.30	0.2053980	–0.0156417
22	SCLK	5217.11	–546.94	0.2053980	–0.0215331
23	SDATA	5217.11	–717.46	0.2053980	–0.0282465
24	GPIO_3	5217.11	–887.98	0.2053980	–0.0349598
25	GPIO_2	5217.11	–1058.50	0.2053980	–0.0416732
26	GPIO_1	5217.11	–1229.02	0.2053980	–0.0483866
27	GPIO_0	5217.11	–1399.54	0.2053980	–0.0551000
28	VAA4	5217.11	–1570.06	0.2053980	–0.0618134
29	VAA3	5217.11	–1740.58	0.2053980	–0.0685268
30	AGND7	5217.11	–1911.10	0.2053980	–0.0752402
31	AGND6	5217.11	–2081.62	0.2053980	–0.0819535
32	DNU[3]	5217.11	–2580.42	0.2053980	–0.1015913
33	DNU	5217.11	–2690.62	0.2053980	–0.1059299
34	DNU	5217.11	–2800.82	0.2053980	–0.1102685
35	VAA_PIX3	5217.11	–2911.02	0.2053980	–0.1146071
36	VAA_PIX2	5217.11	–3081.54	0.2053980	–0.1213205
37	VAA_PIX1	5217.11	–3252.06	0.2053980	–0.1280339
38	VPP	5217.11	–3520.60	0.2053980	–0.1386063
39	AGND5	5217.11	–3789.14	0.2053980	–0.1491787
40	AGND4	5217.11	–3959.66	0.2053980	–0.1558921
41	AGND3	5217.11	–4130.18	0.2053980	–0.1626055
42	AGND2	5217.11	–4350.58	0.2053980	–0.1712827
43	AGND1	5217.11	–4521.10	0.2053980	–0.1779961

Table 1: Bond Pad Location From Center of Pad 1 (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	VAA2	5217.11	–4691.62	0.2053980	–0.1847094
45	VAA1	5217.11	–4862.14	0.2053980	–0.1914228
46	VDD_IO1	171.69	–5096.46	0.0067594	–0.2006480
47	VDD1	1.17	–5096.46	0.0000461	–0.2006480
48	DGND1	–169.35	–5096.46	–0.0066673	–0.2006480
49	FLASH	–230.83	–3367.48	–0.0090878	–0.1325780
50	SHUTTER	–230.83	–3161.00	–0.0090878	–0.1244488
51	FRAME_VALID	–230.83	–2954.52	–0.0090878	–0.1163197
52	PIXCLK	–230.83	–2748.04	–0.0090878	–0.1081906
53	VDD2	–230.83	–2577.52	–0.0090878	–0.1014772
54	VDD_IO2	–230.83	–2407.00	–0.0090878	–0.0947638
55	DGND2	–230.83	–2236.48	–0.0090878	–0.0880504
56	DOUT2	–230.83	–2065.96	–0.0090878	–0.0813370
57	LINE_VALID	–230.83	–1859.48	–0.0090878	–0.0732079
58	DOUT7	–230.83	–1653.00	–0.0090878	–0.0650787
59	DOUT6	–230.83	–1446.52	–0.0090878	–0.0569496
60	VDD_IO3	–230.83	–1276.00	–0.0090878	–0.0502362
61	DGND3	–230.83	–1105.48	–0.0090878	–0.0435228
62	DOUT4	–230.83	–934.96	–0.0090878	–0.0368094
63	DOUT8	–230.83	–728.48	–0.0090878	–0.0286803
64	DOUT5	–230.83	–522.00	–0.0090878	–0.0205512
65	DOUT3	–230.83	–315.52	–0.0090878	–0.0124220

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. TEST must be connected to VDD_IO for proper device functionality.
3. DNU = do not use.
4. To ensure proper device operation, all power supply bond pads must be bonded.

Table 2: Bond Pad Location From Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	VDD_IO4	–2493.14	2548.23	–0.0981551	0.1003240
2	VDD3	–2322.61	2548.23	–0.0914413	0.1003240
3	DGND4	–2152.09	2548.23	–0.0847280	0.1003240
4	DATA_N	–1884.68	2548.23	–0.0741998	0.1003240
5	DATA_P	–1654.68	2548.23	–0.0651447	0.1003240
6	CLK_N	–1424.67	2548.23	–0.0560894	0.1003240
7	CLK_P	–1194.67	2548.23	–0.0470343	0.1003240
8	VDD_TX	–966.57	2548.23	–0.0380539	0.1003240
9	VDD_PLL	594.79	2548.23	0.0234169	0.1003240
10	GND_PLL	765.32	2548.23	0.0301307	0.1003240
11	RESET_BAR	935.83	2548.23	0.0368437	0.1003240
12	EXTCLK	1106.35	2548.23	0.0435571	0.1003240
13	VDD4	1276.87	2548.23	0.0502705	0.1003240
14	VDD_IO5	1590.07	2548.23	0.0626012	0.1003240
15	DOUT0	1760.59	2548.23	0.0693146	0.1003240
16	DGND5	1931.11	2548.23	0.0760280	0.1003240
17	DOUT9	2101.63	2548.23	0.0827413	0.1003240
18	DOUT1	2308.11	2548.23	0.0908705	0.1003240
19	VDD_IO6	2493.14	2548.23	0.0981551	0.1003240
20	DGND6	2723.97	2280.85	0.1072429	0.0897972
21	TEST[2]	2723.97	2150.93	0.1072429	0.0846823
22	SCLK	2723.97	2001.29	0.1072429	0.0787909
23	SDATA	2723.97	1830.77	0.1072429	0.0720776
24	GPIO_3	2723.97	1660.25	0.1072429	0.0653642
25	GPIO_2	2723.97	1489.73	0.1072429	0.0586508
26	GPIO_1	2723.97	1319.21	0.1072429	0.0519374
27	GPIO_0	2723.97	1148.69	0.1072429	0.0452240
28	VAA4	2723.97	978.17	0.1072429	0.0385106
29	VAA3	2723.97	807.65	0.1072429	0.0317972
30	AGND7	2723.97	637.13	0.1072429	0.0250839
31	AGND6	2723.97	466.61	0.1072429	0.0183705
32	DNU[3]	2723.97	–32.19	0.1072429	–0.0012673
33	DNU	2723.97	–142.39	0.1072429	–0.0056059
34	DNU	2723.97	–252.59	0.1072429	–0.0099445
35	VAA_PIX3	2723.97	–362.79	0.1072429	–0.0142831
36	VAA_PIX2	2723.97	–533.31	0.1072429	–0.0209965
37	VAA_PIX1	2723.97	–703.83	0.1072429	–0.0277098
38	VPP	2723.97	–972.37	0.1072429	–0.0382823
39	AGND5	2723.97	–1240.91	0.1072429	–0.0488547
40	AGND4	2723.97	–1411.43	0.1072429	–0.0555681
41	AGND3	2723.97	–1581.95	0.1072429	–0.0622815
42	AGND2	2723.97	–1802.35	0.1072429	–0.0709587
43	AGND1	2723.97	–1972.87	0.1072429	–0.0776720
44	VAA2	2723.97	–2143.39	0.1072429	–0.0843854
45	VAA1	2723.97	–2313.91	0.1072429	–0.0910988

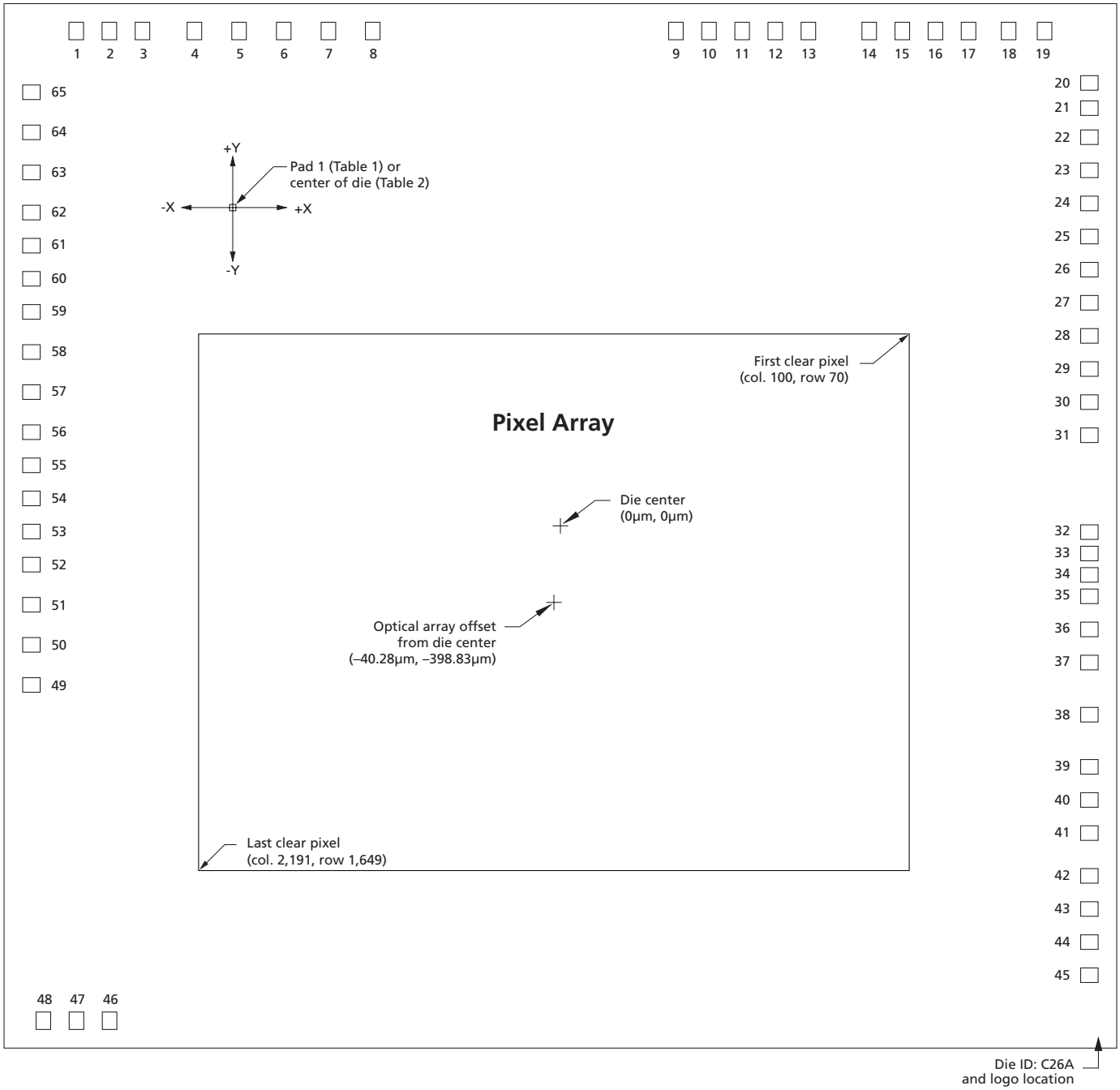
Table 2: Bond Pad Location From Center of Die (0, 0) (continued)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
46	VDD_IO1	–2321.45	–2548.23	–0.0913957	–0.1003240
47	VDD1	–2491.97	–2548.23	–0.0981091	–0.1003240
48	DGND1	–2662.49	–2548.23	–0.1048224	–0.1003240
49	FLASH	–2723.97	–819.25	–0.1072429	–0.0322539
50	SHUTTER	–2723.97	–612.77	–0.1072429	–0.0241248
51	FRAME_VALID	–2723.97	–406.29	–0.1072429	–0.0159957
52	PIXCLK	–2723.97	–199.81	–0.1072429	–0.0078665
53	VDD2	–2723.97	–29.29	–0.1072429	–0.0011531
54	VDD_IO2	–2723.97	141.23	–0.1072429	0.0055602
55	DGND2	–2723.97	311.75	–0.1072429	0.0122736
56	DOUT2	–2723.97	482.27	–0.1072429	0.0189870
57	LINE_VALID	–2723.97	688.75	–0.1072429	0.0271161
58	DOUT7	–2723.97	895.23	–0.1072429	0.0352453
59	DOUT6	–2723.97	1101.71	–0.1072429	0.0433744
60	VDD_IO3	–2723.97	1272.23	–0.1072429	0.0500878
61	DGND3	–2723.97	1442.75	–0.1072429	0.0568012
62	DOUT4	–2723.97	1613.27	–0.1072429	0.0635146
63	DOUT8	–2723.97	1819.75	–0.1072429	0.0716437
64	DOUT5	–2723.97	2026.23	–0.1072429	0.0797728
65	DOUT3	–2723.97	2232.71	–0.1072429	0.0879020

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. TEST must be connected to VDD_IOfor proper device functionality.
3. DNU = do not use.
4. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 3: Die Outline (Top View)

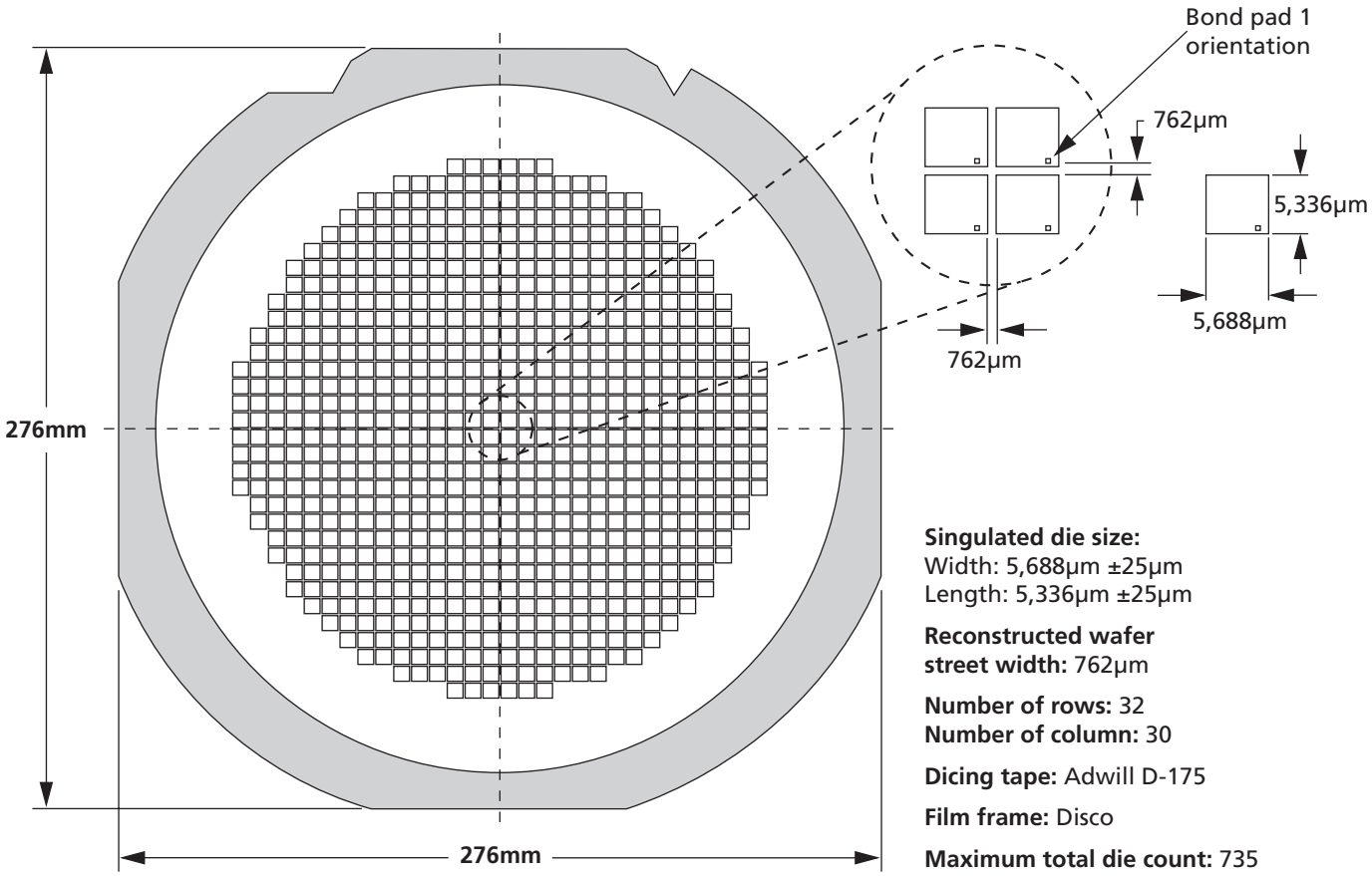


Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Singulated die size Width (X dimension): Length (Y dimension):	 5,688µm ±25µm 5,336µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch between any two bond pads:	 110.2µm (4.339 mil)
Optical array offset Optical center from die center: Optical center from center of pad 1:	 X = –40.28µm, Y = –398.83µm X = 2,452.86µm, Y = –2,947.06µm
First clear pixel (col. 100, row 70) From die center: From center of pad 1:	 X = 1,817.645µm, Y = 1009.68µm X = 4,310.785µm, Y = –1,538.55µm
Last clear pixel (col. 2,191, row 1,649) From die center: From center of pad 1:	 X = –1,897.515µm, Y = –1,807.8µm X = 595.625µm, Y = –4,356.03µm

Figure 4: MT9T013 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 5,688µm ±25µm
Length: 5,336µm ±25µm

Reconstructed wafer street width: 762µm

Number of rows: 32
Number of column: 30

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 735

Revision History

Rev. G 3/16/12

- Updated trademarks

Rev. F, Production 2/19/09

- Re-added Figure 2 on page 5 that was in Rev. D but got hidden in Rev. E
- Updated last page with new corporate address

Rev. E, Production. 9/12/08

- Updated to Aptina template
- Updated title on p. 1
- Updated “Order Information” on page 1
- Modified Note 8 in Figure 1 on page 4
- Modified Note 9 in Figure 2 on page 5 and updated figure to reflect change in the note.

Rev. D, Production 1/08

- Updated template
- Updated Figure 1: “Typical Configuration (Connection)–Serial Output Mode,” on page 4
- Updated Table 3, “Physical Dimensions,” on page 11
- Updated Figure 2: “Typical Configuration: Parallel Pixel Data Interface,” on page 5
- Updated Table 2, “Bond Pad Location From Center of Die (0, 0),” on page 8

Rev. C, Production 10/07

- Updated typical metal 2, 3 thickness “General Physical Specifications” on page 1
- Added typical metal 4 thickness “General Physical Specifications” on page 1
- Added GPI[3:0] to Figure 1 on page 4
- Updated DDS to Production
- Updated Figure 1 on page 4 and Figure 2 on page 5: added XSHUTDOWN

Rev. B, Preliminary 5/07

- Updated Figure 1: “Typical Configuration (Connection)–Serial Output Mode,” on page 4
- Updated Figure 2: “Typical Configuration: Parallel Pixel Data Interface,” on page 5

Rev. A, Preliminary 5/07

- Initial release

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