1/3-Inch Wide-VGA CMOS Digital Image Sensor

MT9V022

Silicon Revision 3 Errata

Introduction

This errata contains deviations from the latest MT9V022 image sensor data sheet. Deviations are either temporary or permanent, as denoted in the tables below.

This information is provided for customer information at this time, and customers are not required to respond to this document. Any permanent changes will be incorporated into the next revision of the data sheet.

Table 1: Known Issues

Issue #	Issue	Notes
1	Row Banding (darkening) occurs in all the pixels of rows that have some pixels receiving very bright illumination.	This issue has been resolved by Rev3.
2	Snapshot mode idle charge accumulation results in a corrupted first frame.	Global reset timing improvement results in proper charge reset before Snapshot mode first frame integration begins.
3	Extra STLN_OUT pulses are transmitted by a master mode sensor at the end of a frame – potentially corrupting sequencing with a capture device or with a stereoscopic slave MT9V022.	This issue has been resolved by Rev3. Rev3 devices have a one line latency between master and slave integration time and readout timing.
4	Some Slave Mode timing conditions cause a missing internal photodiode charge transfer pulse, resulting in a black image.	This issue has been resolved by Rev3. An internal photodiode charge transfer pulse is always generated.
5	Non-ideal anti-eclipse bias default, results in increased column FPN when anti-eclipse is enabled.	Improved anti-eclipse bias default. Column FPN is reduced when anti-eclipse is enabled.
6	Charge transfer timing conflicts cause horizontal shutter line artifacts in the output image when ideal (lowest FPN) timing is used.	Timing conflicts resolved. Improved Charge transfer timing can be used to reduce pixel FPN without shutter line artifacts.
7	Negative Lag pixel response occurs in frames following very bright illumination.	Negative Lag reduced to <0.5%.
8	Limited Timing control prevents the lowest FPN HiDy mode timing. (R0x20:[2] = 1 can not be used.)	Improved timing flexibility allows lowest FPN HiDy mode timing (R0x20:[2] = 1 can be used.)
9	Timing bug effects charge transfer at minimum exposure (R0x0B = 1.) The minimum usable exposure setting is R0x0B = 2.	This issue has been resolved by Rev3. The minimum usable exposure setting is R0x0B = 1.

Recommended Register Settings

Register setting recommendations are based on Aptina's characterization of the image sensor only. Camera module makers should test these recommendations on their module and evaluate the overall performance.

The following table (Table 2) lists the default register changes from the MT9V022 Rev2 to Rev3. It also lists recommended settings for these registers in both linear and HiDy mode for MT9V022 Rev3 devices.

Table 2: Changes from Rev2

Item #	Default Register Changes				Linear Mode	HiDy Mode	Design Change Description
	Register Number	Register Name	Rev2 Default	Rev3 Default			
1	R0x00 and R0xFF	Device ID	0x1311	0x1313	0x1313	0x1313	ID updated.
2	R0x10	Reserved	0x002D	0x0040	0x0040	0x0040	Lowers Column FPN.
3	R0x13	Reserved	0x0E32	0x2D32	0x2D32	0x2D32	Improves Negative Lag.
4	R0x15	Reserved	0x0E32	0x7F32	0x7F32	0x7F32	Lowers pixel-wise FPN and eliminates shutter line artifacts.
5	R0x20	Reserved	0x0015	0x01D1	0x01D1[2]	0x01D5[1,2]	Lower pixel-wise FPN.
6	R0xC2	Analog Controls	0x1840	0x0840	0x0840	0x0940[1]	Improved anti-eclipse reference voltage default results in reduced column FPN.

Notes:
1. These two changes to registers R0x20 and R0xC2 can be used together in HiDy mode to reduce pixel FPN and increase dynamic range.
2. For Snapshot mode, Register 0x20, bit 9, is set to 1. The Linear mode setting becomes 0x03D1. The HiDy mode setting becomes 0x03D5.

Revision History

Rev. D 8/30/10

- Updated to non-confidential

Rev. C 6/2/10

- Updated to Aptina template

Rev. B 8/30/05

- Updates to Table 2, item 5, Linear Mode and HiDy Mode

Rev. A 8/18/05

- Initial release

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