



# 1/3-Inch Wide-VGA CMOS Digital Image Sensor

## MT9V022 Timing Specifications Addendum

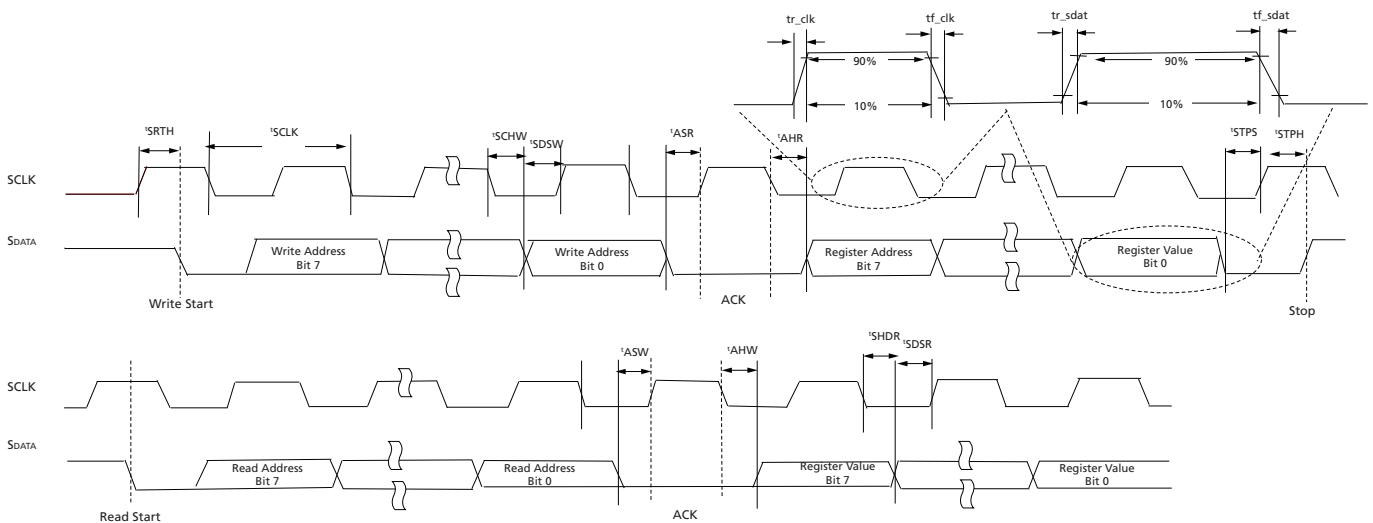
For more information, refer to the data sheet on Micron's Web site: [www.micron.com/imaging](http://www.micron.com/imaging)

### Introduction

This document supplements Micron's MT9V022 data sheet (Revision F 12/2006) with additional AC timing parameters. The standard data sheet should be referenced for a complete description of sensor parameters. The specifications contained in this addendum supersede the specifications listed in the data sheet.

### Two-Wire Serial Bus Timing

This section adds detailed minimum and maximum limits as well as rise- and fall-time parameters information. Waveforms and parameter table follow.



**Table 1: Two-Wire Serial Bus Timing Parameters**

Test Conditions: 25°C, 26.67 MHz, and 3.3V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{SCLK}$	Serial interface input clock frequency				400	kHz
$t_{SCLK}$	Serial Input clock period				2.5	$\mu$ sec
	SCLK duty cycle		40	50	60	%
$t_{r\_sclk}$	SCLK rise time			165		ns
$t_{f\_sclk}$	SCLK fall time			6		ns
$t_{r\_sdat}$	SDATA rise time			180		ns
$t_{f\_sdat}$	SDATA fall time			9		ns



## MT9V022: Timing Specifications Addendum Two-Wire Serial Bus Timing

**Table 1: Two-Wire Serial Bus Timing Parameters (continued)**

Test Conditions: 25°C, 26.67 MHz, and 3.3V

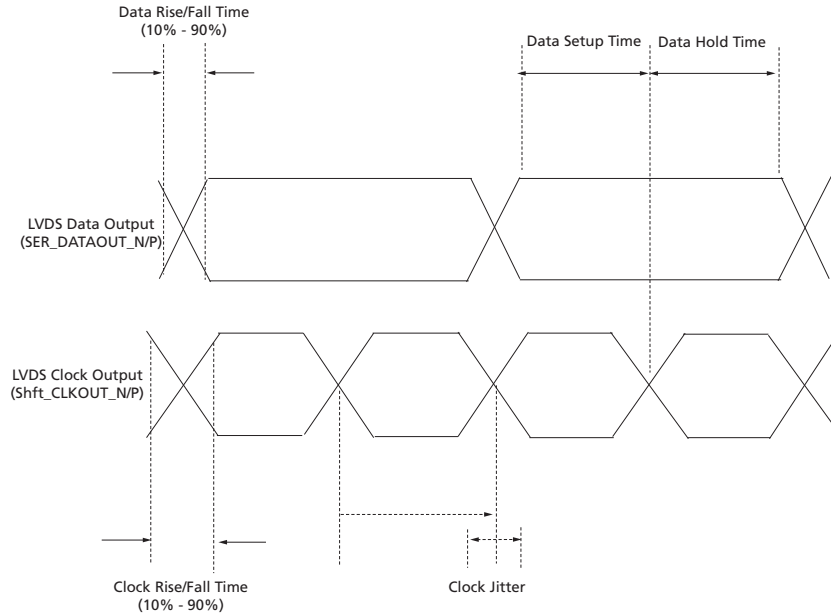
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SRTS}$	Start setup time	WRITE/READ	148	150	167	ns
$t_{SRTH}$	Start hold time	WRITE/READ	36.9	36	37.6	ns
$t_{SDSW}$	SDATA setup	WRITE	0	5	12	ns
$t_{SDHW}$	SDATA hold	WRITE	1.3	36	37	ns
$t_{ASW}$	ACK setup time	WRITE	146	146	148	ns
$t_{AHW}$	ACK hold time	WRITE	98.9	107	144	ns
$t_{STPS}$	Stop setup time	WRITE/READ		624		ns
$t_{STPH}$	Stop hold time	WRITE/READ		1.61		ns
$t_{ASR}$	ACK setup time	READ	192	228	229	ns
$t_{AHR}$	ACK hold time	READ	247	284	287	ns
$t_{SDSR}$	SDATA setup	READ	654	655	690	ns
$t_{SDHR}$	SDATA hold	READ	560	595	596	ns
CIN_SI	Serial interface input pin capacitance			2.57		pF
CLOAD_SD	SDATA max load capacitance				400	pF
RSD	SDATA external pull-up resistor			1.0		k $\Omega$



## LVDS Data Bus Timing

This section adds rise- and fall-time parameters to the LVDS timing section. Waveforms and parameter table follow.

**Figure 1: LVDS Timing**



**Table 2: LVDS AC Timing Specifications**

VPWR = 3.3V ±0.3V; T<sub>J</sub> = - 40°C to +105°C; output load = 100 Ω; frequency 27 MHz

Parameter	Typical	Maximum	Unit
LVDS clock rise time	0.22	0.28	ns
LVDS clock fall time	0.23	0.29	ns
LVDS data rise time	0.28	0.30	ns
LVDS data fall time	0.28	0.30	ns
LVDS data setup time	0.67	1.5	ns
LVDS data hold time	1.34	1.5	ns
LVDS clock jitter		92	ps



## Electrical Specifications

This section provides updated values to Table 12, “DC Electrical Characteristics”, with new values measured across the temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

This section also provides updates to Table 14, “AC Electrical Characteristics”, with new values measured across temperature, as well as additional parameters for rise and fall times relative to PIXCLK.

The updated parameters are in Table 3.

**Table 3: DC Electrical Characteristics Over Temperature**

$V_{PWR} = 3.3\text{V} \pm 0.3\text{V}$ ;  $T_J = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ; output load = 10pF; frequency 13 MHz to 27 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IH}$	Input High Voltage		$V_{PWR} - 1.2$	1.6	1.27	V
$V_{IL}$	Input low voltage		–	1.7		V
$I_{IN}$	Input leakage current	No pull-up resistor; $V_{IN} = V_{PWR}$ or $V_{GND}$	–	0.01	0.6	$\mu\text{A}$
$V_{OH}$	Output high voltage	$I_{OH} = -4.0\text{mA}$	$V_{PWR} - 0.3$	3	–	V
$V_{OL}$	Output low voltage	$I_{OL} = 4.0\text{mA}$		0.22	0.3	V
$I_{OH}$	Output high current	$V_{OH} = V_{DD} - 0.7$	–25.8	–13	–	mA
$I_{OL}$	Output low current	$V_{OL} = 0.7$	–	13	24.5	mA
$I_{PWRA}$	Analog supply current	Default Settings	–	40	60	mA
$I_{PIX}$	Pixel Array Current	Default Settings	–	1.1	1.7	mA
$I_{PWRD}$	Digital Supply Current	Default Settings, Clload = 10 pF	–	35	70	mA
$I_{LVDS}$	LVDS supply current	Default Settings	–	5.0	10.0	mA
$I_{PWRA}$ Standby	Analog standby supply current	STANDBY = $V_{DD}$	–	0.17	6	$\mu\text{A}$
$I_{PIX}$ Standby	Pixel array standby current	STANDBY = $V_{DD}$	–	0.13	0.42	$\mu\text{A}$
$I_{PWRD}$ Standby Clock Off	Digital standby supply current with clock off	STANDBY = $V_{DD}$ , CLKIN = 0 MHz	–	0.1	5	$\mu\text{A}$
$I_{PWRD}$ Standby Clock On	Digital standby supply current with clock on	STANDBY = $V_{DD}$ , CLKIN = 27 MHz	–	1	5	mA
<b>LVDS Driver DC Specifications</b>						
$I_{OZ}$	Output Current when driver is tri-state	Output current when driver is tri-state		0.1	0.2	$\mu\text{A}$



## MT9V022: Timing Specifications Addendum Electrical Specifications

**Table 4: AC Electrical Characteristics Over Temperature Range**

$V_{PWR} = 3.3V \pm 0.3V$ ;  $T_J = -40^{\circ}C$  to  $+105^{\circ}C$ ; output load = 10pF; frequency 13 MHz to 27 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{PLHP}$	SYSCLK to PIXCLK propagation delay	CLOAD = 10pF	4	6	9	ns
$t_{PD}$	PIXCLK to valid DOUT(9:0) propagation delay	CLOAD = 10pF	-1	0.02	2	ns
$t_{PFLR}$	PIXCLK to LINE_VALID propagation delay	CLOAD = 10pF	5	8	10	ns
$t_{PFLF}$	PIXCLK to FRAME_VALID propagation delay	CLOAD = 10pF	5	8	10	ns



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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



## Revision History

Rev. A .....	12/07/2007
<ul style="list-style-type: none"><li>• Initial release</li></ul>	