



## MT9V034 Register Reference

For more information, refer to the data sheet on Aptina's Web site: [www.aplina.com](http://www.aplina.com)

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# MT9V034 Register Reference



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## Introduction

This reference document describes the MT9V034 registers and variables. Summary and detailed information are presented in separate sections:

- Table 1, “Register List,” on page 5
- Table 2, “Register Descriptions,” on page 9

**Note:** Throughout this document, Green1 to corresponds to greenB; green2 corresponds to greenB.

## How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the MT9V034 data sheet.

## Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

## Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when `line_length_pck` (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when `mask_corrupted_frames` (R0x0105) is set to “1.”



## Registers

**Caution** Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.

**Table 1: Register List**  
1 = always 1; 0 = always 0; d = programmable; ? = read only

Register Number (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x00	Chip Version	0001 0011 0010 0100 (LSB)	Iter. 1: 0x1324
0x01	Column Start	0000 00dd dddd dddd	0x0001
0x02	Row Start Context A	0000 000d dddd dddd	0x0004
0x03	Window Height Context A	0000 000d dddd dddd	0x01E0
0x04	Window Width Context A	0000 00dd dddd dddd	0x02F0
0x05	Horizontal Blanking Context A	0000 00dd dddd dddd	0x005E
0x06	Vertical Blanking Context A	0ddd dddd dddd dddd	0x002D
0x07	Chip Control	0000 dddd dddd dddd	0x0388
0x08	Coarse Shutter Width 1 Context A	0ddd dddd dddd dddd	0x01BB
0x09	Coarse Shutter Width 2 Context A	0ddd dddd dddd dddd	0x01D9
0x0A	Shutter Width Ctrl Context A	0000 00dd dddd dddd	0x0164
0x0B	Coarse Total Shutter Width Context A	0ddd dddd dddd dddd	0x01E0
0x0C	Reset	0000 0000 0000 00dd	0x0000
0x0D	Read Mode Context A	0000 0011 dddd dddd	0x0300
0x0E	Read Mode Context B	0000 0000 00dd dddd	0x0000
0x0F	Sensor Type, HDR Enable	0000 000d 0000 00dd	0x0100
0x10	Reserved	–	0x0040
0x11	Reserved	–	0x8042
0x12	Reserved	–	0x0022
0x13	Reserved	–	0x2D32
0x14	Reserved	–	0x0E02
0x15	Reserved	–	0x0E32
0x16	Reserved	–	0x2802
0x17	Reserved	–	0x3E38
0x18	Reserved	–	0x3E38
0x19	Reserved	–	0x2802
0x1A	Reserved	–	0x0428
0x1B	LED_OUT Ctrl	0000 0000 0000 00dd	0x0000
0x1C	Companding	0000 00dd 0000 00dd	0x0302
0x1D	Reserved	–	0x0040
0x1E	Reserved	–	0x0000
0x1F	Reserved	–	0x0000
0x20	Reserved	–	0x01C1
0x21	Reserved	–	0x0020
0x22	Reserved	–	0x0020
0x23	Reserved	–	0x0010
0x24	Reserved	–	0x0010
0x25	Reserved	–	0x0020
0x26	Reserved	–	0x0004



**Table 1: Register List (continued)**  
1 = always 1; 0 = always 0; d = programmable; ? = read only

Register Number (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x27	Reserved	–	0x000C
0x28	Reserved	–	0x0010
0x29	Reserved	–	0x0010
0x2A	Reserved	–	0x0020
0x2B	Reserved	–	0x0004
0x2C	VREF_ADC Control	0000 0000 0000 0ddd	0x0004
0x2D	Reserved	–	0x0004
0x2E	Reserved	–	0x0007
0x2F	Reserved	–	0x0004
0x30	Reserved	–	0x0003
0x31	V1 Context A	0000 0000 000d dddd	0x0027
0x32	V2 Context A	0000 0000 000d dddd	0x001A
0x33	V3 Context A	0000 0000 000d dddd	0x0005
0x34	V4 Context A	0000 0000 000d dddd	0x0003
0x35	Analog Gain Context A	0000 0000 0ddd dddd	0x0010
0x36	Analog Gain Context B	0000 0000 0ddd dddd	0x8010
0x37	Reserved	–	0x0000
0x38	Reserved	–	0x0000
0x39	V1 Control Context B	0000 0000 00dd dddd	0x27
0x3A	V2 Control Context B	0000 0000 00dd dddd	0x26
0x3B	V3 Control Context B	0000 0000 00dd dddd	0x5
0x3C	V4 Control Context B	0000 0000 00dd dddd	0x3
0x40	Reserved	0000 0000 ???? ????	RO
0x42	Frame Dark Average	0000 0000 ???? ????	RO
0x46	Dark Avg Thresholds	dddd dddd dddd dddd	0x231D
0x47	BL Calib Control	1000 0000 ddd0 000d	0x0080
0x48	Black Level Calibration Value	0000 0000 dddd dddd	0x0000
0x4C	BL Calib Step Size	0000 0000 000d dddd	0x0002
0x60	Reserved	0000 0000 0000 0000	0x0000
0x61– 0x66	Unused	–	0x0000
0x67	Reserved	–	0x0000
0x68	Reserved	–	RO
0x69	Reserved	–	RO
0x6A	Reserved	–	RO
0x6B	Reserved	–	RO
0x6C	Reserved	–	0x0000
0x70	Row Noise Corr Control	0000 00dd 0000 00dd	0x0000
0x71	Row Noise Constant	0000 00dd dddd dddd	0x002A
0x72	Pixclk, FV, LV Ctrl	0000 0000 000d dddd	0x0000
0x73 – 0x7E	Unused	–	0x0000
0x7F	Digital Test Pattern	0ddd ddd dddd dddd	0x0000
0x80	Tile Weight/Gain X0_Y0	0000 dddd dddd dddd	0x04F4
0x81	Tile Weight/Gain X1_Y0	0000 dddd dddd dddd	0x04F4
0x82	Tile Weight/Gain X2_Y0	0000 dddd dddd dddd	0x04F4

**Table 1: Register List (continued)**

1 = always 1; 0 = always 0; d = programmable; ? = read only

Register Number (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x83	Tile Weight/Gain X3_Y0	0000 dddd dddd dddd	0x04F4
0x84	Tile Weight/Gain X4_Y0	0000 dddd dddd dddd	0x04F4
0x85	Tile Weight/Gain X0_Y1	0000 dddd dddd dddd	0x04F4
0x86	Tile Weight/Gain X1_Y1	0000 dddd dddd dddd	0x04F4
0x87	Tile Weight/Gain X2_Y1	0000 dddd dddd dddd	0x04F4
0x88	Tile Weight/Gain X3_Y1	0000 dddd dddd dddd	0x04F4
0x89	Tile Weight/Gain X4_Y1	0000 dddd dddd dddd	0x04F4
0x8A	Tile Weight/Gain X0_Y2	0000 dddd dddd dddd	0x04F4
0x8B	Tile Weight/Gain X1_Y2	0000 dddd dddd dddd	0x04F4
0x8C	Tile Weight/Gain X2_Y2	0000 dddd dddd dddd	0x04F4
0x8D	Tile Weight/Gain X3_Y2	0000 dddd dddd dddd	0x04F4
0x8E	Tile Weight/Gain X4_Y2	0000 dddd dddd dddd	0x04F4
0x8F	Tile Weight/Gain X0_Y3	0000 dddd dddd dddd	0x04F4
0x90	Tile Weight/Gain X1_Y3	0000 dddd dddd dddd	0x04F4
0x91	Tile Weight/Gain X2_Y3	0000 dddd dddd dddd	0x04F4
0x92	Tile Weight/Gain X3_Y3	0000 dddd dddd dddd	0x04F4
0x93	Tile Weight/Gain X4_Y3	0000 dddd dddd dddd	0x04F4
0x94	Tile Weight/Gain X0_Y4	0000 dddd dddd dddd	0x04F4
0x95	Tile Weight/Gain X1_Y4	0000 dddd dddd dddd	0x04F4
0x96	Tile Weight/Gain X2_Y4	0000 dddddddd dddd	0x04F4
0x97	Tile Weight/Gain X3_Y4	0000 dddd dddd dddd	0x04F4
0x98	Tile Weight/Gain X4_Y4	0000 dddd dddd dddd	0x04F4
0x99	Tile Coord. X 0/5	0000 00dd dddd dddd	0x0000
0x9A	Tile Coord. X 1/5	0000 00dd dddd dddd	0x0096
0x9B	Tile Coord. X 2/5	0000 00dd dddd dddd	0x012C
0x9C	Tile Coord. X 3/5	0000 00dd dddd dddd	0x01C2
0x9D	Tile Coord. X 4/5	0000 00dd dddd dddd	0x0258
0x9E	Tile Coord. X 5/5	0000 00dd dddd dddd	0x02F0
0x9F	Tile Coord. Y 0/5	0000 000d dddd dddd	0x0000
0xA0	Tile Coord. Y 1/5	0000 000d dddd dddd	0x0060
0xA1	Tile Coord. Y 2/5	0000 000d dddd dddd	0x00C0
0xA2	Tile Coord. Y 3/5	0000 000d dddd dddd	0x0120
0xA3	Tile Coord. Y 4/5	0000 000d dddd dddd	0x0180
0xA4	Tile Coord. Y 5/5	0000 000d dddd dddd	0x01E0
0xA5	AEC/AGC Desired Bin	0000 0000 00dd dddd	0x003A
0xA6	AEC Update Frequency	0000 0000 0000 dddd	0x0002
0xA7	Unused	0000 0000 0000 0000	0x0000
0xA8	AEC LPF	0000 0000 0000 00dd	0x0000
0xA9	AGC Update Frequency	0000 0000 0000 dddd	0x0002
0xAA	AGC LPF	0000 0000 0000 00dd	0x0002
0xAB	Max Analog Gain	0000 0000 0ddd dddd	0x0040
0xAC	AEC Minimum Exposure	dddd dddd dddd dddd	0x0001
0xAD	AEC Maximum Exposure	dddd dddd dddd dddd	0x01E0
0xAE	Bin Difference Threshold	0000 0000 dddd dddd	0x0014



**Table 1: Register List (continued)**  
1 = always 1; 0 = always 0; d = programmable; ? = read only

Register Number (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0xAF	AEC/AGC Enable A/B	0000 00dd 0000 00dd	0x0003
0xB0	AEC/AGC Pix Count	dddd dddd dddd dddd	0xABE0
0xB1	LVDS Master Ctrl	0000 0000 0000 dddd	0x0002
0xB2	LVDS Shift Clk Ctrl	0000 0000 000d 0ddd	0x0010
0xB3	LVDS Data Ctrl	0000 0000 000d 0ddd	0x0010
0xB4	Data Stream Latency	0000 0000 0000 00dd	0x0000
0xB5	LVDS Internal Sync	0000 0000 0000 000d	0x0000
0xB6	LVDS Payload Control	0000 0000 0000 000d	0x0000
0xB7	Stereoscop. Error Ctrl	0000 0000 0000 0ddd	0x0000
0xB8	Stereoscop. Error Flag	0000 0000 0000 000?	RO
0xB9	LVDS Data Output	???? ???? ???? ????	RO
0xBA	AGC Gain Output	0000 0000 0??? ????	RO
0XBB	AEC Gain Output	???? ???? ???? ????	RO
0xBC	AGC/AEC Current Bin	0000 0000 00?? ????	RO
0xBD – 0xBE	Reserved	0000 0000 0000 0000	0x0000
0xBF	Interlace Field Blank	0000 000d dddd dddd	0x0016
0xC0	Mon Mode Capture Ctrl	0000 0000 dddd dddd	0x000A
0xC1	Reserved	0000 00?? ???? ????	RO
0xC2	Anti-eclipse Controls	00dd d000 d100 0000	0x0840
0xC3	Reserved	0000 000? ???? ????	0x007F
0xC4	Reserved	0000 0000 ???? ????	0x007F
0xC5	Reserved	0000 0000 ???? ????	0x007F
0xC6	NTSV FV and LV Control	0000 0000 0000 00dd	0x0
0xC7	NTSC Horiz Blank Ctrl	dddd dddd dddd dddd	0x4416
0xC8	NTSC Vert Blank Ctrl	dddd dddd dddd dddd	0x4421
0xC9	Column Start Context B	0000 00dd dddd dddd	0x001
0xCA	Row Start Context B	0000 000d dddd dddd	0x004
0xCB	Window Height Context B	0000 000d dddd dddd	0x1E0
0xCC	Window Width Context B	0000 00dd dddd dddd	0x2F0
0xCD	Horizontal Blanking Context B	0000 00dd dddd dddd	0x5E
0xCE	Vertical Blanking Context B	0ddd dddd dddd dddd	0x2D
0xCF	Coarse SW1 Context B	0ddd dddd dddd dddd	0x1DE
0xD0	Coarse SW2 Context B	0ddd dddd dddd dddd	0x1DF
0xD1	Shutter Width Ctrl Context B	0000 00dd dddd dddd	0x064
0xD2	Coarse Shutter Width Total Context B	0ddd dddd dddd dddd	0x1E0
0xD3	Fine SW1 Context A	0000 00dd dddd dddd	0x0000
0xD4	Fine SW2 Context A	0000 00dd dddd dddd	0x0000
0xD5	Fine Shutter Width Total Context A	0000 0ddd dddd dddd	0x0000
0xD6	Fine SW1 Context B	0000 0ddd dddd dddd	0x0000
0xD7	Fine SW2 Context B	0000 0ddd dddd dddd	0x0000
0xD8	Fine Shutter Width Total Context B	0000 0ddd dddd dddd	0x0000
0xD9	Monitor Mode	0000 0000 0000 000d	0x0000
0xF0	Byte-wise Addr	0000 0000 dddd dddd	0x0000
0xFE	Register Lock	dddd dddd dddd dddd	0xBEEF



## Shadowed Registers

Some sensor settings cannot be changed during frame readout. For example, changing window width R0x04 part way through frame readout results in inconsistent LV behavior. To avoid this, the MT9V034 double-buffers many registers by implementing a “pending” and a “live” version. Two-wire serial interface READs and WRITEs access the pending register. The live register controls the sensor operation. The value in the pending register is transferred to a live register at a fixed point in the frame timing, called “frame-start.” Frame-start is defined as the point at which the first dark row is read out. By default, this occurs four row times before FRAME\_VALID (FV) goes HIGH. To determine which registers or register fields are double-buffered in this way, see the “Shadowed” column in Table 2.

Notation used in the register description table:

- Shadowed  
N = No. The register value is updated and used immediately.  
Y = Yes. The register value is updated at next frame start. Frame start is defined as when the first dark row is read out. By default this is four rows before FV goes HIGH.
- Read/Write  
R = Read-only register/bit.  
W = Read/Write register/bit.

Table 2 provides a detailed description of the registers. Bit fields that are not identified in the table are read only.

**Table 2: Register Descriptions**

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0x00/0xFF (0/255) Chip Version						
15:0	Chip Version	Chip version—read-only	0x1324 (4900)			R
0x01 (1) Column Start Context A						
9:0	Column Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Readable/active columns are 1–752.	001 (1)	Y	1–752	W
0x02 (2) Row Start Context A						
8:0	Row Start	The first row to be read out (not counting any dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than four is not recommended since the dark rows should be read using R0x0D.	004 (4)	N	4–482	W
0x03 (3) Window Height Context A						
8:0	Window Height	Number of rows in the image to be read out (not counting any dark rows or border rows that may be read).	1E0 (480)	Y	1–480	W
0x04 (4) Window Width Context A						
9:0	Window Width	Number of columns in image to be read out (not counting any dark columns or border columns that may be read).	2F0 (752)	N	1–752	W
0x05 (5) Horizontal Blanking Context A						



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
9:0	Horizontal Blanking	Number of blank columns in a row. Minimum horizontal blanking is 61 for normal mode, 71 for column bin 2 mode, and 91 for column bin 4 mode	05E (94)	Y	61–1023	W
0x06 (6) Vertical Blanking Context A						
14:0	Vertical Blank	Number of blank rows in a frame. V-Blank value must meet the following minimums: Linear Mode: V-Blank (min) = (SW_total - SW1 + 7) = SW_total - R0x08 + 7 If manual exposure, then SW_total = R0x0B. If auto-exposure mode then SW_total = R0xAD.  High Dynamic Range Mode: If Auto-Knee Point disabled, then above equations apply. If Auto-Knee Point enabled, then V-Blank (min) = (t2 + t3 + 7).  Notes: 1. Calculate t2 and t3 taking into account Auto-Exposure setting. 2. When Sequential Mode is enabled, this register is ineffective. Vertical blank = exposure + 6 rows.	002D (45)	N	2–32288	W
0x07 (7) Chip Control						
2:0	Scan Mode	0 = Progressive scan. 1 = Not valid. 2 = Two-field Interlaced scan. Even-numbered rows are read first, and followed by odd-numbered rows. 3 = Single-field Interlaced scan. If the start address is an even number, only even-numbered rows are read out; if the start address is an odd number, only odd-numbered rows are read out. Effective image size is decreased by half.	0	Y	0, 2, 3	W
4–3	Sensor Operating Mode	0 = Slave mode. The user is allowed to initiate exposure and readout. 1 = Master mode. Sensor generates its own exposure and readout timing according to simultaneous/ sequential mode control bit. 2 = Invalid mode. 3 = Snapshot mode. The user triggers the start of frame by providing a pulse at EXPOSURE pin.	1	Y	0,1, 3	W
5	Stereoscopy Mode	0 = Stereoscopy disabled. Sensor is stand-alone and the PLL generates a 320 MHz (x12) clock. Typical maximum cable length is 8 meters. 1 = Stereoscopy enabled. The PLL generates a 540 MHz (x18) clock. Typical maximum cable length is 5 meters.	0	Y	0,1	W
6	Stereoscopic Master/Slave mode	0 = Stereoscopic master. 1 = Stereoscopic slave. Stereoscopy mode should be enabled when using this bit.	0	Y	0,1	W

Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
7	Parallel Output Enable	0 = Disables parallel output, LV and FV. DOUT[9:0], FRAME_VALID, and LINE_VALID are forced to logic "0" in sensor digital core. It does not control pads. 1 = Enables parallel output.	1	Y	0,1	W
8	Simultaneous/Sequential Mode	0 = Sequential mode. Pixel and column readout take place only after exposure is complete. 1 = Simultaneous mode. Pixel and column readout take place in conjunction with exposure.	1	Y	0,1	W
9	Defective Pixel Correction Enable	0 = Disable Defective Pixel Correction feature. 1 = Enable Defective Pixel Correction feature.	1	Y	0, 1	W
15	Context A/B Select	0 = Context A registers are used. 1 = Context B registers are used.	0	Y	0, 1	W
0x08 (8) Coarse Shutter Width 1 Context A						
14:0	Coarse Shutter Width 1	The row number in which the first knee occurs. This may be used when high dynamic range is enabled (R0x0F[0] = 1) and exposure knee point auto adjust is disabled (R0x0A[8] = 0). This register is not shadowed, but any change made does not take effect until the following new frame. This register's minimum value is 2, for either linear or HDR modes. Note: t1 = Shutter width 1; t2 = Shutter width 2 - Shutter width 1; t3 = total integration - Shutter width 2.	1BB (443)	N	0–32765	W
0x09 (9) Coarse Shutter Width 2 Context A						
14:0	Course Shutter Width 2	The row number in which the second knee occurs. This may be used only when high dynamic range is enabled and exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Note: t1 = Shutter width 1; t2 = Shutter width 2 – Shutter 1; t3 = Total integration – Shutter width 2.	1D9 (473)	N	0–32765	W
0x0A (10) Shutter Width Control Context A						
3:0	T2 Ratio	When Exposure Knee Point Auto Adjust is enabled, then one-half to the power of this value indicates the ratio of duration time t2, when saturation control gate is adjusted to level V2, to total coarse integration. This register is not shadowed, but any change made does not take effect until the following new frame. $T2 = \text{Total coarse integration} \times (\frac{1}{2})^{t2\_ratio}$ .	4	N	0–15	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
7:4	T3 Ratio	When Exposure Knee Point Auto Adjust is enabled, then one-half to the power of this value indicates the ratio of duration time $t_3$ , when saturation control gate is adjusted to level V3, to total coarse integration. This register is not shadowed, but any change made does not take effect until the following new frame. $t_3 = \text{Total integration} \times (\frac{1}{2})^{t_3\_ratio}$ . Note: $t_3 = \text{Total integration} - t_2 - t_1$ .	6	N	0–15	W
8	Exposure Knee Point Auto Adjust Enable	0 = Auto adjust disabled. 1 = Auto adjust enabled.	1	N	0,1	W
9	Single Knee Enable	0 = Single knee disabled. 1 = Single knee enabled.	0	N	0,1	W
0x0B (11) Coarse Shutter Width Total Context A						
14:0	Coarse Shutter Width Total	Total integration time in number of rows. This value is used only when AEC is disabled only (bit 0 of R0xAF). This register is not shadowed, but any change made does not take effect until the following new frame.	1E0 (480)	N	0–32765	W
0x0C (12) Reset						
0	Soft Reset	Setting this bit will cause the sensor to abandon the current frame by resetting all digital logic except two-wire serial interface configuration. This is a self-resetting register bit and should always read "0." (This bit de-asserts internal active LOW reset signal for 15 clock cycles.)	0	N	0, 1	W
1	Auto Block Soft Reset	Setting this bit causes the sensor to reset the automatic gain and exposure control logic. This is a self-resetting register bit and should always read "0." (This bit de-asserts internal active LOW reset signal for 15 clock cycles.)	0	Y	0, 1	W
0x0D (13) Read Mode Context A						
1:0	Row Bin	0 = Normal operation. 1 = Row bin 2. Two pixel rows are read per row output. Image size is effectively reduced by a factor of 2 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 2. 2 = Row bin 4. Four pixel rows are read per row output. Image size is effectively reduced by a factor of 4 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 4. 3 = Not valid.	0	Y	0, 1, 2	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
3:2	Column Bin	0 = Normal operation. 1 = Column bin 2. When set, image size is reduced by a factor of 2 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one-half that of master clock. 2 = Column bin 4. When set, image size is reduced by a factor of 4 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one-fourth that of master clock. 3 = Not valid.	0	Y	0, 1, 2	W
4	Row Flip	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Window Height) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Window Height – 1). This ensures that the starting color is maintained. This one pixel adjustment is always performed, for monochrome or color versions.	0	Y	0, 1	W
5	Column Flip	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Window Width) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Window Width – 1). This ensures that the starting color is maintained. This one pixel adjustment is always performed, for monochrome or color versions.	0	Y	0, 1	W
6	Show Dark Rows	When set, three dark rows are output before the active window. Frame valid is thus asserted earlier than normal. This has no effect on integration time or frame rate. Whether the dark rows are shown in the image or not the definition frame start is before the dark rows are read out.	0	Y	0, 1	W
7	Show Dark Columns	When set, 36 dark columns are output before the active pixels in a line. Line valid is thus asserted earlier than normal, and the horizontal blank time is shortened by 36 pixel clocks.	0	Y	0, 1	W
9:8	Reserved	Reserved.	3		3	
0x0E (14) Read Mode Context B						
1:0	Row Bin	0 = Normal Operation 1 = Row bin 2. Two pixel rows are read per row output. Image size is effectively reduced by a factor of 2 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 2. 2 = Row bin 4. Four pixel rows are read per row output. Image size is effectively reduced by a factor of 4 vertically w Resulting frame rate is increased by 4. 3 = Invalid	0	Y	0, 1, 2	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0x0F (15) Sensor Type Control						
0	High Dynamic Range Context A	0 = Linear operation. If Linear mode is selected, then Exposure Knee Point Auto Adjust must also be enabled (R0x0A[8] = 1). 1 = High Dynamic Range. Voltage and shutter width must be correctly set for saturation control to operate.	0	N	0, 1	W
1	Color/Mono Sensor Control	This bit controls some color-specific logic in Black Level Correction and Defective Pixel Correction. 0 = Monochrome 1 = Color It should generally be left at "0" for all part types. It is not required to be set for color sensors to operate properly. When set, it applies an unequal offset to the color planes. For most applications on color parts the bit is best left cleared (monochrome), especially for machine vision applications where predictable image offsets are required. For Black Level Calibration (BLC), when this bit is set, the sensor uses black level correction values from one green plane, which are applied to all colors. Since this bit applies offsets to the color plane, BLC results may be affected. For Defective Pixel Correction (DPC), this bit must be set for the DPC algorithm to calculate replacement pixels based on color plane, otherwise the DPC algorithm will calculate replacement pixels based on nearest-neighbor rather than nearest color-neighbor.	0	Y	0, 1	W
8	High Dynamic Range Context B	0 = Linear operation. If Linear mode is selected, then Exposure Knee Point Auto Adjust must also be enabled (R0xD1[8] = 1). 1 = High Dynamic Range. Voltage and shutter width must be correctly set for saturation control to operate.	1	N	0, 1	W
0x1B (27) LED_OUT Control						
0	Disable LED_OUT	Disable LED_OUT output. When this bit is cleared, the output pin LED_OUT is pulsed HIGH when the sensor is undergoing exposure. When this bit is enabled: If enabled (set to 1), and Invert LED_OUT is disabled, the output pin LED_OUT is held in logic LOW state. If enabled and Invert LED_OUT is enabled, output pin LED_OUT is held in a logic HIGH state.	0	Y	0, 1	W
1	Invert LED_OUT	Inverts polarity of LED_OUT output. When this bit is set, the output pin LED_OUT is pulsed LOW when the sensor is undergoing exposure.	0	Y	0, 1	W
0x1C (28) ADC Companding Mode						
1:0	ADC Mode Context A	0 = Invalid. 1 = Invalid. 2 = 10-bit linear. 3 = 12-to10-bit companding.	2	N	2, 3	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
9:8	ADC Mode Context B	0 = Invalid. 1 = Invalid. 2 = 10-bit linear. 3 = 12-to10-bit companding.	3	N	2,3	W
0x2C (44) – 0x3C (60) Analog Controls Note: These registers are not shadowed, but any change made does not take effect until the following new frame.						
0x2C (44) VREF_ADC Control						
2:0	VREF_ADC Voltage Level	0 = VREF_ADC = 1.0V. 1 = VREF_ADC = 1.1V. 2 = VREF_ADC = 1.2V. 3 = VREF_ADC = 1.3V. 4 = VREF_ADC = 1.4V.(Note: Effective ADC reference voltage is 1.0V.) 5 = VREF_ADC = 1.5V. 6 = VREF_ADC = 1.6V. 7 = VREF_ADC = 2.1V. Range: 1.0–2.1V; Default: 1.4V  Note: This register is not shadowed, but any change made does not take effect until the following new frame.	4	N	0–7	W
0x31 (49) V1 Control Context A						
5:0	V1 voltage level	For bits (5:0) = 0 to 5, $V\_step = \text{bits (5:0)} * 200\text{mV} + 0.2\text{V}$ . Range: 0.2 - 1.2V  For bits (5:0) = 6 to 63 $V\_step = \text{bits (5:0)} * 23.5\text{mV} + 1.62\text{V}$ Range: 1.76-3.1V Note: Equation and range are determined with the assumption that VAA = 3.3V. They may vary with actual VAA voltage. Default: 2.54V Usage: Vstep1 HDR voltage	27 (39)	N	0–63	W
0x32 (50) V2 Control Context A						
5:0	V2 voltage level	For bits (5:0) = 0 to 5, $V\_step = \text{bits (5:0)} * 200\text{mV} + 0.2\text{V}$ . Range: 0.2 - 1.2V  For bits (5:0) = 6 to 63 $V\_step = \text{bits (5:0)} * 23.5\text{mV} + 1.62\text{V}$ Range: 1.76-3.1V Note: equation and range are determined with the assumption that VAA = 3.3V. They may vary with actual VAA voltage. Default: 2.23V Usage: Vstep2 HDR voltage	1A (26)	N	0–63	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0x33 (51) V3 Control Context A						
5:0	V3 voltage level	For bits (5:0) = 0 to 5, $V\_step = \text{bits (5:0)} * 200\text{mV} + 0.2\text{V}$ . Range: 0.2 - 1.2V  For bits (5:0) = 6 to 63 $V\_step = \text{bits (5:0)} * 23.5\text{mV} + 1.62\text{V}$ Range: 1.76-3.1V Note: equation and range are determined with the assumption that $V_{AA} = 3.3\text{V}$ . They may vary with actual $V_{AA}$ voltage. Default: 1.2V Usage: Vstep3 HDR voltage.	05 (5)	N	0–63	W
0x34 (52) V4 Control Context A						
5:0	V4 voltage level	For bits (5:0) = 0 to 5, $V\_step = \text{bits (5:0)} * 200\text{mV} + 0.2\text{V}$ . Range: 0.2 - 1.2V  For bits (5:0) = 6 to 63 $V\_step = \text{bits (5:0)} * 23.5\text{mV} + 1.62\text{V}$ Range: 1.76-3.1V Note: equation and range are determined with the assumption that $V_{AA} = 3.3\text{V}$ . They may vary with actual $V_{AA}$ voltage. Default: 0.8V Usage: Vstep HDR parking voltage, also provides anti-blooming when Vstep is disabled.	03 (3)	N	0–63	W
0x35 (53) Analog Gain Context A						
6:0	Global Analog Gain	Analog gain = bits (6:0) x 0.0625 Range: 16 dec - 64dec for 1X-4X respectively  Column amplifier common gain. Note: No exception detection is installed, user needs to be cautious when programming.	10 (16)	N	16–64	W
15	Global Analog Gain Attenuation	When this bit is set, analog gain will be forced to 0.75X.	0	N	0, 1	W
0x36 (54) Analog Gain Context B						
6:0	Global Analog Gain	Analog gain = bits (6:0) x 0.0625 Range: 16 dec -64dec for 1X-4X respectively  Column amplifier common gain. Note: No exception detection is installed, user needs to be cautious when programming.	10 (16)	N	16–64	W
15	Global Analog Gain Attenuation	When this bit is set, analog gain will be forced to 0.75X.	1	N	0, 1	W





Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0x39 (57) V1 Control Context B						
5:0	V1 Voltage Level	<p>For bits (5:0) = 0 to 5,  <math>V\_step = bits(5:0) * 200mV + 0.2V</math>.            Range: 0.2 - 1.2V</p> <p>For bits (5:0) = 6 to 63  <math>V\_step = bits(5:0) * 23.5mV + 1.62V</math>            Range: 1.76-3.1V            Note: equation and range are determined with the assumption that <math>VAA = 3.3V</math>. They may vary with actual VAA voltage.            Default: 2.54V            Usage: Vstep 1 HDR voltage</p>	27 (39)	N	0-63	W
0x3A (58) V2 Control Context B						
5:0	V2 Voltage Level	<p>For bits (5:0) = 0 to 5,  <math>V\_step = bits(5:0) * 200mV + 0.2V</math>.            Range: 0.2 - 1.2V</p> <p>For bits (5:0) = 6 to 63  <math>V\_step = bits(5:0) * 23.5mV + 1.62V</math>            Range: 1.76-3.1V            Note: Equation and range are determined with the assumption that <math>VAA = 3.3V</math>. They may vary with actual VAA voltage.            Default: 2.51V            Usage: Vstep2 HDR voltage</p>	36 (38)	N	0-63	W
0x3B (59) V3 Control Context B						
5:0	V3 Voltage Level	<p>For bits (5:0) = 0 to 5,  <math>V\_step = bits(5:0) * 200mV + 0.2V</math>.            Range: 0.2 - 1.2V</p> <p>For bits (5:0) = 6 to 63  <math>V\_step = bits(5:0) * 23.5mV + 1.62V</math>            Range: 1.76-3.1V            Note: Equation and range are determined with the assumption that <math>VAA = 3.3V</math>. They may vary with actual VAA voltage.            Default: 1.2V            Usage: Vstep3 HDR voltage</p>	05 (5)	N	0-63	W
0x3C (60) V4 Control Context B						



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
5:0	V4 Voltage Level	For bits (5:0) = 0 to 5, V_step = bits (5:0) * 200mV + 0.2V. Range: 0.2 - 1.2V For bits (5:0) = 6 to 63 V_step = bits (5:0) * 23.5mV + 1.62V Range: 1.76-3.1V Note: Equation and range are determined with the assumption that VAA = 3.3V. They may vary with actual VAA voltage. Default: 0.8V Usage: Vstep HDR parking voltage, also provides anti-blooming when Vstep is disabled.	03 (3)	N	0–63	W
0x42 (66) Frame Dark Average						
7:0	Frame Dark Average	The value read is the frame averaged black level, that is, used in the black level algorithm calculations.	0			R
0x46 (70) Dark Average Thresholds						
7:0	Lower threshold	Lower threshold for targeted black level in ADC LSBs.	1D (29)	N	0–255	W
15:8	Upper threshold	Upper threshold for targeted black level in ADC LSBs.	23 (35)	N	0–255	W
0x47 (71) Black Level Calibration Control						
0	Manual Override	Manual override of black level correction. 1 = Override automatic black level correction with programmed values. (R0x48). 0 = Normal operation (default).	0	N	0, 1	W
7:5	Frames to average over	Two to the power of this value decide how many frames to average over when the black level algorithm is in the averaging mode. In this mode the running frame average is calculated from the following formula: Running frame ave = Old running frame ave - (old running frame ave)/2n + (new frame ave)/ 2n.	4	N	0–7	W
0x48 (72) Black Level Calibration Value						
7:0	Black Level Calibration Value	Analog calibration offset: Negative numbers are represented with two's complement, which is shown in the following formula: Sign = bit 7 (0 is positive, 1 is negative). If positive offset value: Magnitude = bit 6:0. If negative offset value: Magnitude = not (bit 6:0) + 1. During two-wire serial interface read, this register returns the user-programmed value when manual override is enabled (R0x47 bit 0); otherwise, this register returns the result obtained from the calibration algorithm.	–	N	–127 to 127	RW
0x4C (76) Black Level Calibration Value Step Size						
4:0	Step Size of Calibration Value	This is the size calibration value may change (positively or negatively) from frame to frame. Note: 1 calib LSB = ½ ADC LSB, assuming analog gain = 1.	02	N	0–31	W

Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
<b>0x70 (112) Row Noise Correction Control</b>						
0	Enable Noise Correction Context A	0 = Normal operation 1 = Enable row noise cancellation algorithm. When this bit is set, on a per row basis, the dark average will be subtracted from each pixel in the row, and then a constant (Reg 0x71) will be added.	0	N	0, 1	W
1	Use black level average Context A	0 = Use the average value of the dark columns read out in each row as dark average. 1 = Use black level frame average from the dark rows in the row noise correction algorithm for low gains. Note that this frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off.	0	N	0, 1	W
8	Enable noise correction Context B	0 = Normal operation 1 = Enable row noise cancellation algorithm. When this bit is set, on a per row basis, the dark average will be subtracted from each pixel in the row, and then a constant (Reg 0x71) will be added.	0	N	0, 1	W
9	Use black level average Context B	0 = Use the average value of the dark columns read out in each row as dark average. 1 = Use black level frame average from the dark rows in the row noise correction algorithm for low gains. Note that this frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off.	0	N	0, 1	W
<b>0x71 (113) Row Noise Constant</b>						
9:0	Row noise constant	Constant used in the row noise cancellation algorithm. It should be set to the dark level targeted by the black level algorithm plus the noise expected between the averaged values of dark columns. At default the constant is set to 42 LSB.	2A (42)	Y	0–1023	W
<b>0x72 (114) Pixel Clock, FRAME and LINE VALID Control</b>						
0	Invert LINE VALID	Invert LINE_VALID. When set, LINE_VALID will be reset to logic "0" when PDOUT is valid.	0	Y	0, 1	W
1	Invert Frame Valid	Invert FRAME_VALID. When set, FRAME_VALID is reset to logic "0" when frame is valid.	0	Y	0, 1	W
2	XOR Line Valid	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID 0 = LINE_VALID determined by bit 3. Ineffective if Continuous Line Valid is set.	0	Y	0, 1	W
3	Continuous Line Valid	1 = "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blank). 0 = Normal LINE_VALID (default, no LINE_VALID during vertical blank).	0	Y	0, 1	W
4	Invert Pixel Clock	Invert pixel clock. When set, LINE_VALID, FRAME_VALID, and PDOUT will be set up to the rising edge of pixel clock, PIXCLK. When clear, they are set up to the falling edge of PIXCLK.	0	Y	0, 1	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
<b>0x7F (127) Digital Test Pattern</b>						
9:0	Two-wire Serial Interface Test Data	The 10-bit test data in this register is used in place of the data from the sensor. The data is inserted at the beginning of the digital signal processing. Both test enable (bit 13) and use two-wire serial interface (bit 10) must be set.	000	N	0–1023	W
10	Use Two-wire Serial Interface Test Data	0 = Use Gray Shade Test Pattern as test data. 1 = Use Two-wire Serial Interface Test Data (bits 9:0) as test data.	0	N	0, 1	W
12:11	Gray Shade Test Pattern	0 = None. 1 = Vertical Shades. 2 = Horizontal Shades. 3 = Diagonal Shade. When bits (12:11) $\neq$ 0, the MT9V034 generates a gray shaded test pattern to be used as digital test data. Ineffective when Use Two-wire Serial Interface Test Data (bit 10) is set.	0	N	0–3	W
13	Test Enable	Enable the use of test data/gray-shaded test pattern in the signal chain. The data will be inserted instead of data from the ADCs.  When using this mode, disable Row Noise Correction (R0x70 bit 0 and bit 8). If Row Noise Correction is enabled, the row-wise correction algorithm will process the test data values and the result will not be accurate.	0	Y	0, 1	W
14	Flip Two-Wire Serial Interface Test Data	Use only when bit 10 is set. When set, the Two-Wire Test Data (bits 9:0) will be used in place of the data from ADC/memory on odd columns, while complement of the same data will be used on even columns.	0	N	0, 1	W
<b>0x80 (128) - 0x98 (152) Tiled Digital Gain</b>						
3:0	Tile Gain Context A	Tile Digital Gain = Bits (3:0) * 0.25	4 (4)	Y	1–15	W
7:4	Sample Weight	To indicate the weight of individual tile used in the automatic gain/exposure control algorithm	F (15)	Y	1–15	W
11:8	Tile Gain Context B	Tile Digital Gain = Bits (3:0) * 0.25	4 (4)	Y	1–15	W
<b>0x99 (153) – 0xA4 (164) Digital Tile Coordinate</b>						
<b>0x99 (153) Digital Tile Coordinate 1 - X-direction</b>						
9:0	X <sub>0/5</sub>	The starting x-coordinate of digital tiles X0_*.	000 (0)	N	0–752	W
<b>0x9A (154) Digital Tile Coordinate 2 - X-direction</b>						
9:0	X <sub>1/5</sub>	The starting x-coordinate of digital tiles X1_*.	096 (150)	N	0–752	W
<b>0x9B (155) Digital Tile Coordinate 3 - X-direction</b>						
9:0	X <sub>2/5</sub>	The starting x-coordinate of digital tiles X2_*.	12C (300)	N	0–752	W
<b>0x9C (156) Digital Tile Coordinate 4 - X-direction</b>						
9:0	X <sub>3/5</sub>	The starting x-coordinate of digital tiles X3_*.	1C2 (450)	N	0–752	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0x9D (157) Digital Tile Coordinate 5 - X-direction						
9:0	X <sub>4/5</sub>	The starting x-coordinate of digital tiles X4_*.	258 (600)	N	0–752	W
0x9E (158) Digital Tile Coordinate 6 - X-direction						
9:0	X <sub>5/5</sub>	The ending x-coordinate of digital tiles X4_*.	2F0 (752)	N	0–752	W
0x9F (159) Digital Tile Coordinate 1 - Y-direction						
8:0	Y <sub>0/5</sub>	The starting y-coordinate of digital tiles *_Y0.	000 (0)	N	0–480	W
0xA0 (160) Digital Tile Coordinate 2 - Y-direction						
8:0	Y <sub>1/5</sub>	The starting y-coordinate of digital tiles *_Y1.	060 (96)	N	0–480	W
0xA1 (161) Digital Tile Coordinate 3 - Y-direction						
8:0	Y <sub>2/5</sub>	The starting y-coordinate of digital tiles *_Y2.	0C0 (192)	N	0–480	W
0xA2 (162) Digital Tile Coordinate 4 - Y-direction						
8:0	Y <sub>3/5</sub>	The starting y-coordinate of digital tiles *_Y3.	120 (288)	N	0–480	W
0xA3 (163) Digital Tile Coordinate 5 - Y-direction						
8:0	Y <sub>4/5</sub>	The starting y-coordinate of digital tiles *_Y4.	180 (384)	N	0–480	W
0xA4 (164) Digital Tile Coordinate 6 - Y-direction						
8:0	Y <sub>5/5</sub>	The ending y-coordinate of digital tiles *_Y4.	1E0 (480)	N	0–480	W
0xA5 (165) AEC/AGC Desired Bin						
5:0	Desired Bin	User-defined “desired bin” that gives a measure of how bright the image is intended.	3A (58)	Y	1–64	W
0xA6 (166) AEC Update Frequency						
3:0	Exp Skip Frame	The number of frames that the AEC must skip before updating the exposure register (R0xBB).	2	Y	0–15	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
<b>0xA8 (168) AEC Low Pass Filter</b>						
1:0	Exp LPF	<p>This value plays in role in determining the increment/decrement size of exposure value from frame to frame. If current bin <math>\neq 0</math> (R0xBC),</p> <p>When Exp LPF = 0: Actual new exposure = Calculated new exposure.</p> <p>When Exp LPF = 1: if <math> (Calculated. new exp - current exp)  &gt; (current exp / 4)</math>, Actual new exposure = Calculated new exposure, otherwise Actual new exposure = Current exp +/- (calc new exp/2)</p> <p>When Exp LPF = 2: if <math> (Calculated new exp - current exp)  &gt; (current exp / 4)</math>, Actual new exposure = Calc. new exposure, otherwise Actual new exposure = Current exp +/- (calc new exp/4)</p>	0	Y	0–2	W
<b>0xA9 (169) AGC Output Update Frequency</b>						
3:0	Gain Skip Frame	The number of frames that the AGC must skip before updating the gain register (R0xBA).	2	Y	0–15	W
<b>0xAA (170) AGC Low Pass Filter</b>						
1:0	Gain LPF	<p>This value plays a role in determining the increment/decrement size of gain value from frame to frame. If current bin (R0xBC) <math>\neq 0</math></p> <p>When Gain LPF = 0: Actual new gain = Calculated new gain</p> <p>When Exp LPF = 1: if <math> (Calculated new gain - current gain)  &gt; (current gain / 4)</math>, Actual new gain = Calculated new gain, otherwise Actual new gain = Current gain <math>\pm</math> (calculated new gain / 2)</p> <p>When Exp LPF = 2: if <math> (Calculated new gain - current gain)  &gt; (current gain / 4)</math>, Actual new gain = Calculated new gain, otherwise Actual new gain = Current gain <math>\pm</math> (calculated new gain / 4).</p>	2	Y	0–2	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
<b>0xAB (171) Maximum Analog Gain</b>						
6:0	Maximum Analog Gain	This register is used by the automatic gain control (AGC) as the upper threshold of gain. This ensures the new calibrated gain value will not exceed that which MT9V034 supports. Range: 16 dec -64dec for 1X-4X respectively Note: No exception detection is installed, user needs to be cautious when programming.	40 (64)	N	16–64	W
<b>0xAC (172) Minimum Coarse Shutter Width</b>						
15:0	Minimum Coarse Shutter Width Total	This register is used by the automatic exposure control (AEC) as the lower threshold of exposure. This ensures the new calibrated integration value will not exceed that which MT9V034 supports.	1	N	1–32765	W
<b>0xAD (173) Maximum Coarse Shutter Width</b>						
15:0	Maximum Coarse Shutter Width Total	This register is used by the automatic exposure control (AEC) as the upper threshold of exposure. This ensures the new calibrated integration value will not exceed that which MT9V034 supports.	01E0 (480)	N	1–32765	W
<b>0xAE (174) AGC/AEC Bin Difference Threshold</b>						
7:0	Bin Difference Threshold	This register is used by the AEC if exposure reaches the Minimum Coarse Shutter Width value (R0xAC). Then if the difference between desired bin (R0xA5) and current bin (R0xBC) is larger than the threshold, the exposure will be increased.	14 (20)	Y	0–63	W
<b>0xAF (175) AGC/AEC Enable</b>						
0	AEC Enable Context A	0 = Disables Automatic Exposure Control. 1 = Enables Automatic Exposure Control.	1	Y	0, 1	W
1	AGC Enable Context A	0 = Disables Automatic Gain Control. 1 = Enables Automatic Gain Control.	1	Y	0, 1	W
8	AEC Enable Context B	0 = Disables Automatic Exposure Control. 1 = Enables Automatic Exposure Control.	0	Y	0, 1	W
9	AGC Enable Contest B	0 = Disables Automatic Gain Control. 1 = Enables Control.	0	Y	0, 1	W
<b>0xB0 (176) AGC/AEC Pixel Count</b>						
15:0	Pixel Count	The number of pixel used for the AEC/AGC histogram.	ABE0 (44,000)	Y	0–65535	W
<b>0xB1 (177) LVDS Master Control</b>						
0	PLL Bypass	0 = Internal shift-CLK is driven by PLL. 1 = Internal shift-CLK is sourced from the LVDS_BYPASS_CLK.	0	Y	0, 1	W
1	LVDS Power-down	0 = Normal operation. 1 = Powers down LVDS block.	1	Y	0, 1	W
2	PLL Test Mode	0 = Normal operation. 1 = The PLL output frequency is equal to the system clock frequency (26.6 MHz).	0	Y	0, 1	W
3	LVDS Test Mode	0 = Normal operation. 1 = The SER_DATAOUT_P drives a square wave in both stereo and stand-alone modes). In stereo mode, ensure that SER_DATAIN_P is logic "0."	0	Y	0, 1	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
<b>0xB2 (178) LVDS Shift Clock Control</b>						
2:0	Shift-clk Delay Element Select	The amount of shift-CLK delay that minimizes inter-sensor skew.	0	Y	0–7	W
4	LVDS Clock Output Enable	When this bit is set, the LVDS Clock (SHFT_CLKOUT) pins are disabled. Has no effect on SER_DATAOUT pins.	1	Y	0, 1	W
<b>0xB3 (179) LVDS Data Control</b>						
2:0	Data Delay Element Select	The amount of data delay that minimizes inter-sensor skew.	0	Y	0–7	W
4	LVDS Data Input Enable	When this bit is set, the LVDS Data Receiver (SER_DATAIN pins) is disabled. If this bit is changed, it is mandatory that a soft reset (R0x0C) is then issued for proper operation.	1	Y	0, 1	W
<b>0xB4 (180) LVDS Latency</b>						
1:0	Stream Latency Select	The amount of delay so that the two streams are in sync.	0	Y	0–3	W
<b>0xB5 (181) LVDS Internal Sync</b>						
0	LVDS Internal Sync Enable	When this bit is set, the MT9V034 generates sync pattern (data with all zeros except start bit) on LVDS_SER_DATA_OUT.	0	Y	0, 1	W
<b>0xB6 (182) LVDS Payload Control</b>						
0	Use 10-bit Pixel Enable	When this bit is set, all 10 bits will contain pixel (with embedded controls) in standalone mode. If clear, payload will be 8 bits of pixel with 2 bits of controls.	0	Y	0, 1	W
<b>0xB7 (183) Stereoscopic Error Control</b>						
0	Enable Stereo Error Detect	Set this bit to enable stereo error detect mechanism.	0	Y	0, 1	W
1	Enable Stick Stereo Error Flag	When this bit is set, the stereo error flag remains asserted once an error is detected unless clear stereo error flag (bit 2) is set.	0	Y	0, 1	W
2	Clear Stereo Error Flag	Set this bit to clear the stereoscopic error flag (R0xB8 returns to logic 0).	0	Y	0, 1	W
<b>0xB8 (184) Stereoscopic Error Flag</b>						
0	Stereoscopic Error Flag	Stereoscopic error status flag. It is also directly connected to the ERROR output pin.				R
<b>0xB9 (185) LVDS Data Output</b>						
15:0	Combo Reg	This 16-bit value contains both 8-bit pixel values from both stereoscopic master and slave sensors. It can be used in diagnosis to determine how well in sync the two sensors are. Captures the state when master sensor has issued a reserved byte and slave has not. Note: This register should be read from the stereoscopic master sensor only.				R
<b>0xBA (186) AGC Gain Output</b>						
6:0	AGC Gain	Status register to report the current gain value obtained from the AGC algorithm.	10			R
<b>0xBB (187) AEC Exposure Output</b>						
15:0	AEC Exposure	Status register to report the current exposure value obtained from the AEC algorithm.	00C8 (200)			R





Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xBC (188) AGC/AEC Current Bin						
5:0	Current Bin	Status register to report the current bin of the histogram.				R
0xBF (191) Field Vertical Blank						
8:0	Field Vertical Blank	The number of blank rows between odd and even fields. Note: For interlace (both field) mode (R0x07 bits1:0) only.  Note: When Field Vertical Blank is set to 0, the blank time between odd and even fields is one master clock cycle.	016 (22)	Y	1–255	W
0xC0 (192) Monitor Mode Capture Control						
7:0	Image Capture Num	The number of frames to be captured during the wake-up period when monitor mode is enabled.	0A (10)	Y	1–255	W
0xC2 (194) Analog Controls						
6	Reserved	Reserved. Leave at "1"	1	N	0, 1	W
7	Anti-Eclipse Enable	Setting this bit turns on anti-eclipse circuitry.	0	N	0, 1	W
13:11	V_rst_lim voltage Level	V_rst_lim = bits [13:11] * 50mV + 1.90V Range: 1.90–2.25; Default: 1.95 V Usage: For anti-eclipse reference voltage control	1	N	0–7	W
0xC6 (198) NTSC Frame Valid Control						
0	Extend Frame Valid	When this bit is set, frame valid is extended for half-line in length at the odd field.	0	Y	0, 1	W
1	Replace FV/LV with Ped/Snyc	When this bit is set, frame valid and line valid is replaced by ped and sync signals respectively.	0	Y	0, 1	W
0xC7 (198) NTSC Horizontal Blank Control						
7:0	Front porch width	The front porch width in number of master clock cycles. NTSC standard is 1.5?sec ±0.1?sec	16 (22)	N	0–255	W
15:8	Sync Width	The sync pulse width in number of master clock cycle. NTSC standard is 4.7?sec ±0.1?sec.	44 (68)	N	0–255	W
0xC8 (200) NTSC Vertical Blank Control						
7:0	Equalizing Pulse Width	The pulse width in number of master clock cycles. NTSC standard is 2.3?sec ±0.1?sec.	21 (33)	N	0–255	W
15:8	Vertical Serration Width	The pulse width in number of master clock cycles. NTSC standard is 4.7?sec ±0.1?sec.	44 (68)	N	0–255	W
0xC9 (201) Column Start Context B						
9:0	Column Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value.	000 (1)	N	0–752	W
0xCA (202) Row Start Context B						
8:0	Row Start	The first row to be read out (not counting any dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than four is not recommended since the dark rows should be read using R0x0D.	004 (4)	N	4–2482	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xCB (203) Window Height Context B						
8:0	Window Height	Number of rows in the image to be read out (not counting any dark rows or border rows that may be read).	1E0 (480)	N	1–480	W
0xCC (204) Window Width Context B						
9:0	Window Width	Number of columns in image to be read out (not counting any dark columns or border columns that may be read).	2F0 (752)	N	1–752	W
0xCD(205) Horizontal Blanking Context B						
9:0	Horizontal Blanking	Number of blank columns in a row. Minimum horizontal blanking is 61 for normal mode, 71 for column bin 2 mode, and 91 for column bin 4 mode	05E (94)	N	61–71023	W
0xCE(206) Vertical Blanking Context B						
14:0	Vertical Blanking	Number of blank rows in a frame. V-Blank value must meet the following minimums: Linear Mode: $V\text{-Blank (min)} = (SW\_total - SW1 + 7)$ $= SW\_total - R0x08 + 7$ If manual exposure, then $SW\_total = R0xD2$ . If auto-exposure mode then $SW\_total = R0xAD$ .  High Dynamic Range Mode: If Auto-Knee Point disabled, then above equations apply. If Auto-Knee Point enabled, then $V\text{-Blank (min)} = (t2 + t3 + 7)$ .  Note: Calculate t2 and t3 taking into account Auto Exposure setting.  Note: When Sequential Mode is enabled, this register is ineffective. Vertical blank = exposure + 6 rows.	002D (45)	N	2–32288	W
0xCF(207) Coarse Shutter Width 1 Context B						
14:0	Coarse Shutter Width 1	The row number in which the first knee occurs. This may be used when high dynamic range is enabled ( $R0x0F[8] = 1$ ) is enabled & exposure knee point auto adjust is disabled ( $R0xD1[8] = 0$ ). This register is not shadowed, but any change made does not take effect until the following new frame. This register minimum value is 2, for either linear or HDR modes.  Note: t1 = Shutter width 1; t2 = Shutter width 2 - Shutter width 1; t3 = total integration - Shutter width 2	1DE (478)	N	0–32765	W

Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xD0(208) Coarse Shutter Width 2 Context B						
14:0	Coarse Shutter Width 2	The row number in which the second knee occurs. This may be used only when high dynamic range is enabled & exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame.  Note: t1 = Shutter width 1; t2 = Shutter width 2 - Shutter width 1; t3 = total integration - Shutter width 2	1DE (479)	N	0–32765	W
0xD1(209) Shutter Width Control Context B						
3:0	T2 Ratio	One-half to the power of this value indicates the ratio of duration time t2, when saturation control gate is adjusted to level V2, to total coarse integration when exposure knee point auto adjust control bit is enabled. This register is not shadowed, but any change made does not take effect until the following new frame.  $T2 = \text{total coarse integration} * (\frac{1}{2})^{t2\_ratio}$	4	N	0–15	W
7:4	T3 Ratio	One-half to the power of this value indicates the ratio of duration time t3, when saturation control gate is adjusted to level V3, to total coarse integration when exposure knee point auto adjust control bit is enabled. This register is not shadowed, but any change made does not take effect until the following new frame.  $T3 = \text{total coarse integration} * (\frac{1}{2})^{t3\_ratio}$  Note: t1 = total coarse integration - t2 - t3	6	N	0–15	W
8	Exposure Knee Point Auto Adjust Enable	0 = Auto adjust disabled. 1 = Auto adjust enabled.	1	N	0,1	W
9	Single Knee Enable	1 = Single knee enabled.	0	N	0,1	W
0xD2 (210) Coarse Shutter Width Total Context B						
14:0	Coarse Shutter Width Total	Total integration time in number of rows. This value is used only when AEC is disabled only (bit 0 of Register 175). This register is not shadowed, but any change made does not take effect until the following new frame.	1E0 (480)	N	0–32765	W

Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xD3 (211) Fine Shutter Width 1 Context A						
10:0	Fine Shutter Width 1	This register, combined with Coarse Shutter Width 1, defines the time when the first knee occurs. This may be used only when high dynamic range is enabled and the exposure knee point auto-adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are master clock cycles. Operational maximum is (row time - 1) = (Window Width + HBLANK - 1) Total maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Notes: t1 = Shutter width 1 t2 = Shutter width 2 - Shutter width 1 t3 = Total integration - Shutter width 2	0 (0)	N	0–1774	W
0xD4 (212) Fine Shutter Width 2 Context A						
10:0	Fine Shutter Width 2	This register, combined with Coarse Shutter Width 2, defines the time when the second knee occurs. This may be used only when high dynamic range is enabled and the exposure knee point auto-adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are master clock cycles. Maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Notes: t1 = Shutter width 1 t2 = Shutter width 2 - Shutter width 1 t3 = Total integration - Shutter width 2	0 (0)	N	0–1774	W
0xD5 (213) Fine Shutter Width Total Context A						
10:0	Fine Shutter Width Total	This register, combined with Coarse Shutter Width Total, defines the total integration time. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are master clock cycles. Maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Note: When Coarse Shutter Width Total is zero, Minimum Fine Shutter Width = 260	0 (0)	N	0–1774	W



Table 2: Register Descriptions (continued)

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xD6 (214) Fine Shutter Width 1 Context B						
10:0	Fine Shutter Width 1	This register, combined with Coarse Shutter Width 1, defines the time when the first knee occurs. This may be used only when high dynamic range is enabled and the exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are master clock cycles. Maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Notes: t1 = Shutter width 1 t2 = Shutter width 2 - Shutter width 1 t3 = Total integration - Shutter width 2	0 (0)	N	0–1774	W
0xD7 (215) Fine Shutter Width 2 Context B						
10:0	Fine Shutter Width 2	This register, combined with Coarse Shutter Width 2, defines the time when the second knee occurs. This may be used only when high dynamic range is enabled and the exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are master clock cycles. Maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Notes: t1 = Shutter width 1 t2 = Shutter width 2 - Shutter width 1 t3 = Total integration - Shutter width 2	0 (0)	N	0–1774	W
0xD8 (216) Fine Shutter Width Total Context B						
10:0	Fine Shutter Width Total	This register, combined with Coarse Shutter Width Total, defines the total integration time. This register is not shadowed, but any change made does not take effect until the following new frame. Register units are in master clock cycles. Maximum is HBLANK (R0x05) + 751 = 1023 + 751 = 1774 Note: When Coarse Shutter Width Total is zero, Minimum Fine Shutter Width = 260	0 (0)	N	0–1774	W
0xD9 (217) Monitor Mode						
10:0	Monitor Mode Enable	Setting this bit puts the sensor into a cycle of sleeping for approximately five minutes, and waking up to capture a programmable number of frames (Register 0XC0). Clearing this bit will resume normal operation.	0 (0)	Y	0–1	W



**Table 2: Register Descriptions (continued)**

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shadowed	Legal Values (Dec)	Read/Write
0xF0 (240) Byte-wise Address						
	Byte-wise Address	Special address to perform 8-bit reads and writes to the sensor. See Two-Wire Interface description for further details on how to use this functionality.				
0xFE (254) Register Lock						
15:0	Register Lock Code	To lock all registers except R0xFE, program data with 0xDEAD; to unlock access to all registers, program data with 0xBEEF.  To lock Registers 0x0D and 0x0E only, program data with 0xDEAF; to unlock, program data with 0xBEEF. While R0x0D and R0x0E are locked, any subsequent writes to those registers will be ignored until registers are unlocked.	BEEF (48,879)	N	48879 (0xBEEF), 57005 (0xDEAD), 57007 (0xDEAF)	W



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## Revision History

Rev. A .....9/26/12

- Initial release

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