1/4-Inch SOC VGA CMOS Digital Image Sensor Die

MT9V111

For the product data sheet, refer to Micron's Web site: www.micron.com

Features

- Micron®DigitalClarity® CMOS Imaging technology
- System-on-a-chip (SOC)—Completely integrated camera system
- Ultra low-power, low-cost CMOS image sensor
- Superior low-light performance
- Up to 30 fps progressive scan at 27 MHz for high-quality video at VGA resolution
- On-die image flow processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, 2X fixed zoom
- Image decimation to arbitrary size with smooth, continuous zoom and pan
- Automatic exposure, white balance and black compensation, flicker avoidance, color saturation, and defect identification and correction, auto frame rate, black light compensation
- Xenon and LED flash support
- Two-wire serial programming interface
- ITU-R BT.656 (YCbCr), YUV, 565RGB, 555RGB, or 444RGB output data formats

General Physical Specifications

Die thickness: 200µm ±12µm*(Consult factory for other die thickness)*

- Backside wafer surface of polished bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.1kÅ
- Typical metal 3 thickness: 6.1kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 6.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

2.8V Power Supply

Die: MT9V111D00STCK82AC1

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database K82A

- Die outline, see Figure 2 on page 8
- Singulated die size (nominal dimension): 6,225µm ±25µm x 6,225µm ±25µm
- Bond Pad Location and Identification Tables, see page 4–8

Options

- Form
  - Die D
- Testing
  - Standard (level 1) probe C1

Product#	Form	Temp	Chrom	Die database	Testing level

MT9V111D00STCK82AC1

Key Performance Parameters

- Optical format: 1/4-inch (4:3)
- Active imager size: 3.58mm(H) x 2.69mm(V), 4.48mm diagonal
- Active pixels: 640H x 480V (VGA)
- Pixel size: 5.6µm x 5.6µm
- Color filter array: RGB bayer pattern
- Shutter type: electronic rolling shutter (ERS)
- Data rate/master clock: 12–13.5 MPS/24–27 MHz
- Frame rate: VGA (640H x 480V) 15 fps at 12 MHz (default), programmable up to 30 fps at 27 MHz
  CIF (352H x 288V) programmable up to 60 fps
  QVGA (320H x 240V) programmable up to 90 fps
- ADC resolution: 10 bit, on die
- Responsivity: 1.9V/lux-sec (550nm)
- Dynamic range: 60 dB
- SNR MAX: 45dB
- Supply voltage: 2.8V ±0.25V
- Power consumption: <80mW at 2.8V, 15 fps at 12 MHz
- Operating temperature: –30°C to +70°C

General Description

The Micron Imaging MT9V111 die is a VGA-format 1/4-inch CMOS active-pixel digital image sensor, the result of combining the MT9V011 image sensor core with Micron Imaging's third-generation digital image flow processor (IFP) technology. The MT9V111 has an active imaging pixel array of 649 x 489, capturing high-quality color images at VGA resolution. The sensor is a complete camera-on-a-chip solution and is designed specifically to meet the demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-die and is programmable through a simple two-wire serial interface.

This SOC VGA CMOS image sensor die features DigitalClarity—Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The MT9V111 die is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed via a parallel eight-bit DOUT port as shown in Figure 1 on page 3. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. The sensor can be put in an ultra-low power sleep mode by asserting the STANDBY signal. Output pads can also be tri-stated by de-asserting the OE# signal. The MT9V111 die internal registers can be configured using a two-wire serial interface.

Die Testing Procedures

Micron imager die products are tested with a standard probe (C1) test. Wafer probe is performed at an elevated temperature to test product functionality in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die A/D converter, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Micron's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For functional and parametric specifications, refer to the product data sheet found on Micron's Web site.

Bonding Instructions

The MT9V111 Imager die has 44 bond pads. Refer to Table 1 on page 4 and Table 2 on page 6 for a complete list of bond pads and coordinates.

The MT9V111 Imager die does not require the user to determine bond option features.

The MT9V111 Imager die also has several pads defined as “do not use.” These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 3 shows the MT9V111 typical die connections. For low-noise operation, the MT9V111 die requires separate supplies for analog and digital power.

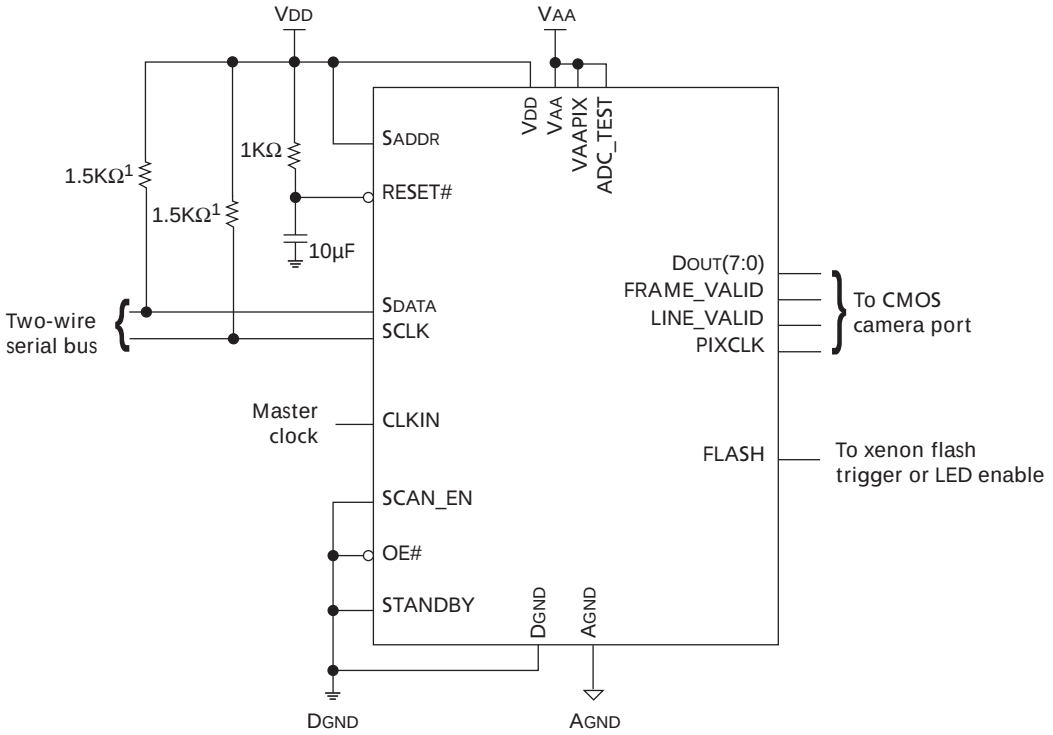
Storage Requirements

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing reliability evaluations. Micron’s QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as the “Accelerated Life” and “Environmental Stress” tests. During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Figure 1: Typical Configuration (Connection)



Notes: 1. A resistor value of 1.5kΩ is recommended, but may be greater for slower two-wire speed.

Bond Pad Location and Identification Tables

Table 1: MT9V111 Bond Pad Location and Identification From Center of Pad 1

Pad	MT9V111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND3	0.00	0.00	0.0000000	0.0000000
2	DOUT2	466.56	0.00	0.0183685	0.0000000
3	DOUT3	933.12	0.00	0.0367370	0.0000000
4	DOUT4	1399.68	0.00	0.0551055	0.0000000
5	DOUT5	1866.24	0.00	0.0734740	0.0000000
6	DGND4	2332.80	0.00	0.0918425	0.0000000
7	VDD3	2799.36	0.00	0.1102110	0.0000000
8	DOUT6	3686.72	0.00	0.1451465	0.0000000
9	DOUT7	4153.28	0.00	0.1635150	0.0000000
10	VDD4	4619.84	0.00	0.1818835	0.0000000
11	DGND5	5086.40	0.00	0.2002520	0.0000000
12	VDD5	5502.95	–416.55	0.2166514	–0.0163994
13	VDD6	5502.95	–883.11	0.2166514	–0.0347679
14	DGND	5502.95	–1349.67	0.2166514	–0.0531364
15	DGND6	5502.95	–1816.23	0.2166514	–0.0715049
16	VDD7	5502.95	–2282.79	0.2166514	–0.0898734
17	DGND7	5502.95	–2749.35	0.2166514	–0.1082419
18	OE#	5502.95	–3215.91	0.2166514	–0.1266104
19	STANDBY	5502.95	–3682.47	0.2166514	–0.1449789
20	RESET#	5502.95	–4149.03	0.2166514	–0.1633474
21	VAAPIX	5502.95	–4655.91	0.2166514	–0.1833033
22	ADC_TEST	5502.95	–5142.63	0.2166514	–0.2024656
23	AGND1	5086.40	–5798.21	0.2002520	–0.2282760
24	VAA1	4619.84	–5798.21	0.1818835	–0.2282760
25	AGND0	4153.28	–5798.21	0.1635150	–0.2282760
26	VAA0	3686.72	–5798.21	0.1451465	–0.2282760
27	VDD0	2799.36	–5798.21	0.1102110	–0.2282760
28	DGND0	2332.80	–5798.21	0.0918425	–0.2282760
29	SADDR	1866.24	–5798.21	0.0734740	–0.2282760
30	SDATA	1399.68	–5798.21	0.0551055	–0.2282760
31	SCLK	933.12	–5798.21	0.0367370	–0.2282760
32	CLKIN	466.56	–5798.21	0.0183685	–0.2282760
33	DGND1	0.00	–5798.21	0.0000000	–0.2282760
34	VDD1	–295.27	–5142.63	–0.0116246	–0.2024656

Table 1: MT9V111 Bond Pad Location and Identification From Center of Pad 1 (continued)

Pad	MT9V111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
35	FRAME_VALID	–295.27	–4655.91	–0.0116246	–0.1833033
36	LINE_VALID	–295.27	–4149.03	–0.0116246	–0.1633474
37	PIXCLK	–295.27	–3682.47	–0.0116246	–0.1449789
38	FLASH	–295.27	–3215.91	–0.0116246	–0.1266104
39	DGND2	–295.27	–2749.35	–0.0116246	–0.1082419
40	DNU[2]	–295.27	–2282.79	–0.0116246	–0.0898734
41	DNU	–295.27	–1816.23	–0.0116246	–0.0715049
42	DOUT0	–295.27	–1349.67	–0.0116246	–0.0531364
43	DOUT1	–295.27	–883.11	–0.0116246	–0.0347679
44	VDD2	–295.27	–416.55	–0.0116246	–0.0163994

Notes: 1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions" on page 2.

Table 2: MT9V111 Bond Pad Location and Identification From Center of Die (0,0)

Pad	MT9V111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	DGND3	–2603.84	2899.11	–0.1025134	0.1141380
2	DOUT2	–2137.28	2899.11	–0.0841449	0.1141380
3	DOUT3	–1670.72	2899.11	–0.0657764	0.1141380
4	DOUT4	–1204.16	2899.11	–0.0474079	0.1141380
5	DOUT5	–737.60	2899.11	–0.0290394	0.1141380
6	DGND4	–271.04	2899.11	–0.0106709	0.1141380
7	VDD3	195.52	2899.11	0.0076976	0.1141380
8	DOUT6	1082.88	2899.11	0.0426331	0.1141380
9	DOUT7	1549.44	2899.11	0.0610016	0.1141380
10	VDD4	2016.00	2899.11	0.0793701	0.1141380
11	DGND5	2482.56	2899.11	0.0977386	0.1141380
12	VDD5	2899.11	2482.56	0.1141380	0.0977386
13	VDD6	2899.11	2016.00	0.1141380	0.0793701
14	DGND	2899.11	1549.44	0.1141380	0.0610016
15	DGND6	2899.11	1082.88	0.1141380	0.0426331
16	VDD7	2899.11	616.32	0.1141380	0.0242646
17	DGND7	2899.11	149.76	0.1141380	0.0058961
18	OE#	2899.11	–316.80	0.1141380	–0.0124724
19	STANDBY	2899.11	–783.36	0.1141380	–0.0308409
20	RESET#	2899.11	–1249.92	0.1141380	–0.0492094
21	VAAPIX	2899.11	–1756.80	0.1141380	–0.0691654
22	ADC_TEST	2899.11	–2243.52	0.1141380	–0.0883276
23	AGND1	2482.56	–2899.11	0.0977386	–0.1141380
24	VAA1	2016.00	–2899.11	0.0793701	–0.1141380
25	AGND0	1549.44	–2899.11	0.0610016	–0.1141380
26	VAA0	1082.88	–2899.11	0.0426331	–0.1141380
27	VDD0	195.52	–2899.11	0.0076976	–0.1141380
28	DGND0	–271.04	–2899.11	–0.0106709	–0.1141380
29	SADDR	–737.60	–2899.11	–0.0290394	–0.1141380
30	SDATA	–1204.16	–2899.11	–0.0474079	–0.1141380
31	SCLK	–1670.72	–2899.11	–0.0657764	–0.1141380
32	CLKIN	–2137.28	–2899.11	–0.0841449	–0.1141380
33	DGND1	–2603.84	–2899.11	–0.1025134	–0.1141380
34	VDD1	–2899.11	–2243.52	–0.1141380	–0.0883276
35	FRAME_VALID	–2899.11	–1756.80	–0.1141380	–0.0691654
36	LINE_VALID	–2899.11	–1249.92	–0.1141380	–0.0492094
37	PIXCLK	–2899.11	–783.36	–0.1141380	–0.0308409
38	FLASH	–2899.11	–316.80	–0.1141380	–0.0124724
39	DGND2	–2899.11	149.76	–0.1141380	0.0058961

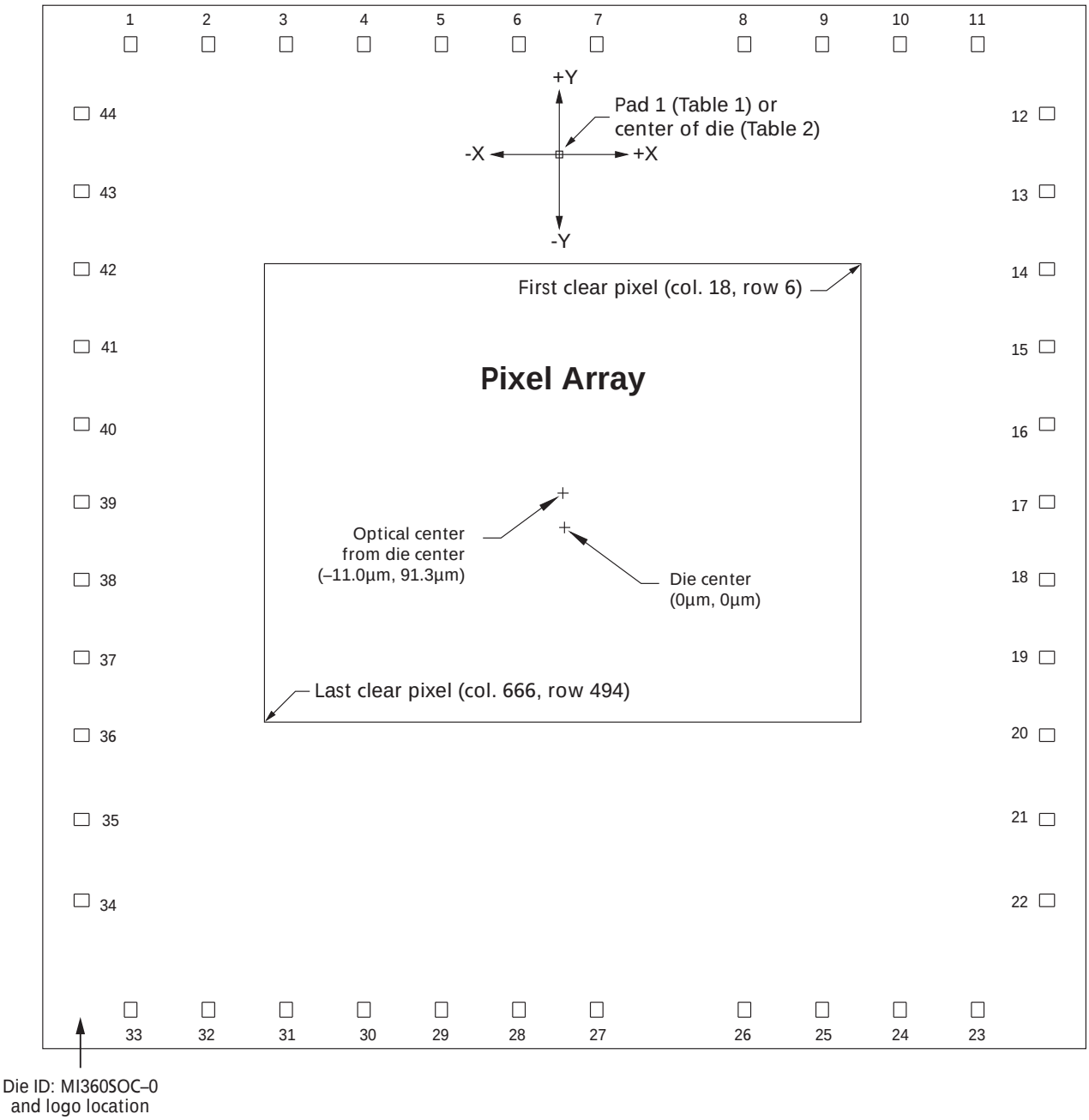
Table 2: MT9V111 Bond Pad Location and Identification From Center of Die (0,0) (continued)

Pad	MT9V111	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
40	DNU[2]	–2899.11	616.32	–0.1141380	0.0242646
41	DNU	–2899.11	1082.88	–0.1141380	0.0426331
42	DOUT0	–2899.11	1549.44	–0.1141380	0.0610016
43	DOUT1	–2899.11	2016.00	–0.1141380	0.0793701
44	VDD2	–2899.11	2482.56	–0.1141380	0.0977386

Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use." See "Bonding Instructions" on page 2.

Die Features

Figure 2: Die Outline (Top View)

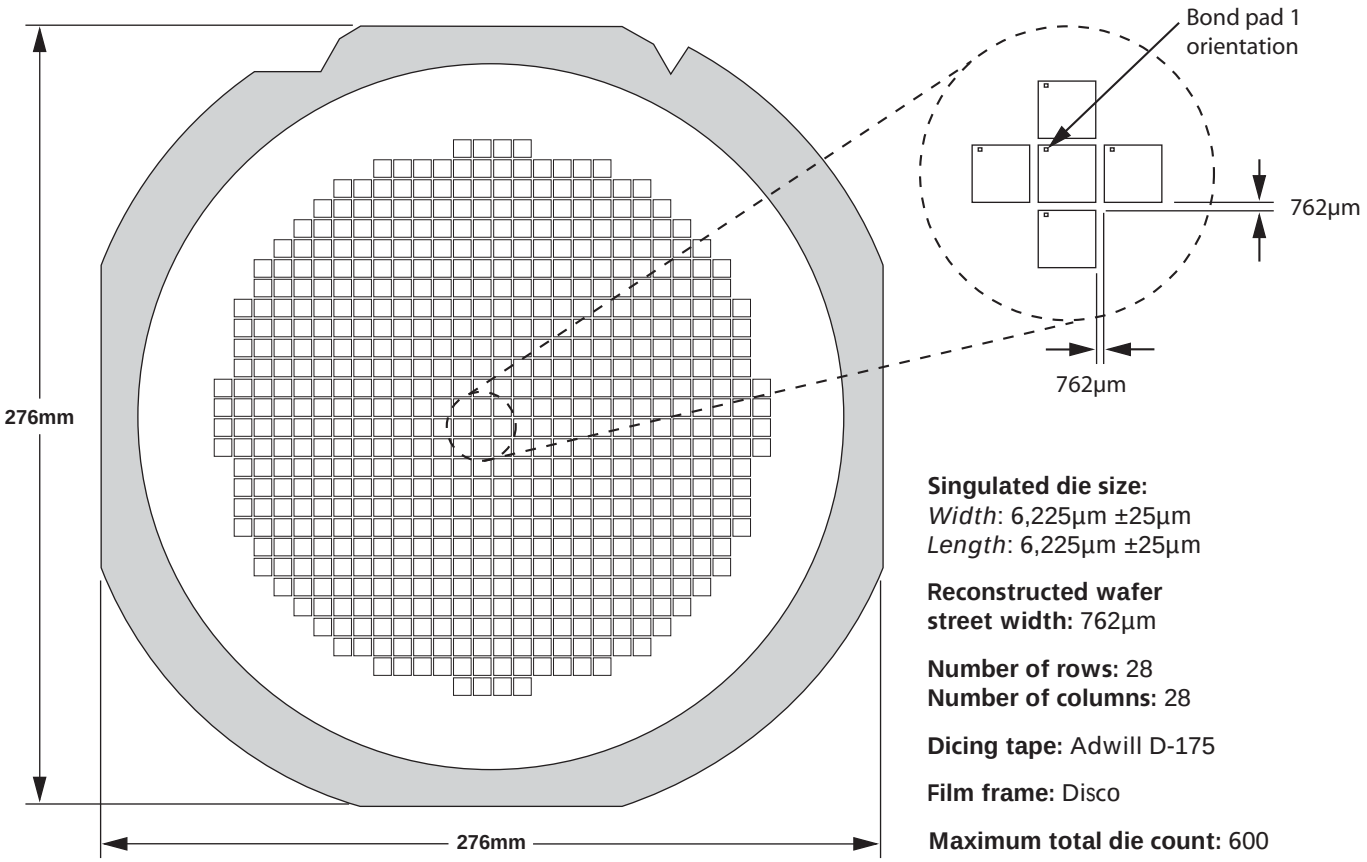


Physical Specifications

Table 3: Die Dimensions

Features	Dimensions
Wafer diameter	200mm (8in)
Die thickness	200µm ±12µm
Wafer thickness	750µm ±12µm
Singulated die size *Width:* *Length:*	 6,225µm ±25µm 6,225µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	466.56µm (18.369 mil)
Optical array *Optical center from die center:*	 X = –11.0µm, Y = 91.3µm
First clear pixel (col. 18, row 6) *From die center:* *From center of pad 1:*	 X = 1803.41µm, Y = 1457.47µm X = 4407.34µm, Y = –1441.61µm
Last clear pixel (col. 666, row 494) *From die center:* *From center of pad 1:*	 X = –1825.39µm, Y = –1275.32µm X = 778.44µm, Y = –4174.41µm

Figure 3: MT9V111 Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 6,225µm ±25µm
Length: 6,225µm ±25µm

Reconstructed wafer street width: 762µm

Number of rows: 28
Number of columns: 28

Dicing tape: Adwill D-175

Film frame: Disco

Maximum total die count: 600

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Revision History

Rev. K, Preliminary 10/07

- Corrected typographical error in footer

Rev. K, Preliminary 6/07

- Added DigitalClarity to trademarks
- Updated format to current standard

Rev. J, No Mark 5/05

- Fixed typos

Rev. H, Pub 03/05, No Mark 3/05

- Changed operating temperature range on page 1 from -20°C to +60°C to -30°C to +70°C
- Updated format
- Added singulated die size to Table 3 and Figure 3
- Removed wafer information

Rev. G, Pub 08/04, No Mark 8/04

- Revised title
- Added SOC information to **"Features"** section
- Revised **"Key Performance Parameters"** and **"General Description"**
- Revised bond pad names in Figure 1, **Table 1,** and **Table 2**
- Added center of die and optical center of die to **Figure 2**
- Removed note 2 from **Figure 2**
- Corrected x coordinate of **"Optical array Optical center from die center:"**

Rev. F, Pub. 04/04, No Mark 4/04

- Added Figure 3

Rev. E, Pub. 03/04, No Mark 3/04

- Added information to the "Features" and "Key Performance Parameters" paragraphs in page 1
- Changed second paragraph under "General Description"
- Modified 1 to show how to connect bond pad 22 (ADC_TEST)
- Changed bond pad 22 name to better describe its function (ADC_TEST)

Rev. D, Pub. 02/04, No Mark 2/04

- Changed YCrCb to YCbCr
- Changed Supply Voltage: 2.8V ±0.3V to Supply Voltage: 2.8V ±0.25V

Rev. C, Pub. 02/04, No Mark 2/04

- Added **"Key Performance Parameters"**
- Added Figure 1
- Modified **"Features"** and **"Bonding Instructions"**
- Changed data sheet designation to No Mark

Rev. B, Pub. 11/03, Preliminary 11/03

- Updated part numbers

Rev. A, Pub. 11/03, Preliminary 11/03

- Initial release