1/4-Inch SOC VGA CMOS Active-Pixel Digital Image Sensor

MT9V111 Automotive Addendum

For detailed specification information, see the MT9V111 data sheet on the Aptina Web site: www.aptina.com.

Introduction

This document supplements the Aptina® MT9V111 data sheet (Revision K). The information included in this addendum is specific to 1/4-inch SOC CMOS active-pixel automotive digital image sensor. The standard CMOS image sensor data sheet should be referenced for a complete description of this 1/4-inch VGA SOC image sensor. The specifications contained in this addendum supersede the specifications listed in the referenced CMOS image sensor data sheet.

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/4-inch (4:3)
Active imager size		3.584mm(H) x 2.688mm(V)
Active pixels		640H x 480V
Pixel size		5.6µm x 5.6µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate Master clock		12—13.5 Mp/s 24—27 MHz
Frame rate	VGA (640 x 480)	15 fps at 12 MHz (default), programmable up to 30 fps at 27 MHz
	CIF (352 x 288)	Programmable up to 60 fps
	QVGA (320 x 240)	Programmable up to 90 fps
ADC resolution		10-bit, on-chip
Responsivity		1.9 V/lux-sec (550nm)
Pixel dynamic range		60dB
SNR_{MAX}		45dB
Supply voltage		2.8 ±0.25V
Power consumption		<80mW at 2.8V, 15 fps at 12 MHz
Operating temperature		-40°C to +85°C
Packaging		52-Ball IBGA, wafer or die

Applications

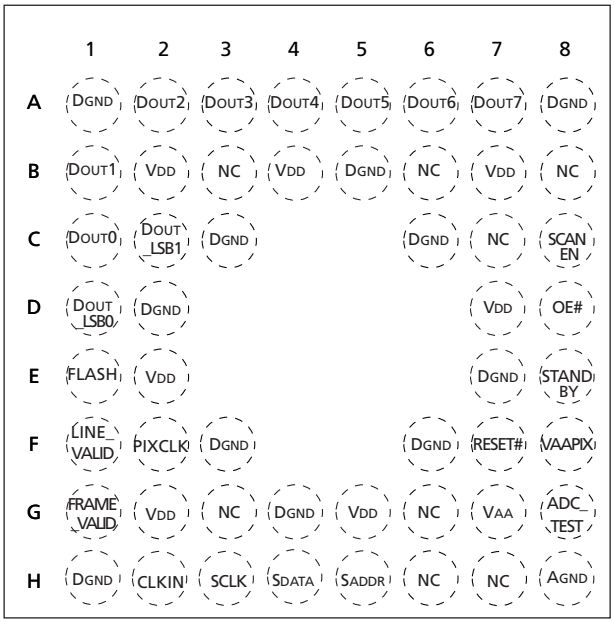
- Automotive
- Security cameras
- Industrial

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V111IA7ATC	IBGA package (Pb-free)
MT9V111D00ATC K82AC1	Bare die
MT9V111I99STCD ES	Demo kit
MT9V111I99STCH ES	Headboard

Figure 1: Ball Assignment



Top View
(Ball Down)

Electrical Specifications

Table 3: DC Electrical Characteristics
$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input high voltage	V_{IH}		V_{DD} –0.25	–	V_{DD} +0.25	V
Input low voltage	V_{IL}		–0.3	–	0.8	V
Input leakage current	I_{IN}	No pull-up resistor; $V_{IN} = V_{DD}$ or D_{GND}	–5	–	5	µA
Output high voltage	V_{OH}		V_{DD} –0.2	–	–	V
Output low voltage	V_{OL}		–	–	0.2	V
Output high current	I_{OH}		–	–	15	mA
Output low current	I_{OL}		–	–	20	mA
Tri-state output leakage current	I_{OZ}		–	–	5	µA
Analog operating supply current	I_{AA}	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz	–	20	25	mA
		Default settings, C_{LOAD} = 10pF CLKIN = 27 MHz	–	20	25	mA
Digital operating supply current	I_{DD}	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz	–	8	20	mA
		Default settings, C_{LOAD} = 10pF CLKIN = 27 MHz	–	15	20	mA
Analog standby supply current	I_{AA} Standby	STDBY = V_{DD}	–	2.5	5	µA
Digital standby supply current	I_{DD} Standby	STDBY = V_{DD}	–	2.5	5	µA

Notes:
1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 4: AC Electrical Characteristics

$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Notes
Input clock frequency		^{f}CLKIN		10	12	27	MHz	
Clock duty cycle			50:50	45	50	55	%	1
Input clock rise time		^{t}R		1	2	5	ns	
Input clock fall time		^{t}F		1	2	5	ns	
CLKIN to PIXCLK propagation delay	LOW-to-HIGH	$^{t}PLH_P$	C_{LOAD} = 10pF	6	12	14	ns	3
	HIGH-to-LOW	$^{t}PHL_P$		6	10	14	ns	
PIXCLK to DOUT[7:0] at 27 MHz	Setup time	^{t}DSETUP	C_{LOAD} = 10pF	11	18	–	ns	2
	Hold time	^{t}DHOLD		11	18	–	ns	
PIXCLK to FRAME_VALID and LINE_VALID propagation delay	LOW-to-HIGH	$^{t}PLH_{F,L}$	C_{LOAD} = 10pF	4	9.0	13	ns	
	HIGH-to-LOW	$^{t}PHL_{F,L}$		4	7.5	13	ns	
Output rise time		$^{t}OUT_R$	C_{LOAD} = 10pF	5	7.0	15	ns	
Output fall time		$^{t}OUT_F$	C_{LOAD} = 10pF	5	9.0	15	ns	

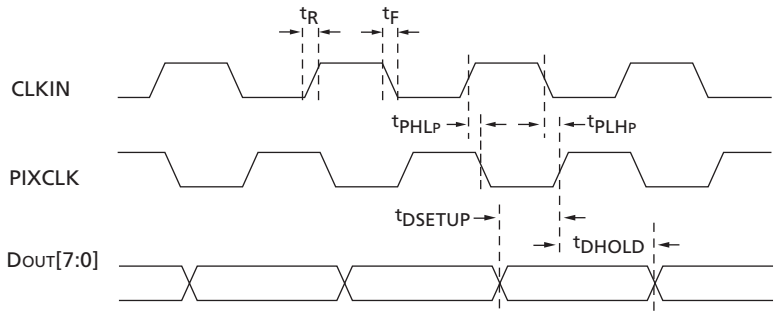
Notes:
1. For 30 fps operation with a 27 MHz clock, the user must have a precise duty cycle equal to 50 percent. With a slower frame rate and a slower clock, the clock duty cycle can be relaxed.
2. Typical is 1/2 of CLKIN period.
3. PIXCLK can be programmed to be inverted or non-inverted.

Propagation Delays

Propagation Delays for PIXCLK and Data Out Signals

The output PIXCLK delay, relative to the master clock (CLKIN), is typically 10–12ns. Note that the data outputs change on the rising edge of the master clock (CLKIN), as shown in in Figure 2. PIXCLK by default is inverted from CLKIN but can be programmed to be non-inverted.

Figure 2: Propagation Delays for PIXCLK and Data Out Signals

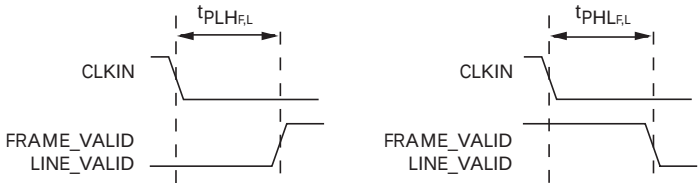


Note: Default condition of the IPA register R0x08[9] = 0.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same clock edge as the data output. The LINE_VALID goes HIGH on the same falling master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock falling edge as the end of the output of the last valid pixel's data. The default timing of PIXCLK with respect to LINE_VALID and FRAME_VALID is shown in Figure 3.

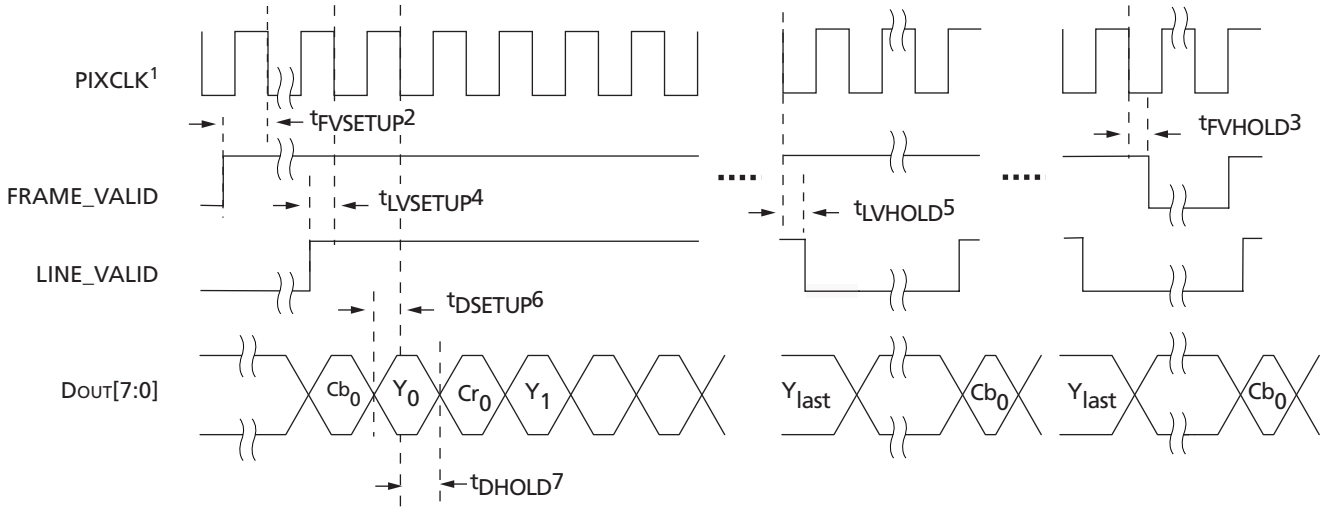
Figure 3: Propagation Delays for FRAME_VALID and LINE_VALID Signals



Output Data Timing

As shown in Figure 4, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to 6 pixel clocks after the last LINE_VALID goes LOW.

Figure 4: Data Output Timing Diagram

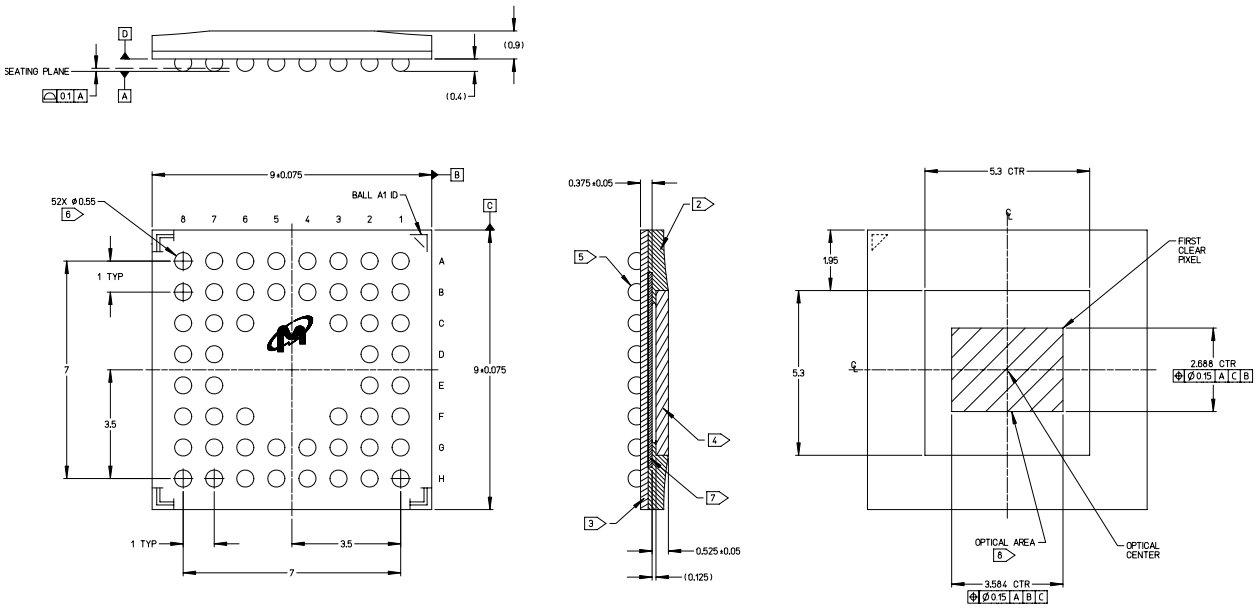


Notes:
1. PIXCLK = 27 MHz (MAX).
2. ^{t}FVSETUP = setup time for FRAME_VALID before falling edge of PIXCLK = 18ns.
3. ^{t}FVHOLD = hold time for FRAME_VALID after falling edge of PIXCLK = 18ns.
4. ^{t}LVSETUP = setup time for LINE_VALID before falling edge of PIXCLK = 18ns.
5. ^{t}LVHOLD = hold time for LINE_VALID after falling edge of PIXCLK = 18ns.
6. ^{t}DSETUP = setup time for DOUT before falling edge of PIXCLK = 18ns.
7. ^{t}DHOLD = hold time for DOUT after falling edge of PIXCLK = 18ns.
   Frame start: FF00 00A0.
   Line start: FF00 0080.
   Line end: FF00 0090.
   Frame end: FF00 00B0.
8. Drawing shown has R0x08[9] = 1.
9. Drawing not to scale.

Package Dimensions

Note: All dimensions in millimeters.

Figure 5: 52-Ball IBGA (Pb-Free)



Revision History

Rev. F 6/17/10

- Updated to Aptina template
- Updated to non-confidential
- Updated Table 2 on page 1
- Deleted Figure 5 (renumbered Fig 6 to Fig 5)

Rev. E, Production. 5/6/2008

- Added Pb-free part number to Table 2, “Available Part Numbers,” on page 1
- Updated to Aptina template
- Added Figure 5: “52-Ball IBGA (Pb-Free),” on page 6

Rev. D, Preliminary. 3/5/2007

- Updated Table 4 on page 3, changed note 2
- Updated Figure 2 on page 4 (setup and hold referenced to rising edge of CLKIN)
- Added note 8 to Figure 4 on page 5

Rev. C, Preliminary 1/07

- Updated Table 1 on page 1, Table 3 on page 2, and Table 4 on page 3
- Updated Figure 2 on page 4, Figure 3 on page 4, and Figure 4 on page 5

Rev. B, Preliminary 1/06

- Added complete part numbers

Rev. A, Preliminary 11/05

- Initial release

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