1/6-Inch SOC VGA CMOS Digital Image Sensor

MT9V112I2ASTC

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, low cost, progressive scan CMOS image sensor
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing:
  - Color recovery and correction
  - Sharpening
  - Gamma
  - Lens shading correction,
  - On-the-fly defect correction
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Automatic Features:
  - Auto exposure (AE)
  - Auto white balance (AWB)
  - Auto black reference (ABR)
  - Auto flicker avoidance
  - Auto color saturation
  - Auto defect identification and correction
- Fully automatic Xenon and LED-type flash support, fast exposure adaptation
- Multiple parameter contexts, easy/fast mode switching
- Camera control sequencer automates:
  - Snapshots
  - Snapshots with flash
  - Video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats

Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

Table 1: Key Performance Parameters

Parameter		typical Value
Optical Format		1/6-inch (4:3)
Active Imager Size		2.30mm(H) x 1.73mm(V) 2.88mm Diagonal
Active Pixels		640H x 480V
Pixel Size		3.6µm x 3.6µm
Color Filter Array		RGB Bayer Pattern
Shutter type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		12 MPS–13.5 MPS/ 24 MHz–27 MHz
Frame Rate (VGA 640H x 480V)		30 fps at 27 MHz
ADC Resolution		10-bit, on-chip
Responsivity		1.0V/lux-sec (550nm)
Dynamic Range		71dB
SNR_{MAX}		44dB[1]
Supply Voltage	I/O Digital	1.7V–3.1V (VDD nominal)
	Core Digital	1.7V–1.9V or 2.5V–3.1V (1.8V or 2.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power Consumption		76mW at 1.8V, 15 fps
Operating temperature		–30°C to +70°C
Packaging		36-Ball ICSP, wafer or die

Note:1.Measured at 1.0 lux*sec and 100% stauration

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V112I2ASTC	36-Ball iCSP (standard)
MT9V112I9ASTC	36-Ball iCSP (lead-free)

Table of Contents

List of Figures

List of Tables

General Description

The Aptina MT9V112 is a VGA-format, single-chip camera CMOS active-pixel digital image sensor. this device combines the MT9V012 image sensor core with fourth-generation digital image flow processor technology from Aptina Imaging. It captures high-quality color images at VGA resolution.

The VGA CMOS image sensor features Aptina breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9V112 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance, and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes.

The MT9V112 can be programmed to output progressive-scan images up to 30 frames per second (fps). The image data can be output in any one of six 8-bit formats:

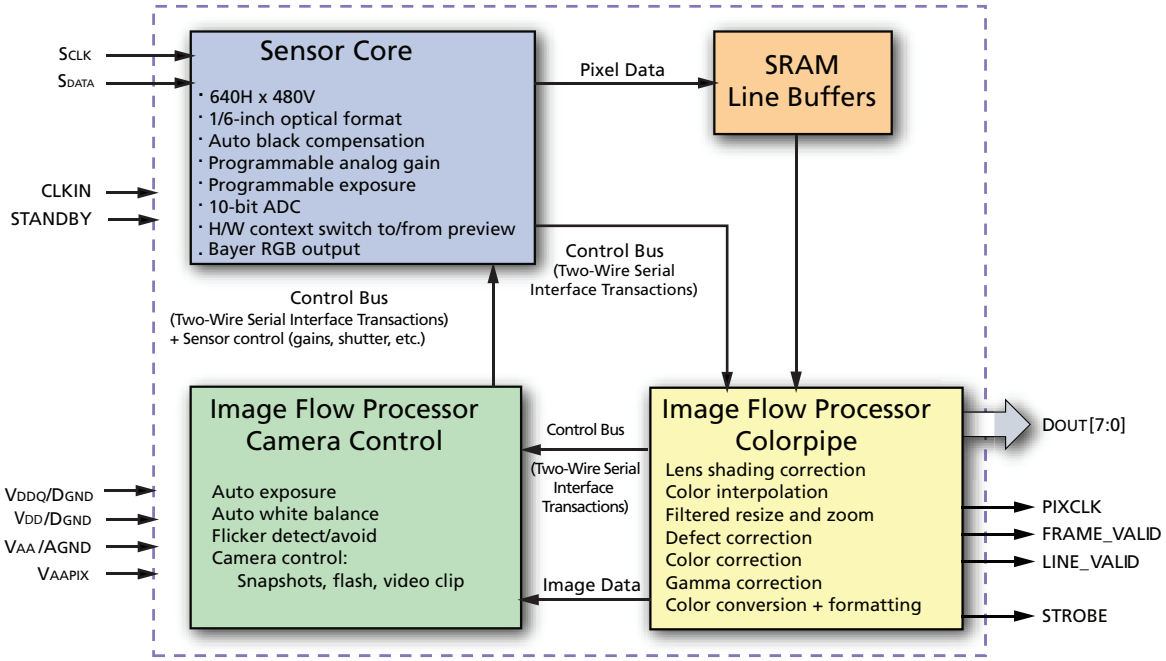
- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated balls, along with a pixel clock that is synchronous with valid data.

Functional Overview

The MT9V112 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed via a parallel 8-bit DOUT port, shown in *Figure 1, Functional Block Diagram, on page 6*. The output pixel clock is used to latch data, while FRAME_VALID and LINE_VALID signals indicate the active video. The MT9V112 internal registers are configured using a two-wire serial interface.

Figure 1: Functional Block Diagram



The device can be put in a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry in STANDBY mode also can be achieved via two-wire serial interface register writes.

The MT9V112 accepts input clocks up to 27 MHz, delivering up to 30 fps for VGA resolution images.

Internal Architecture

Internally, the MT9V112 consists of a sensor core and an image flow processor. The IFP is divided in two sections: the colorpipe (CP), and the camera controller .

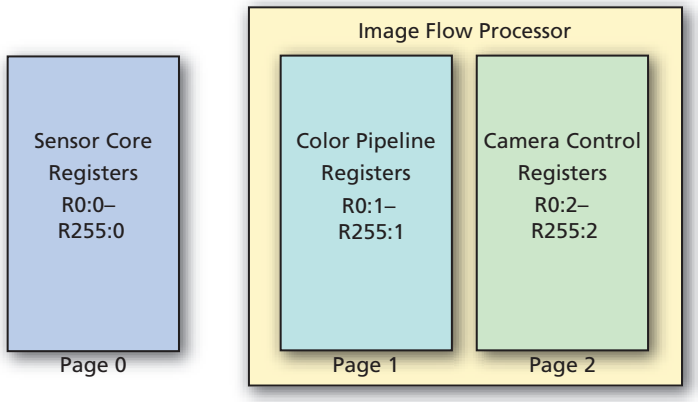
The sensor core captures raw Bayer-encoded images that are then input to the IFP.

The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes.

Register Overview

The sensor core, CP, and CC registers are grouped in three separate address spaces, shown in *Figure 2, Internal Registers Grouping, on page 7*.

Figure 2: Internal Registers Grouping



Notes:
Internal registers are grouped in three address spaces. Program R240 selects the desired address space.

The register notation is defined in the section below. When accessing internal registers via the two-wire serial interface, select the desired address space by programming the R240 register.

The sensor registers are summarized in Table 12, “Sensor Registers – Address Page 0,” on page 70. The colorpipe registers are summarized in Table 8, “Colorpipe Registers – Address Page 1,” on page 20. The camera control registers are summarized in Table 9, “Camera Control Registers – Address Page 2,” on page 23.

Register Notation

The following register address notations are used:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register in sensor page (page 0). Used to uniquely specify a register.
- R<decimal address>
  Example: R240—Page address register. Used when the register address is global in all three pages or when by context the address page is understood.
- 0x<2 digit hex address>
  Example: 0xF0—Page address register. Used when the register address is global in all three pages, or when by context the address page is understood.
- 0x<3 digit hex address>
  Example: 0x105— Page 1, Aperture Correction register (0x05). Same as 0x<2 digit hex address> notation; leading digit signifies page number.

When accessing internal registers via the two-wire serial interface, select the desired address space by programming the R240 register.

The MT9V112 accelerates mode-switching with hardware-assisted context switching, and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9V112 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

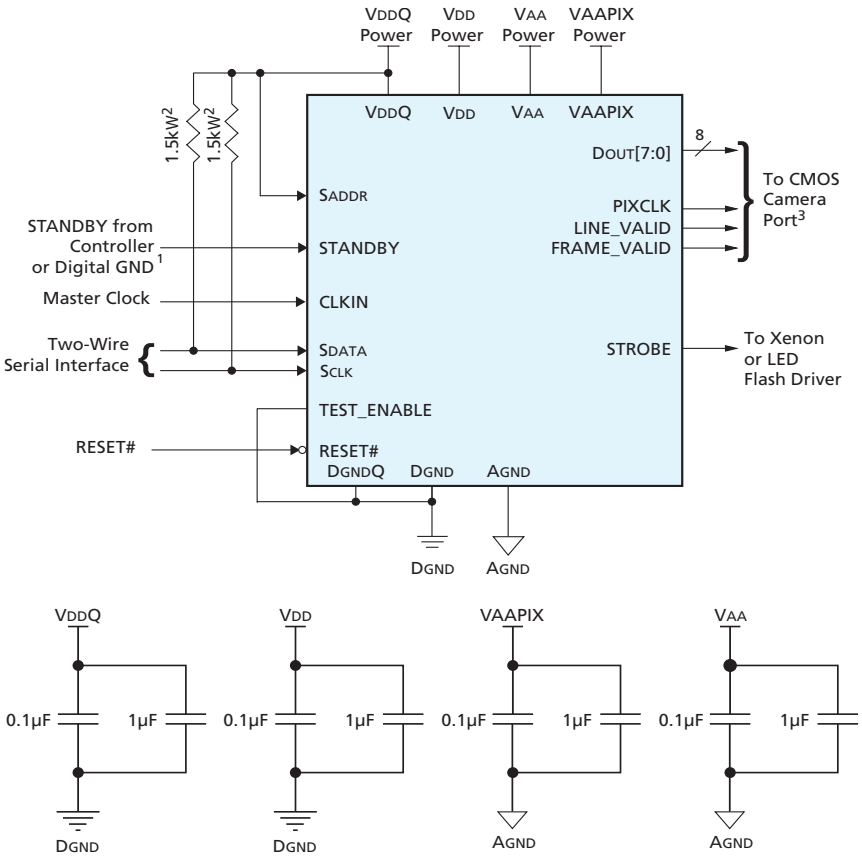
- Standard FRAME_VALID/LINE_VALID video interface with gated pixel clocks
- ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocking

Typical Connections

Figure 3, Typical Configuration (connection), on page 8 shows typical MT9V112 device connections. For low-noise operation, the MT9V112 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

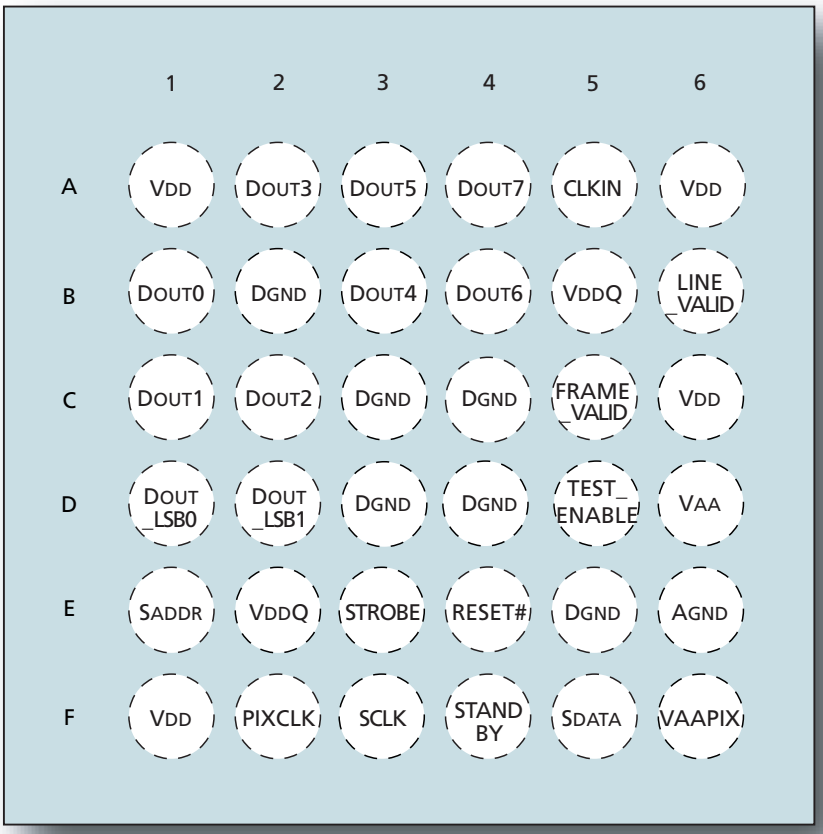
The MT9V112 also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGND) power domains that can be at different voltages.

Figure 3: Typical Configuration (connection)



Notes:
1. MT9V112 STANDBY can be connected to customer's ASIC controller directly or to Digital GND, depending on the capability of the controller.
2. A 1.5KΩ resistor value is recommended, but may be greater for slower two-wire speed.
3. The bus connecting the sensor to the camera port is called the pixel bus.

Figure 4: 36-Ball ICSP Assignment



Top View
(Ball Down)

Table 3: Ball Descriptions

Ball Assignment	Name	Type	Description
A5	CLKIN	Input	Master clock in sensor.
E4	RESET#	Input	Active LOW: RESET[1].
E1	SADDR	Input	Two-Wire Serial Interface Device ID selection 1:0xBA, 0:0x90.
D5	TEST_ENABLE	Input	Tie to DGND for normal operation. (Manufacturing use only.)
F3	SCLK	Input	Two-Wire Serial Interface Clock.
F4	STANDBY	Input	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
F5	SDATA	Input/Output	Two-Wire Serial Interface Data I/O.
B1, C1, C2, A2, B3, A3, B4, A4	DOUT[7:0][2]	Output	Pixel Data Output bit 0, DOUT[7] (most significant bit (MSB)), DOUT[0] (least significant bit (LSB)).
D1	DOUT_LSB0	Output	Sensor bypass mode output 0—typically left unconnected for normal SOC operation.
D2	DOUT_LSB1	Output	Sensor bypass mode output 1—typically left unconnected for normal SOC operation.
C5	FRAME_VALID	Output	Active HIGH: FRAME_VALID; indicates active frame.
B6	LINE_VALID	Output	Active HIGH: LINE_VALID, DATA_VALID; indicates active pixel.
F2	PIXCLK	Output	Pixel clock output.
E3	STROBE	Output	Active HIGH: STROBE (Xenon) or turn on (LED) flash.
E6	AGND	Supply	Analog ground.
B2, C3, C4, D3, D4, E5	DGND	Supply	Core digital ground.
D6	VAA	Supply	Analog power: 2.5V–3.1V (2.8V nominal).
F6	VAAPIX	Supply	Pixel array analog power supply: 2.5V–3.1V (2.8V nominal).
A1, A6, C6, F1	VDD	Supply	Core digital power: 1.7V–1.9V or 2.5V–3.1V (1.8V or 2.8V nominal).
B5, E2	VDDQ	Supply	I/O digital power: 1.7V–3.1V (VDD nominal).

Note: 1. A proper reset sequence requires an active CLKIN signal after the RESET# signal has been driven low. For more details about the reset sequence refer to the MT9V112 Developer Guide.

DOUT[7:0] Output Data Ordering

Data ordering formats are defined in the following tables.

Table 4: Data Ordering in YCbCr Mode

Mode	Byte	Byte + 1	Byte +	Byte + 3
Default	Cbi	Yi	Cri	Yi+1
Swap CrCb	Cri	Yi	Cbi	Yi+1
SwapYC	Yi	Cbi	Yi+1	Cri
Swap CrCb, SwapYC	Yi	Cri	Yi+1	Cbi

Table 5: Output Data Ordering in Processed Bayer Mode

Mode	Line	Byte	Byte + 1	Byte + 2	Byte + 3
Default	First	Gi	Ri+1	Gi+2	Ri+3
	Second	Bi	Gi+1	Bi+2	Gi+3
Flip Bayer Col	First	Ri	Gi+1	Ri+2	Gi+3
	Second	Gi	Bi+1	Gi+2	Bi+3
Flip Bayer Row	First	Bi	Gi+1	Bi+2	Gi+3
	Second	Gi	Ri+1	Gi+2	Ri+3
Flip Bayer Col, Flip Bayer Row	First	Gi	Bi+1	Gi+2	Bi+3
	Second	Ri	Gi+1	Ri+2	Gi+3

Table 6: Output Data Ordering in RGB Mode

Mode (Swap disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
RGB444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGBx444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Table 7: Output Data Ordering in (8 + 2) Bypass Mode

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
8 + 2 bypass	First	B9	B8	B7	B6	B5	B4	B3	B2
	Second	0	0	0	0	0	0	B1	B0

Modes and Timing

This section provides .an overview of typical usage modes for the MT9V112.

Contexts

The MT9V112 supports hardware-accelerated context switching. A number of parameters have two copies of their setup registers; this allows two “contexts” to be loaded at any given time. These are referred to as context A and context B. Context selection for any single parameter is determined by the global context control register (GCCR, see R200:2).

There are copies of this register in each address page. A write to any one of them has the identical effect. However, a read from address page 0 only returns the subset bits of R200 that are specific to the sensor core.

Contexts are generically named because they can be utilized for a variety of purposes. One typical usage model is to define context A as viewfinder or preview mode and context B as snapshot mode. The device defaults are configured with this in mind. this mechanism enables the user to have settings for viewfinder and snapshot modes loaded at the same time, and then switch between them with a single write to a register (e.g., R200:2).

Viewfinder/Preview and Full-Resolution/Snapshot Modes

No context switching is necessary in the sensor core because this is a single ADC device. Context switching occurs in the colorpipe stage.

Preview Mode

QVGA (320 x 240) images are generated at up to 30 fps. The reduced-size images are generated by a scaling down operation. The sensor always outputs a VGA size image to the colorpipe in both context A and context B.

Snapshot Mode

VGA (640 x 480) images are generated at up to 30 fps. this is typically selected by setting R200:n[10] = 1 selecting resize/zoom context B.

Switching Modes

Typically, switching to snapshot mode is achieved by writing R200:2 = 0x9F0B. this restarts the sensor and sets most contexts to context B. Following this write, a read from R200:1 or R200:2 results in 0x1F0B being read.

The MSB is cleared automatically by the sensor. A read from R200:0 results in 0x000B, as only the lower 4 bits and the restart MSB are implemented in the sensor core.

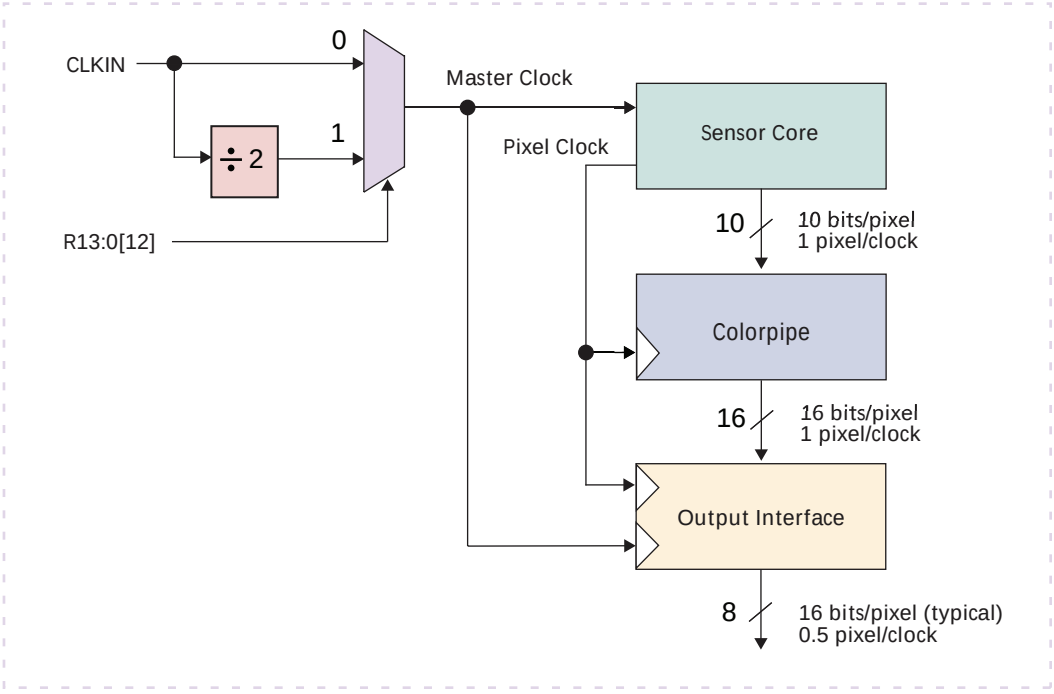
Clocks

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions—particularly resize. The relationship of the primary clocks are depicted in Figure 5 on page 13.

The image flow pipeline typically generates up to 16-bits per pixel—for example, YCbCr or RGB565—but has only an 8-bit port through which to communicate this pixel data. There is no phase-locked loop (PLL), so the primary input clock (CLKIN) must be twice the fundamental pixel rate (defined by the sensor pixel clock).

To generate VGA images at 30 fps, the sensor core requires a clock in the 24 MHz–27 MHz range. The device defaults assume a 24 MHz clock, and minimum clock frequency is 2 MHz.

Figure 5: Primary Sensor Core Clock Relationships



Note: If R13:0[12] = 0 then the Master Clock will be equal to the frequency of CLKIN.
If R13:0[12] = 1 then the Master Clock will be 1/2 of the frequency of CLKIN.
Frequency of Master Clock = 2*Frequency of Pixel Clock

Tuning Frame Rates

Actual frame rates can be tuned by adjusting various sensor parameters. The sensor registers are in address page 0, some of which are shown in Table 8.

Table 8: Register Address Functions

Register	Function
R0x04:0	Column width, typically 640 in the MT9V112
R0x03:0	Row width, typically 480 in the MT9V112
R0x07:0, R0x05:0	Horizontal blanking, default is 203 (units of sensor pixel clocks)
R0x08:0, R0x06:0	Vertical blanking, default is 11 (rows including black rows)

Default Blanking Calculations

the MT9V112 default blanking calculations are shown in Table 9.

Table 9: Blanking Parameter Calculations

Parameter	Calculation
PC_PERIOD Sensor Pixel Clock Period	(2/24)µs = 0.083µs
A: Active Data time (per line): R0 x 04:0 + 8 (border) * PC_PERIOD	648 x (2/24) = 54µs
Q: Horizontal Blanking: [R0 x 05:0 | R0 x 07:0] * PC_PERIOD	154 x (2/24) = 12.83µs
Row time = Q + A	66.83µs
P: Frame Start / End Blanking: 6 * PC_PERIOD	6 x (2/24) = 0.5µs
V: Vertical Blanking: [R0 x 06:0 | R0 x 08:0] * (Q + A) + (Q - 2 * P)	(11 x 66.83) + (12.83 - 1.0) = 747µs
F: Total Frame time: (R0 x 03:0 + [R0 x 06:0 | R00 x 08:0]) * (Q + A)	(488 + 11) x 66.83µs = 33349.83 ?s ≥ 30 fps

In the MT9V112, the sensor core adds four border pixels all the way around the image, taking the active image size to 648 x 488 in full power mode. this is achieved through the default settings:

- Oversize and show border bits are set by default
- Oversize and show border bits are not context switchable, and therefore, their location is only in read mode context B.

User Blanking Calculations

When calculating blanking for different clock rates, minimum values for horizontal blanking and vertical blanking must be taken into account. Table 10 shows minimum values for each register.

.

Table 10: User Blanking Minimum Values

Parameter	Minimum
Horizontal Blanking	132 (sensor pixel clocks)
Vertical Blanking	6 + Reg0x22:0[2:0] rows

Output Timing

Figure 6: Vertical Timing

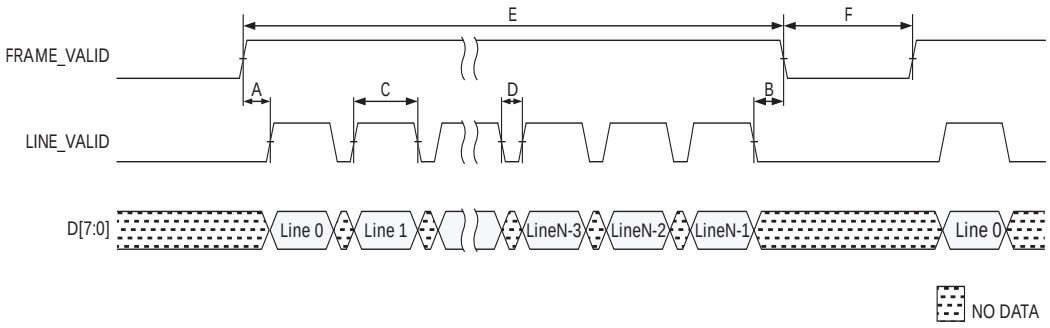
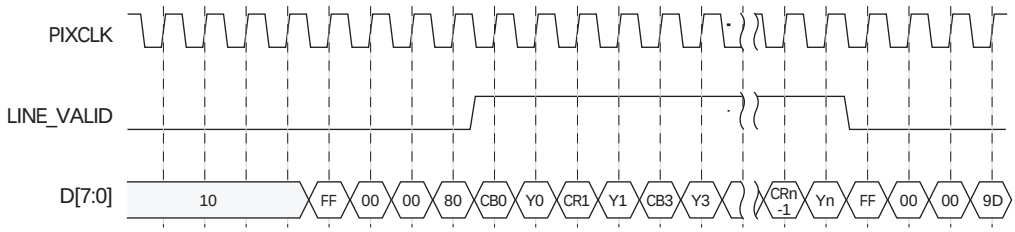


Figure 7: Horizontal Timing



Typical Resolutions, Modes, and Timing

The parameters listed in Table 11 are illustrated in a waveform diagram, *Figure 6, Vertical Timing, on page 15*. *Figure 20, AC Electrical Characteristics, on page 23* provides values for these parameters in some common resolutions and operating modes.

Table 11: Blanking Definitions

Designation	Definition
(A)	FRAME_VALID (rising edge) to LINE_VALID (rising edge) delay
(B)	LINE_VALID (falling edge) to FRAME_VALID (falling edge) delay
(C)	LINE_VALID (HIGH/valid) time
(D)	LINE_VALID (LOW/horizontal blanking) time
(E)	FRAME_VALID (HIGH/valid) time
(F)	FRAME_VALID (LOW/vertical blanking) time

RESET, Clocks, and STANDBY

RESET

Power-up reset is asserted/de-asserted on RESET#. It is active LOW. In this reset state, all control registers have the default values.

Soft reset is asserted/de-asserted by the two-wire serial interface program. In soft-reset mode, the two-wire serial interface and register ring bus are still running. All control registers are reset using default values. See R13:0.

Clocks

The MT9V112 has two primary clocks; a master clock coming from the CLKIN signal, and a pixel clock via a clock-gated operation running at half frequency of the master clock. All device clocks are turned off in power-down mode. When the MT9V112 operates in sensor stand-alone mode, the image flow pipeline clocks can be shut off to conserve power. See R13:0.

When the MT9V112 is operated with the MT9M111 in a dual-camera application, the MT9V112 employs a divide-by-two clock option, allowing a 54 MHz input to the master clock. For more information about this feature, see the R13:0 register description on page 74 in Table 13.

STANDBY

STANDBY is a multifunctional signal that controls power-down, device addressing, and tri-state functions. Table 12 shows how STANDBY affects the output signal state. When the sensor is in standby mode (hard or soft) CLKIN must be active (toggling) for commands and data to be received by the two-wire serial interface bus.

Hard standby is asserted/de-asserted on STANDBY. It is active HIGH. In this hard standby state, all internal clocks are turned off and the analog block is in STANDBY mode to save power consumption. The signal state is High-Z when R13:0[4] = 0 and R13:0[6] = 0.

Two-wire interface ID addressing is based on the result of SADDR XOR R13:0[10]. (The R13:0[10] default is "0".) the R13:0[10] bit is not writable when STANDBY is asserted "1."

Soft standby is asserted/de-asserted by a two-wire serial interface to R13:0[2]. In soft standby, all internal clocks are turned off, the analog block is in standby mode, but the signal state is not affected. Following the assertion of either hard or soft STANDBY, the analog circuitry completes reading the current row and then enters the standby state. It is necessary to keep clocking the sensor for an entire row time to ensure proper entry into the standby state.

Table 12: STANDBY Effect on the Output State

Output Disable R13:0[4]	Drive Signal R13:0[6]	STANDBY	Output State
0	0	0	Driven
0	0	1	High-Z
0	1	x	Driven
1	x	x	High-Z

Electrical Specifications

Operating Conditions

Table 13: Operating Conditions

Symbol	Definition	MIN	Typical	MAX	Units
V_{DDQ}	I/O Digital Voltage	1.7	V_{DD}	3.1	V
V_{DD}	Core Digital Voltage (condition 1)	2.5	2.8	3.1	V
	Core Digital Voltage (condition 2)	1.7	1.8	1.9	V
V_{AA}	Analog Voltage	2.5	2.8	3.1	V
V_{AAPIX}	Pixel Supply Voltage	2.5	2.8	3.1	V
T_C	Operating temperature (At Junction)	–30	30	70	°C

Note: Note: Recommended die operating temperature range is from Ta = –20°C to 40°C. The sensor image quality may degrade above 40°C.

Table 14: Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating		Unit
			MIN	MAX	
V_{DD}	Digital power (2.8V)		-0.3	4.0	V
V_{DDQ}	I/O power		-0.3	4.0	V
V_{AA}	Analog power (2.8V)		-0.3	4.0	V
VAAPIX	Pixel array power		-0.3	4.0	V
V_{IN}	DC Input Voltage		-0.3	V_{DDQ}+0.3	V
V_{OUT}	DC Output Voltage		-0.3	V_{DDQ}+0.3	V
T_{STG}[1]	Storage temperature		-40	85	°C
I_{LZ}	High Impedance Output Leakage Current	V_{IN} = V_{DDQ} or DGND	-10	10	µA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Table 15: DC Electrical Characteristics (Condition 1)

V_{DD} = 2.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
V_{IH}	Voltage Input High	2.5	2.8	3.1	V
V_{IL}	Voltage Input Low	–0.3	0	0.3	V
I_{IL}	Current Input leakage Low	–5		5	µA
I_{IH}	Current Input leakage High	–5		5	µA
V_{OH}	Voltage Output High	V_{DDQ}-0.3		V_{DDQ}	V
V_{OL}	Voltage Output Low	0	0	0.3	V
I_{OH}	Current Output High	12		15	mA
I_{OL}	Current Output Low	14		17	mA

Table 16: DC Electrical Characteristics (Condition 2)

V_{DD} = 1.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 1.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
V_{IH}	Voltage Input High	1.7	1.8	1.9	V
V_{IL}	Voltage Input Low	–0.3	0	0.3	V
I_{IL}	Current Input leakage Low	–5		5	µA
I_{IH}	Current Input leakage High	–5		5	µA
V_{OH}	Voltage Output High	V_{DDQ}-0.3		V_{DDQ}	V
V_{OL}	Voltage Output Low	0	0	0.3	V
I_{OH}	Current Output High	8		10	mA
I_{OL}	Current Output Low	10		12	mA

I/O Parameters

Table 17: I/O Parameters

V_{AA} = 2.8V, V_{AAPIX} = 2.8V, fCLKIN = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Signal	Parameter	Definitions	Condition	Min	Typical	Max	Units
All Outputs		Load capacitance				30	pF
		Output signal slew	VDD = VDDQ = 2.8V, 30pF load	0.25		1.25	V/ns
			VDD = VDDQ = 1.8V, 30pF load	0.1		0.6	V/ns
All Inputs	Signal CAP	Input signal capacitance				5	pF
CLKIN	freq	Master clock frequency	Absolute minimum	2			MHz
			VGA at 30 fps	24		27	MHz

Note: I/O pins exhibit the characteristics of either the input signals or the output signals as defined in this table depending on the mode of the pin.

Power Consumption

Table 18: Operating Power Consumption

V_{AA} = 2.8V, V_{AAPIX} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30 °C,Light Condition = 90 lux

Mode	fps	Definition	(V_{DD},V_{DDQ} = 2.8V)		(V_{DD},V_{DDQ} = 1.8V)		Units
			TYP	MAX	TYP	MAX	
VGA	30 fps	Operating I_{DD}	15	25	9	16	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	11	30	5	17	mA
		Operating I_{AAPIX}	1	1	1	1	mA
VGA	30 fps	Total power consumption w/o I_{DDQ}	98	136	72	94	mW
VGA	15 fps	Operating I_{DD}	15	20	9	12	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	10	19	5	11	mA
		Operating I_{AAPIX}	1	1	1	1	mA
VGA	15 fps	Total power consumption w/o I_{DDQ}	98	122	72	88	mW
QVGA	30 fps	Operating I_{DD}	15	25	9	15	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	9	14	4	8	mA
		Operating I_{AAPIX}	1	2	1	2	mA
QVGA	30 fps	Total power consumption w/o I_{DDQ}	98	136	72	94	mW
QVGA	15 fps	Operating I_{DD}	15	20	9	12	mA
		Operating I_{AA}	19	22	19	22	mA
		Operating I_{DDQ}	8	11	4	7	mA
		Operating I_{AAPIX}	1	1	1	1	mA
QVGA	15 fps	Total power consumption w/o I_{DDQ}	98	121	72	88	mW

STANDBY Power Consumption

Table 19: STANDBY Power Consumption

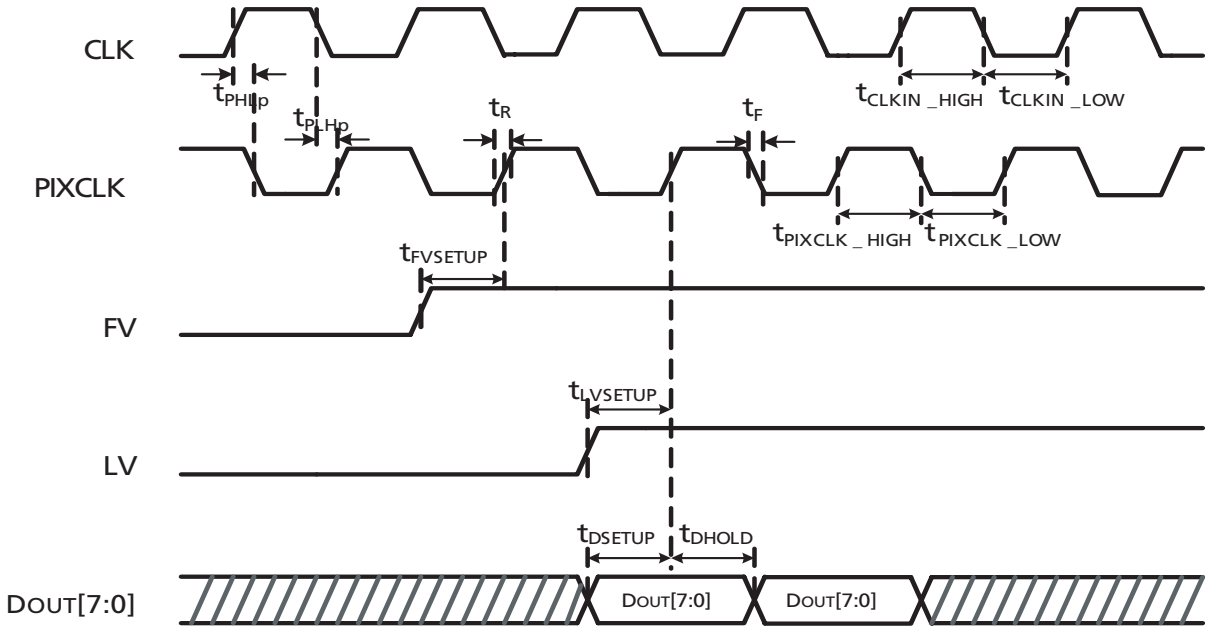
V_{AA} = 2.8V, V_{AAPIX} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30 °C

Definition	MAX (V_{DD},V_{DDQ} = 2.8V)	MAX (V_{DD},V_{DDQ} = 1.8V)	Units
Hard STANDBY I_{DD} (without clock)	1	1	µA
Hard STANDBY I_{DDQ} (without clock)	4	2	µA
Hard STANDBY I_{AA} (without clock)	1	1	µA
Hard STANDBY I_{AAPIX} (without clock)	1	1	µA
Total Power Consumption (without clock)	20	11	µW
Hard STANDBY I_{DD} (with clock)	821	487	µA
Hard STANDBY I_{DDQ} (with clock)	22	8	µA
Hard STANDBY I_{AA} (with clock)	1	1	µA
Hard STANDBY I_{AAPIX} (with clock)	1	1	µA
Total Power Consumption (with clock)	2366	897	µW

I/O Timing

By default, the MT9V112 launches pixel data, FRAME_VALID, and LINE_VALID synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FRAME_VALID, and LINE_VALID using the rising edge of PIXCLK. The timing diagram is shown in Figure 8. As an option, the polarity of the PIXCLK can be inverted from the default. this is achieved by programming R58:1[9] or R155:1[9] to "0."

Figure 8: AC Output Timing Diagram



AC Electrical Characteristics

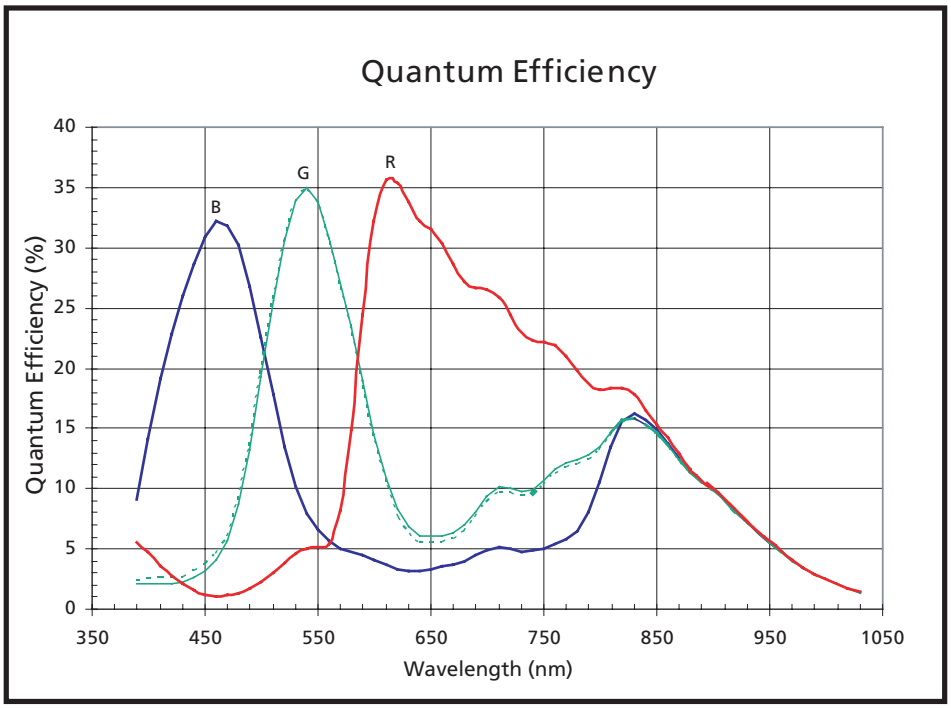
Table 20: AC Electrical Characteristics

V_{DD} = 2.8V, V_{AA} = 2.8V, V_{AAPIX} = 2.8V, V_{DDQ} = 2.8V, f_{CLKIN} = 27 MHz (50% duty cycle), Ta = 30°C, Light Condition = Dark

Symbol	Definition	MIN	Typical	MAX	Units
f_{CLKIN}	Input clock frequency		13.5	27	MHz
t_R	Pixel clock rise time		10		ns
t_F	Pixel clock fall time		10		ns
t_{PLHP}	CLKIN to PIXCLK propagation delay (L–H)		48		ns
t_{PHLP}	CLKIN to PIXCLK propagation delay (H–L)		48		ns
$t_{LVSETUP}$	Setup time for LINE_VALID before rising edge of PIXCLK		1/2 PIXCLK Period		ns
$t_{FVSETUP}$	Setup time for FRAME_VALID before rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{DSETUP}	Setup time for DOUT before rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{DHOLD}	Hold time for DOUT after rising edge of PIXCLK		1/2 PIXCLK Period		ns
t_{CLKIN_HIGH}	Master clock duty cycle (High time)	40	50	60	%
t_{CLKIN_LOW}	Master clock duty cycle (Low time)	40	50	60	%
t_{PIXCLK_HIGH}	Pixel clock duty cycle (High time)	40	50	60	%
t_{PIXCLK_LOW}	Pixel clock duty cycle (Low time)	40	50	60	%

Spectral Characteristics

Figure 9: Typical Spectral Characteristics



Appendix A

Serial Bus Description

Registers are written to and read from the MT9V112 through the two-wire serial interface bus. The sensor is a serial interface slave controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred in and out of the MT9V112 through the serial data (SDATA) line. The SDATA line is pulled up to VDDQ off-chip by a 1.5KΩ resistor. Either the slave or the master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- Start bit
- (No) Acknowledge bit
- 8-bit message
- Stop bit
- Slave device 8-bit address

SADDR and R13:0[10] are used to select between two different addresses in case of conflict with another device. If SADDR XOR R13:0[10] is LOW, the slave address is 0x90; if SADDR XOR R13:0[10] is HIGH, the slave address is 0xBA. See Table 21.

Table 21: Two-Wire Interface ID Switching

SADDR	R13:0[10]	Two-Wire Interface ID
0	0	0x90
0	1	0xBA
1	0	0xBA
1	1	0x90

Sequence

A typical read or write sequence begins with the master sending a start bit. After the start bit, the master sends the 8-bit slave device address. The last bit of the address determines if the request is a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master transfers the 8-bit register address for where a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data, eight bits at a time, with the slave sending an acknowledge bit after each eight bits.

The MT9V112 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. The master sends the write mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master clocks out the register data, eight

bits at a time, and sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xBA; the read address is 0xBB. This applies only when the SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver signals an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample

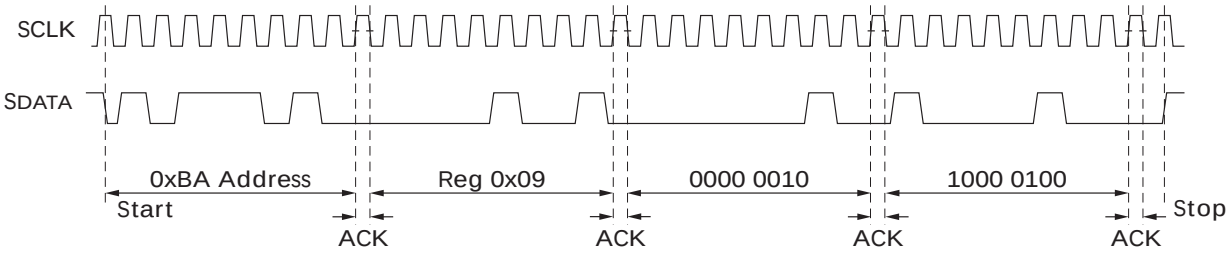
Write and read sequences (SADDR = 1).

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 10. A start bit sent by the master starts the sequence, followed by the write address. The image sensor sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit.

All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

Figure 10: Write Timing to R0x09:0—Value 0x0284

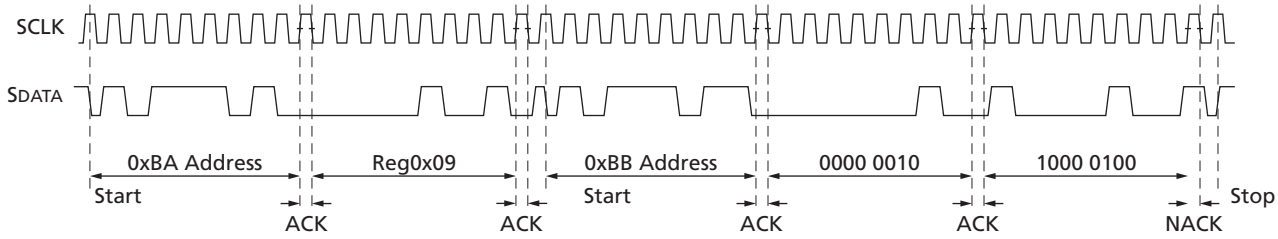


16-Bit Read Sequence

A typical read sequence is shown in Figure 11. The master writes the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to occur from the register. The master then clocks out the register data, 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer.

The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

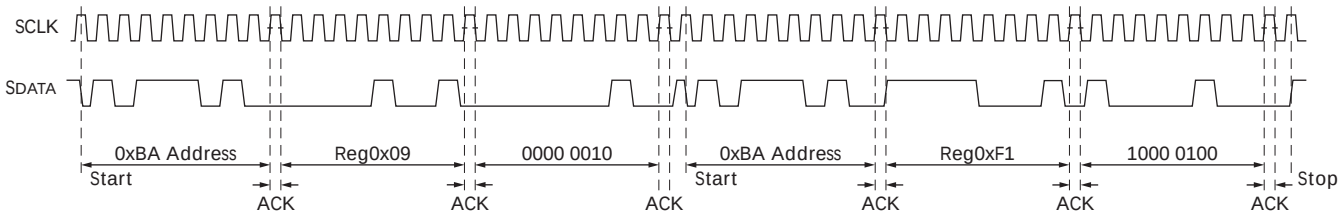
Figure 11: Read Timing from R0x09:0; Returned Value 0x0284



8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is started by writing the upper eight bits to the desired register, then writing the lower eight bits to the special register address (R0xF1:0). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. In Figure 12, a typical sequence for an 8-bit write is shown. The second byte is written to the special register (R0xF1:0).

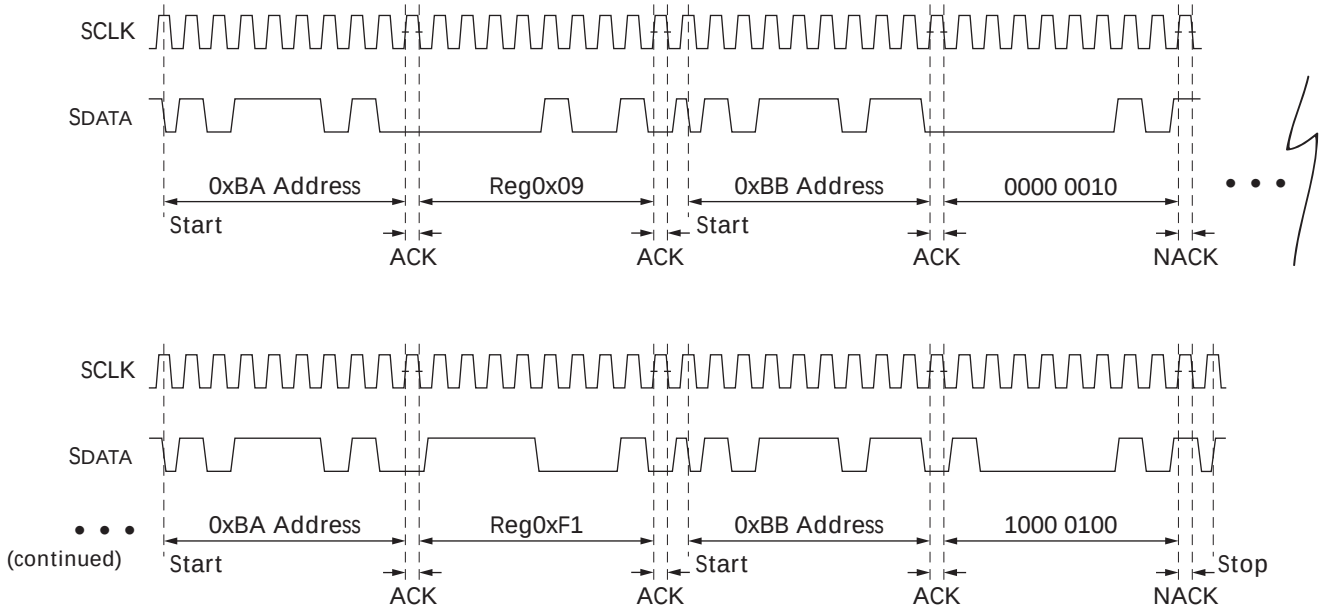
Figure 12: Write Timing to R0x09:0—Value 0x0284



8-Bit Read Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper eight bits are read from the desired register. By following this with a read from the special register (R0xF1:0), the lower eight bits are accessed (Figure 13). The master sets the no-acknowledge bits.

Figure 13: Read Timing from R0x09:0; Returned Value 0x0284



Two-wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified in the table below in master clock cycles.

Table 22: Two-wire Serial Bus Timing

V_{DD} = 2.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, $V_{DD}Q$ = 1.8V T_a = 55°C

Symbol	Definition	MIN	TYP	MAX	Units
f_{ic}	Two_Wire Serial Bus Input Clock Frequency			400	KHz
t_{ic}	Two-Wire Serial Bus Input Clock period	2500	–	–	ns
t_{icl}	Two-Wire Serial Bus Clock Low	1000	1250	1500	ns
t_{ich}	Two-Wire Serial Bus Clock High	1000	1250	1500	ns
t_{iss}	Setup time for start condition	600	–	–	ns
t_{ihs}	Hold time for start condition	600	–	–	ns
t_{isd}	Setup time for input data	600	–	–	ns
t_{ihd}	Hold time for input data	600	–	–	ns
t_{oaa}	Output data delay time	–	–	600	ns
t_{oda}	Output data hold time	600	–	–	ns
t_{isp}	Setup time of stop condition	600	–	–	ns
t_{ihp}	Hold time for stop condition	600	–	–	ns
C_{IN}	Input pin capacitance	–	3.5	–	pF
C_{LOAD}	SDATA max load capacitance	–	–	30	pF
RSD	SDATA pull-up resistor	–	1.5	–	KΩ

Note: T = one master clock cycle

Figure 14: Two-wire Serial Bus Signal Timing at the Pins of the Sensor

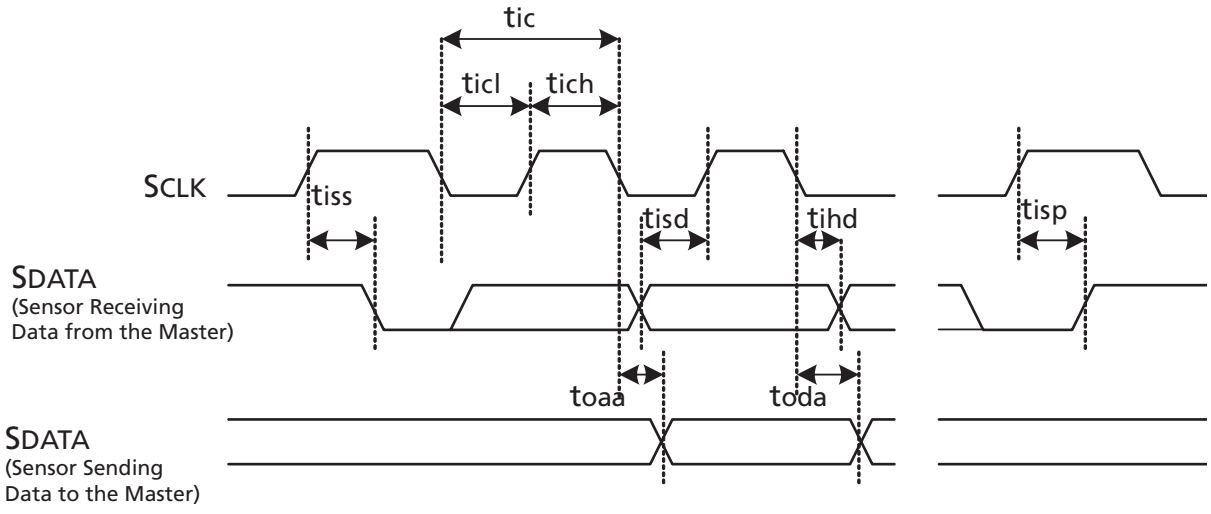
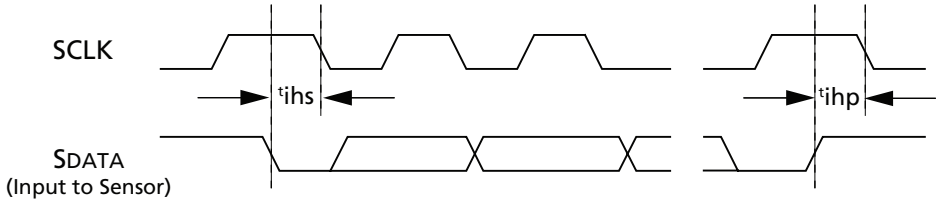
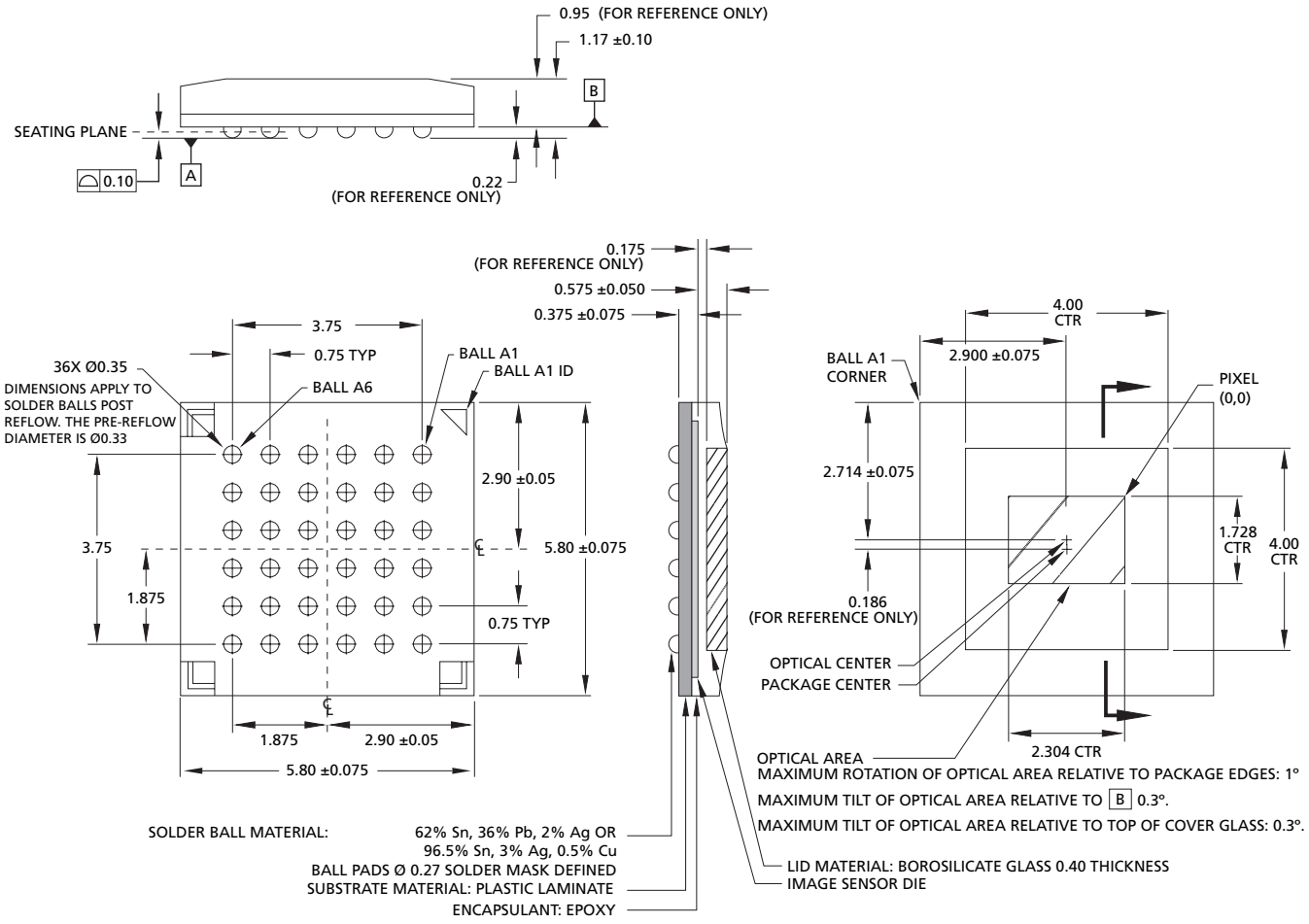


Figure 15: Two-wire Serial Bus Signal Timing at the Pins of the Sensor(2)



36-Ball ICSP Package

Figure 16: 36-Ball ICSP Package



Note: All dimensions in millimeters.

Revision History

Rev. M 5/4/11

- Updated trademarks
- Applied updated template

Rev. L 6/2/10

- Updated to non-confidential

Rev. K 5/5/2010

- Updated to Aptina template
- Transfered registers to a seperate document

Rev. J 5/30/2006

- Added note to Table 1 on page 1 and updated Figure 15 on page 30.

Rev. H 3/10/2006

- Updated Note 2 in Table 3 on page 10.

Rev. G 3/2/2006

- Updated Table 22 on page 29 for output delay time from 3T to 4T and hold time for output data from 4T to 3T.

Rev. F 2/2/2006

- Moved Value of Output Delay Time (3T) from Min column to Max column in Table 22 on page 29.
- Updated descriptions of SDATA in Table 14 on page 29.

Rev. E 1/19/2006

- Figure 5 on page 13 added more detail and Figure 7: Horizontal Timing on page 15 updated last data out value to 9D (was 90).
- Table 3 definition of RESET changed from async to sync, Table 13 R0x00D Reset Bit 12 definition expanded, Table 12 columns swapped, and Table 17 note added, Table 19 column headings changed from Typical to MAX.

Rev. D 8/3/2005

- New outline drawing (36_ICSP(5_8x5_8)SMD_MTG-341.eps) per PCN1543-K12A_PHC, Figure 16 on page 31.

Rev. C 7/29/2005

- R161 changed to R161:1, new description and bits definition
- R161 changed to R164:1, new description
- R13:0[4] new description
- R32:0[10] is now reserved
- R33:0[10] is now reserved
- R40:2[12] new description
- IFP Block Diagram Edit
- Table 1 Edit
- Conversion to 1 column template

Rev. B 11/15/2004

- Operating Conditions
- DC Electrical Characteristics (two conditions)

- Operating Power Consumption
- STANDBY Power Consumption
- Two-Wire Serial Bus Timing
- Two-Wire Serial Bus Signal Timing (two figures)
- AC Electrical Characteristics
- AC Timing Diagram
- Register Summary 0x format
- Register Description - standardized bit value definitions and register format

Rev. A 10/6/2004

- Initial release

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