1/11-Inch VGA SOC CMOS Digital Image Sensor Reflowable Camera Module with Parallel Output

MT9V113M02

Features

- Reflowable module features
  - Ultracompact
  - 260°C Pb-free solder reflowable
  - 66° diagonal field-of-view
  - 1/11-inch, two-element four-surface lens
  - Bottom contact 30-ball grid array
  - RoHS green
- Image sensor features
  - VGA resolution sensor (640 x 480) featuring DigitalClarity® CMOS imaging technology
  - 10-bit, on-chip ADC
  - Low-power standby mode
  - Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, panning, and skip 2X
  - On-chip phase-lock loop (PLL) oscillator
  - Integrated image flow processor (IFP) for complete camera in a module design
  - Two-wire serial programming interface (I^2C compatible)
  - Fail-safe I/O with programmable slew rate
  - 8-bit parallel pixel output
  - YCbCr, 565RGB, 555RGB, or 444RGB formats (progressive scan)

Applications

- Cellular phones
- PC cameras

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9V113M02	30-ball, reflowable camera module

Table 2: Key Parameters

Parameter			Value
Module size			4.15 x 4.15 x 2.5mm
Full resolution			640 x 480 pixels (VGA)
Pixel size			2.2µm x 2.2µm
Frame rate at full resolution			30 fps
ADC resolution			10-bit, on-chip
Responsivity			1.1 V/lux-sec (550nm)
Dynamic range			67.0dB
SNRMAX			>39dB
Supply voltage			
	Analog		2.5–3.1V
	Digital		1.7–1.95V
Power consumption			70mW, operating mode
Optical format			1/11-inch
F-number			2.85
Field-of-view			66° diagonal (4:3)
35mm equivalent			35mm
Depth of field			20cm to infinity (with focus at 35cm)
IR-cut filter			Yes
IR-cut frequency (T = 50%)			650nm
Spatial frequency response (SFR)			
	Field 0%	at 56 lp/mm	>0.78
		at 114 lp/mm	>0.6
		at 228 lp/mm	>0.3
	Field 70%	at 56 lp/mm	>0.68
		at 114 lp/mm	>0.5
	Field 90%	at 56 lp/mm	>0.55
		at 114 lp/mm	>0.35
System relative illumination (before correction)			>45% on edge
MAX optical distortion			<–2%, <+1%
MAX TV distortion			<1% TV lines of distortion
Operating temperature (ambient)			–15°C to +40°C

General Description

The Aptina™ Imaging MT9V113M02 is a 1/11-inch, Pb-free reflowable camera module with a pixel array of 640H x 480V. The module has a 30-ball grid array and is compatible with reflow temperatures up to 260°C. (Refer to TN-00-15 for recommended reflow profile.)

The module incorporates Aptina's Osmium™ technology—a combination of through-wafer interconnects, a redistribution layer, and wafer-level encapsulation—to distribute the ball-grid on the back side of the image sensor die.

The module's two-element four-surface lens achieves a corner relative illumination of greater than 45 percent uncorrected while maintaining a TV distortion less than +1 percent. The relative illumination of the module may be corrected and calibrated by the user through Aptina's sophisticated on-chip lens-shading correction feature that minimizes shading and color artifacts.

This reflowable camera module features an MT9V113 digital image sensor with DigitalClarity technology–Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, power consumption, and integration advantages of CMOS.

The module incorporates sophisticated on-chip camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface. An on-chip phase-lock loop (PLL) generates all internal clocks from a single master input clock.

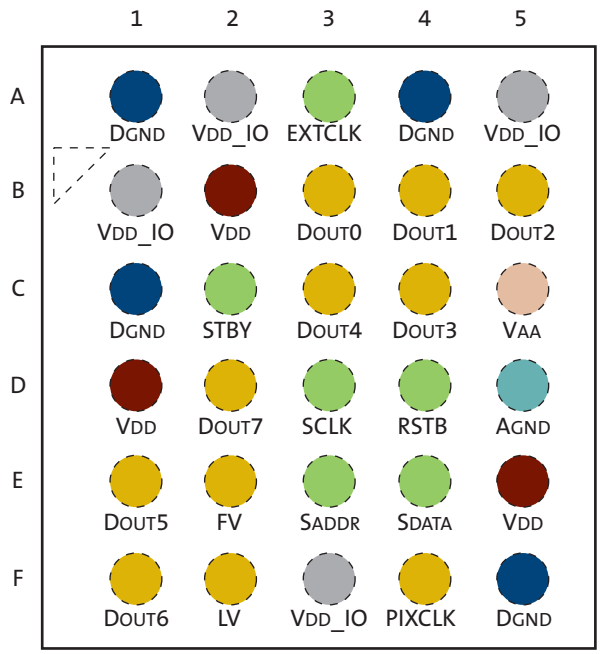
Module Pin Descriptions

Table 3: Pin Descriptions

MT9V113 Sensor Signal Name	Module Signal Name	Ball Number	Type	Description
EXTCLK	EXTCLK	A3	Input	Input clock signal.
RESET_BAR	RSTB	D4	Input	Master reset signal, active LOW (can leave floating if not used).
STANDBY	STBY	C2	Input	Controls sensor's standby mode, active HIGH.
SCLK	SCLK	D3	Input	Two-wire serial interface clock.
SADDR	SADDR	E3	Input	Selects device address for the two-wire serial interface. The address is 0x78 when SADDR is tied LOW, 0x7A when tied HIGH.
SDATA	SDATA	E4	I/O	Two-wire serial interface data.
FRAME_VALID	FV	E2	Output	Identifies rows in the active image.
LINE_VALID	LV	F2	Output	Identifies pixels in the active line.
PIXCLK	PIXCLK	F4	Output	Pixel clock.
DOUT7	DOUT7	D2	Output	8-bit image data output; bit 7 (MSB).
DOUT6	DOUT6	F1	Output	8-bit image data output; bit 6.
DOUT5	DOUT5	E1	Output	8-bit image data output; bit 5.
DOUT4	DOUT4	C3	Output	8-bit image data output; bit 4.
DOUT3	DOUT3	C4	Output	8-bit image data output; bit 3.
DOUT2	DOUT2	B5	Output	8-bit image data output; bit 2.
DOUT1	DOUT1	B4	Output	8-bit image data output; bit 1.
DOUT0	DOUT0	B3	Output	8-bit image data output; bit 0 (LSB).
VDD	VDD	B2, D1, E5	Supply	Digital power (TYP 1.8V).
VAA, VAA_PIX, VDD_PLL	VAA	C5	Supply	Analog, pixel array, and PLL power (TYP 2.8V).
VDD_IO	VDD_IO	A2, A5, B1, F3	Supply	I/O power supply (TYP 1.8V or TYP 2.8V).
DGND, GND_IO, GND_PLL	DGND	A1, A4, C1, F5	Supply	Digital, I/O, and PLL ground.
AGND	AGND	D5	Supply	Analog ground.

BGA Layout

Figure 1: 30-Ball Assignments (Top View)



Legend:

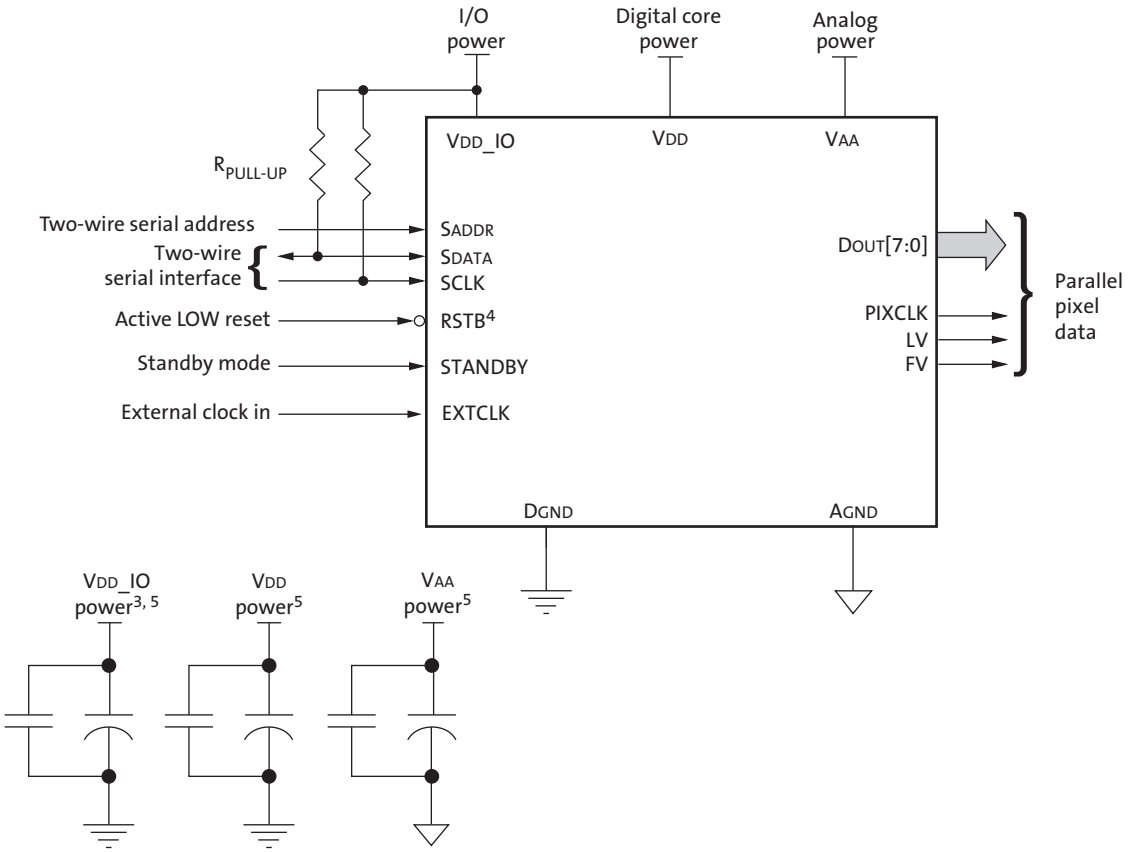
- Control: Host controls the sensor state. Used to access registers and variables.
- Data: Parallel pixel data output and line and frame synchronization signals.
- VDD: Core digital power.
- VDD_IO: I/O power.
- VAA: Analog, pixel array, and PLL power.
- DGND: Core digital, I/O, and PLL ground.
- AGND: Analog ground.

Typical Connections

Figure 2 shows typical connections for this device. For low-noise operation, the module requires separate analog and digital power supplies. All power supply rails should be decoupled from ground using capacitors as close as possible to the module. The use of inductance filters is not recommended on the power supplies or output signals.

This module supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGND) power domains that can be at different voltages. Analog requires a clean power source (VAA).

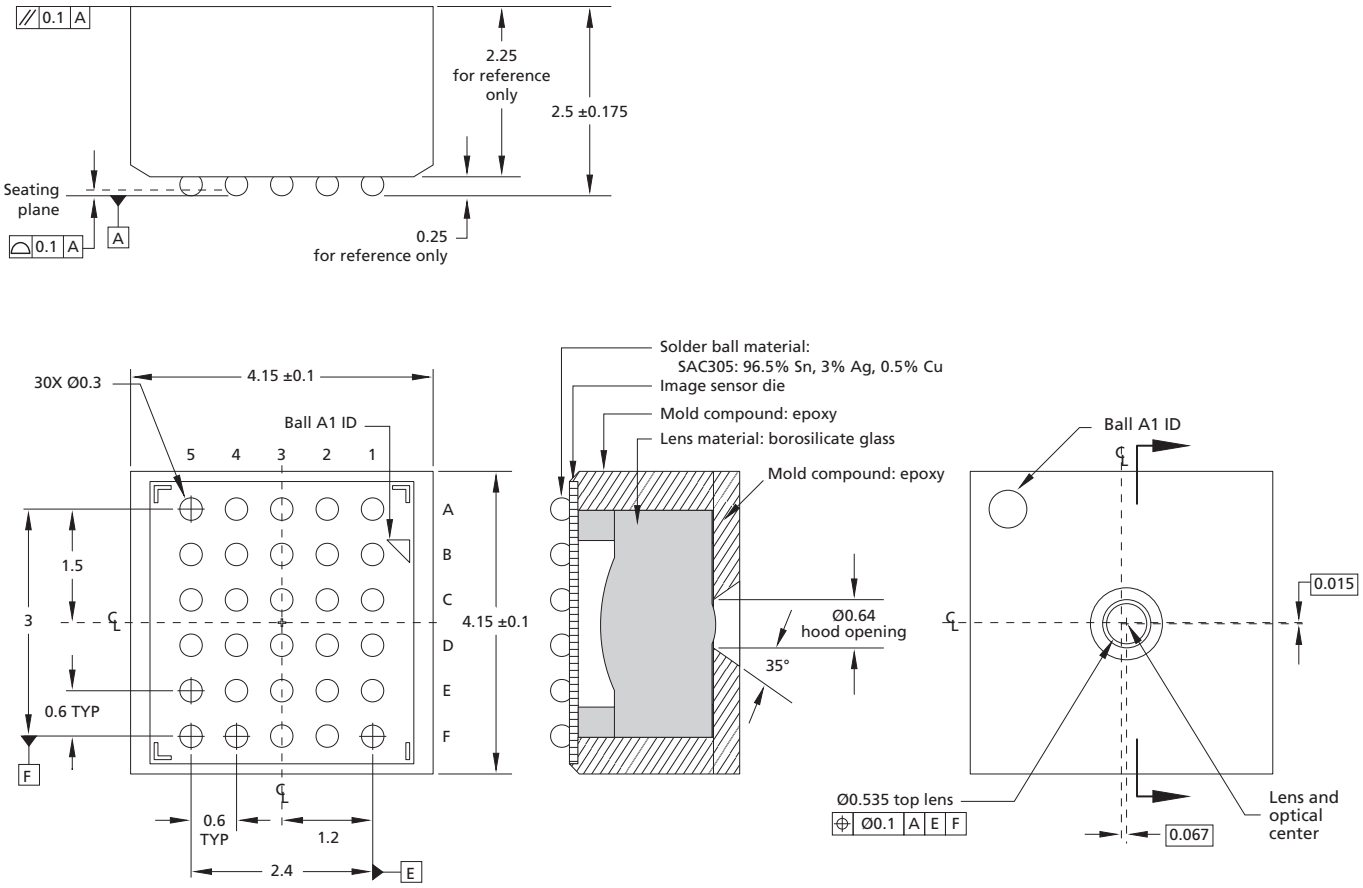
Figure 2: Typical Configuration (connection)



Notes:
1. This typical connection shows only one scenario out of multiple possible variations for this sensor.
2. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface $R_{PULL-UP}$; however, a greater value may be used for slower transmission speed.
3. All inputs must be configured with VDD_IO.
4. RSTB has an internal pull-up resistor and can be left floating.
5. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the module (Low-Z path). Actual values and numbers may vary depending on layout and design considerations, such as capacitor effective series resistance (ESR), dielectric, or power supply source impedance.

Module Dimensions

Figure 3: 30-Ball Module Dimensions



Notes: 1. Dimensions are in millimeters.

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Advance: This data sheet contains initial descriptions of products still under development.

Revision History

Rev. B **3/19/2008**

- Removed “Confidential and Proprietary” mark

Rev. B **3/3/2008**

- Updated formats
- Changed module size from 4.0 x 4.0 to 4.15 x 4.15 in Table 2, “Key Parameters,” on page 1
- Updated Figure 2: “Typical Configuration (connection),” on page 5
- Updated module size and added triangle in Figure 3: “30-Ball Module Dimensions,” on page 6

Rev. A **11/01/2007**

- Initial release