MT9V126 Registers and Variables

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

MT9V126 Register and Variable Reference

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Introduction

This reference document describes the MT9V126 registers and variables accessible for control through DevWare version 3.1-Alpha4 and after.

How to Access Registers and Variables

Registers and variables are accessed in different ways.

Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

The MT9V126 Data Sheet describes the interface protocol of the two-wire serial interface in more detail.

Variables

Variables are located in the microcontroller RAM memory. Each firmware driver has a unique ID (0...31) number and a set of variables associated with that driver. Each variable associated with that component is uniquely identified by its offset.

All driver variables can be accessed through the mcu_variable_address and mcu_variable_data registers in the XDMA register map. The variables are accessed using a logical address. This address, which is set in the mcu_variable_address register, consists of a 5-bit driver ID number and a 8-bit variable offset. This is known as indirect addressing.

Logical Addressing

The MT9V126 can access the driver variables through the XDMA registers, as shown in the example below, setting the CAM1_SENSOR_0_Y_ADDR_END variable to a value of 0x01F3..

REG= 0x098E, 0x4804 // CAM1_SENSOR_0_Y_ADDR_END

REG= 0x0990, 0x01F3 //

The address for 0x098E is calculated as follows:

1. Set Bit 15 = 0.
2. Set Bit [14:10] = driver number
3. Set bit [9:0] = offset number

The MT9V126 is capable of direct addressing the variables, as shown in the example below.

Direct Addressing

REG = 0xC804, 0x01F3 // CAM1_SENSOR_0_Y_ADDR_END

To calculate the address for direct addressing:

1. Set Bit 15 = 1.
2. Set Bit [14:10] = driver number
3. Set Bit [9:0] = offset number

Host Command Interface

The MT9V126 supports an interrupt-driven host interface. The command register (SYSCTL 0x40)is used to generate the interrupts depending on which bit is set. The host sets the bits in the command register (the firmware then clears the bits when the command completes). For a complete spec on host commands, refer to the MT9V126 Host Command Interface Specification.

Reserved

Do not change any of the reserved bits.

Register Map

Table 1 shows the locations used within the address space. Locations that are not shown in the table are reserved for future use; they should not be read from or written to maintain compatibility with future designs. Locations that are shown as "Reserved" should not be accessed. The default read values of these registers are subject to change.

Caution **The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.**

Table 1 below through Table 8 on page 15 list sensor registers and their default values. Table 9 on page 16 through Table 18 on page 29 lists sensor variables and their default values.Table 19 on page 30 through Table 26 on page 62 lists sensor registers and their descriptions.Table 27 on page 63 through Table 36 on page 89 lists sensor variables and their descriptions.

Register List and Default Values

Core Registers List

Table 1: 0: Core Registers
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	model_id_	dddd dddd dddd dddd	8833 (0x2281)
R12290 (R0x3002)	y_addr_start_	0000 dddd dddd dddd	12 (0x000C)
R12292 (R0x3004)	x_addr_start_	0000 00dd dddd dddd	16 (0x0010)
R12294 (R0x3006)	y_addr_end_	0000 dddd dddd dddd	499 (0x01F3)
R12296 (R0x3008)	x_addr_end_	0000 00dd dddd dddd	663 (0x0297)
R12298 (R0x300A)	frame_length_lines_	dddd dddd dddd dddd	525 (0x020D)
R12300 (R0x300C)	line_length_pck_	0000 dddd dddd dddd	858 (0x035A)
R12304 (R0x3010)	fine_correction	0000 dddd dddd dddd	49 (0x0031)
R12306 (R0x3012)	coarse_integration_time_	dddd dddd dddd dddd	16 (0x0010)
R12308 (R0x3014)	fine_integration_time_	0000 dddd dddd dddd	164 (0x00A4)
R12314 (R0x301A)	reset_register	dd0d 0ddd dddd dddd	4312 (0x10D8)
R12318 (R0x301E)	data_pedestal_	0000 00dd dddd dddd	42 (0x002A)
R12320 (R0x3020)	software_reset_	0000 000d 0000 0000	0 (0x0000)
R12322 (R0x3022)	grouped_parameter_hold_	0000 000d 0000 000d	0 (0x0000)

Table 1: 0: Core Registers (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12324 (R0x3024)	pixel_order_	0000 0000 0000 00??	0 (0x0000)
R12326 (R0x3026)	gpi_status	dddd dd00 0ddd ????	64639 (0xFC7F)
R12338 (R0x3032)	digital_gain_greenr_	0000 0ddd 0000 0000	256 (0x0100)
R12340 (R0x3034)	digital_gain_red_	0000 0ddd 0000 0000	256 (0x0100)
R12342 (R0x3036)	digital_gain_blue_	0000 0ddd 0000 0000	256 (0x0100)
R12344 (R0x3038)	digital_gain_greenb_	0000 0ddd 0000 0000	256 (0x0100)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12352 (R0x3040)	read_mode	dd00 dddd dddd dddd	65 (0x0041)
R12374 (R0x3056)	green1_gain	0ddd 0000 dddd dddd	4144 (0x1030)
R12376 (R0x3058)	blue_gain	0ddd 0000 dddd dddd	4144 (0x1030)
R12378 (R0x305A)	red_gain	0ddd 0000 dddd dddd	4144 (0x1030)
R12380 (R0x305C)	green2_gain	0ddd 0000 dddd dddd	4144 (0x1030)
R12382 (R0x305E)	global_gain	0ddd 0000 dddd dddd	4144 (0x1030)
R12400 (R0x3070)	test_pattern_mode_	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red_	0000 00dd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr_	0000 00dd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue_	0000 00dd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb_	0000 00dd dddd dddd	0 (0x0000)
R12448 (R0x30A0)	x_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc_	0000 0000 0000 0ddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc_	0000 0000 0000 0ddd	1 (0x0001)
R12788 (R0x31F4)	fuse_id1	dddd dddd dddd dddd	0 (0x0000)
R12790 (R0x31F6)	fuse_id2	dddd dddd dddd dddd	0 (0x0000)

Table 1: 0: Core Registers (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12792 (R0x31F8)	fuse_id3	dddd dddd dddd dddd	0 (0x0000)
R12794 (R0x31FA)	fuse_id4	dddd dddd dddd dddd	0 (0x0000)

SOC1 Registers List

Table 2: 1: SOC1 Registers
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12816 (R0x3210)	color_pipeline_control	0000 0d00 d0dd d000	176 (0x00B0)
R12884 (R0x3254)	first_color	0000 0000 0000 00dd	0 (0x0000)
R12908 (R0x326C)	aperture_parameters_2d	0ddd dddd dddd dddd	4616 (0x1208)
R12910 (R0x326E)	low_pass_yuv_filter	0000 0000 dddd dddd	128 (0x0080)
R12912 (R0x3270)	threshold_for_y_filter_r_channel	0000 dddd dddd dddd	1962 (0x07AA)
R12914 (R0x3272)	threshold_for_y_filter_g_channel	0000 dddd dddd dddd	2020 (0x07E4)
R12916 (R0x3274)	threshold_for_y_filter_b_channel	0000 0000 0ddd dddd	42 (0x002A)
R12918 (R0x3276)	black_level_to_ccm	0000 00dd dddd dddd	0 (0x0000)
R12922 (R0x327A)	red_offset	0000 000d dddd dddd	168 (0x00A8)
R12924 (R0x327C)	green1_offset	0000 000d dddd dddd	168 (0x00A8)
R12926 (R0x327E)	green2_offset	0000 000d dddd dddd	168 (0x00A8)
R12928 (R0x3280)	blue_offset	0000 000d dddd dddd	168 (0x00A8)
R12986 (R0x32BA)	red_offset_to_ccm	0000 00dd dddd dddd	0 (0x0000)
R12988 (R0x32BC)	green_offset_to_ccm	0000 00dd dddd dddd	0 (0x0000)
R12990 (R0x32BE)	blue_offset_to_ccm	0000 00dd dddd dddd	0 (0x0000)
R12992 (R0x32C0)	ccm_exp_low_byte	0ddd dddd dddd dddd	14627 (0x3923)
R12994 (R0x32C2)	ccm_exp_high_byte	0000 dddd dddd dddd	1828 (0x0724)
R12996 (R0x32C4)	ccm_elements_1_and_2	dddd dddd dddd dddd	55790 (0xD9EE)

Table 2: 1: SOC1 Registers (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12998 (R0x32C6)	ccm_elements_3_and_4	dddd dddd dddd dddd	11035 (0x2B1B)
R13000 (R0x32C8)	ccm_elements_5_and_6	dddd dddd dddd dddd	35818 (0x8BEA)
R13002 (R0x32CA)	ccm_elements_7_and_8	dddd dddd dddd dddd	32022 (0x7D16)
R13004 (R0x32CC)	ccm_elements_9_and_signs	00dd dddd dddd dddd	11714 (0x2DC2)
R13102 (R0x332E)	output_format_configuration	0000 0ddd dddd dddd	0 (0x0000)
R13104 (R0x3330)	output_format_test	0000 d00d d0dd dddd	0 (0x0000)
R13106 (R0x3332)	fm_line_count	0000 ???? ???? ????	0 (0x0000)
R13108 (R0x3334)	fm_frame_count	???? ???? ???? ????	0 (0x0000)
R13180 (R0x337C)	yuv_ycbcr_control	0000 0000 0000 dddd	6 (0x0006)
R13182 (R0x337E)	y_rgb_offset	dddd dddd dddd dddd	0 (0x0000)
R13300 (R0x33F4)	kernel_config	0000 0000 ddd0 dddd	3 (0x0003)

SOC2 Register List

Table 3: 2:SOC2 Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13888 (R0x3640)	p_g1_p0q0	dddd dddd dddd dddd	16 (0x0010)
R13890 (R0x3642)	p_g1_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13892 (R0x3644)	p_g1_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13894 (R0x3646)	p_g1_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13896 (R0x3648)	p_g1_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13898 (R0x364A)	p_r_p0q0	dddd dddd dddd dddd	16 (0x0010)
R13900 (R0x364C)	p_r_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13902 (R0x364E)	p_r_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13904 (R0x3650)	p_r_p0q3	dddd dddd dddd dddd	0 (0x0000)

Table 3: 2:SOC2 Register List (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13906 (R0x3652)	p_r_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13908 (R0x3654)	p_b_p0q0	dddd dddd dddd dddd	16 (0x0010)
R13910 (R0x3656)	p_b_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13912 (R0x3658)	p_b_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13914 (R0x365A)	p_b_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13916 (R0x365C)	p_b_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13918 (R0x365E)	p_g2_p0q0	dddd dddd dddd dddd	16 (0x0010)
R13920 (R0x3660)	p_g2_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13922 (R0x3662)	p_g2_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13924 (R0x3664)	p_g2_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13926 (R0x3666)	p_g2_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13952 (R0x3680)	p_g1_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13954 (R0x3682)	p_g1_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13956 (R0x3684)	p_g1_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13958 (R0x3686)	p_g1_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13960 (R0x3688)	p_g1_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13962 (R0x368A)	p_r_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13964 (R0x368C)	p_r_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13966 (R0x368E)	p_r_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13968 (R0x3690)	p_r_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13970 (R0x3692)	p_r_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13972 (R0x3694)	p_b_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13974 (R0x3696)	p_b_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13976 (R0x3698)	p_b_p1q2	dddd dddd dddd dddd	0 (0x0000)

Table 3: 2:SOC2 Register List (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13978 (R0x369A)	p_b_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13980 (R0x369C)	p_b_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13982 (R0x369E)	p_g2_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13984 (R0x36A0)	p_g2_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13986 (R0x36A2)	p_g2_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13988 (R0x36A4)	p_g2_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13990 (R0x36A6)	p_g2_p1q4	dddd dddd dddd dddd	0 (0x0000)
R14016 (R0x36C0)	p_g1_p2q0	dddd dddd dddd dddd	0 (0x0000)
R14018 (R0x36C2)	p_g1_p2q1	dddd dddd dddd dddd	0 (0x0000)
R14020 (R0x36C4)	p_g1_p2q2	dddd dddd dddd dddd	0 (0x0000)
R14022 (R0x36C6)	p_g1_p2q3	dddd dddd dddd dddd	0 (0x0000)
R14024 (R0x36C8)	p_g1_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14026 (R0x36CA)	p_r_p2q0	dddd dddd dddd dddd	0 (0x0000)
R14028 (R0x36CC)	p_r_p2q1	dddd dddd dddd dddd	0 (0x0000)
R14030 (R0x36CE)	p_r_p2q2	dddd dddd dddd dddd	0 (0x0000)
R14032 (R0x36D0)	p_r_p2q3	dddd dddd dddd dddd	0 (0x0000)
R14034 (R0x36D2)	p_r_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14036 (R0x36D4)	p_b_p2q0	dddd dddd dddd dddd	0 (0x0000)
R14038 (R0x36D6)	p_b_p2q1	dddd dddd dddd dddd	0 (0x0000)
R14040 (R0x36D8)	p_b_p2q2	dddd dddd dddd dddd	0 (0x0000)
R14042 (R0x36DA)	p_b_p2q3	dddd dddd dddd dddd	0 (0x0000)
R14044 (R0x36DC)	p_b_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14046 (R0x36DE)	p_g2_p2q0	dddd dddd dddd dddd	0 (0x0000)
R14048 (R0x36E0)	p_g2_p2q1	dddd dddd dddd dddd	0 (0x0000)

Table 3: 2:SOC2 Register List (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14050 (R0x36E2)	p_g2_p2q2	dddd dddd dddd dddd	0 (0x0000)
R14052 (R0x36E4)	p_g2_p2q3	dddd dddd dddd dddd	0 (0x0000)
R14054 (R0x36E6)	p_g2_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14080 (R0x3700)	p_g1_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14082 (R0x3702)	p_g1_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14084 (R0x3704)	p_g1_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14086 (R0x3706)	p_g1_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14088 (R0x3708)	p_g1_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14090 (R0x370A)	p_r_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14092 (R0x370C)	p_r_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14094 (R0x370E)	p_r_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14096 (R0x3710)	p_r_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14098 (R0x3712)	p_r_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14100 (R0x3714)	p_b_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14102 (R0x3716)	p_b_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14104 (R0x3718)	p_b_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14106 (R0x371A)	p_b_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14108 (R0x371C)	p_b_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14110 (R0x371E)	p_g2_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14112 (R0x3720)	p_g2_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14114 (R0x3722)	p_g2_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14116 (R0x3724)	p_g2_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14118 (R0x3726)	p_g2_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14144 (R0x3740)	p_g1_p4q0	dddd dddd dddd dddd	0 (0x0000)

Table 3: 2:SOC2 Register List (continued)

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14146 (R0x3742)	p_g1_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14148 (R0x3744)	p_g1_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14150 (R0x3746)	p_g1_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14152 (R0x3748)	p_g1_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14154 (R0x374A)	p_r_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14156 (R0x374C)	p_r_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14158 (R0x374E)	p_r_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14160 (R0x3750)	p_r_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14162 (R0x3752)	p_r_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14164 (R0x3754)	p_b_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14166 (R0x3756)	p_b_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14168 (R0x3758)	p_b_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14170 (R0x375A)	p_b_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14172 (R0x375C)	p_b_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14174 (R0x375E)	p_g2_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14176 (R0x3760)	p_g2_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14178 (R0x3762)	p_g2_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14180 (R0x3764)	p_g2_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14182 (R0x3766)	p_g2_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14208 (R0x3780)	pga_control	0000 000d dddd ddd0	72 (0x0048)

SYSCTL Register List

Table 4: SYSCTL Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R0 (R0x0000)	k22b_chip_id	???? ???? ???? ????	8833 (0x2281)
R16 (R0x0010)	pll_dividers	00dd dddd dddd dddd	530 (0x0212)
R18 (R0x0012)	pll_p_dividers	00dd dddd ???? ????	0 (0x0000)
R20 (R0x0014)	pll_control	?d0d dddd dddd dddd	22598 (0x5846)
R26 (R0x001A)	reset_and_misc_control	dddd 0000 0000 000d	0 (0x0000)
R48 (R0x0030)	pad_slew	0ddd 0ddd 0ddd 0ddd	1024 (0x0400)
R50 (R0x0032)	pad_control	dddd 00d0 dd0d 000d	209 (0x00D1)
R52 (R0x0034)	pad_gpi_status	???? 000? ???? ????	0 (0x0000)
R64 (R0x0040)	command_register	dddd dddd dddd dddd	0 (0x0000)

XDMA Register List

Table 5: XDMA Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R2434 (R0x0982)	access_ctl_stat	0000 0000 dd0? ???d	0 (0x0000)
R2442 (R0x098A)	physical_address_access	dddd dddd dddd dddd	0 (0x0000)
R2446 (R0x098E)	logical_address_access	dddd dddd dddd dddd	0 (0x0000)
R2448 (R0x0990)	mcu_variable_data0	dddd dddd dddd dddd	0 (0x0000)
R2450 (R0x0992)	mcu_variable_data1	dddd dddd dddd dddd	0 (0x0000)
R2452 (R0x0994)	mcu_variable_data2	dddd dddd dddd dddd	0 (0x0000)
R2454 (R0x0996)	mcu_variable_data3	dddd dddd dddd dddd	0 (0x0000)
R2456 (R0x0998)	mcu_variable_data4	dddd dddd dddd dddd	0 (0x0000)
R2458 (R0x099A)	mcu_variable_data5	dddd dddd dddd dddd	0 (0x0000)
R2460 (R0x099C)	mcu_variable_data6	dddd dddd dddd dddd	0 (0x0000)

Table 5: XDMA Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R2462 (R0x099E)	mcu_variable_data7	dddd dddd dddd dddd	0 (0x0000)

TX_SS Register List

Table 6: TX_SS Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R15360 (R0x3C00)	parallel_bus_ctrl	000d 000d 000d 0ddd	4096 (0x1000)
R15362 (R0x3C02)	gpo	dddd 000d dddd dddd	0 (0x0000)
R15368 (R0x3C08)	tvenc_ctrl_1	00dd 000d 000d 000d	8193 (0x2001)
R15370 (R0x3C0A)	tvenc_ctrl_2	00dd 00dd 00dd 00dd	0 (0x0000)

OVERLAY_SS Register List

Table 7: OVERLAY_SS Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R20224 (R0x4F00)	overlay_status	??00 0000 00?? ????	49152 (0xC000)
R20226 (R0x4F02)	overlay_control	d000 0000 0000 000d	0 (0x0000)
R20228 (R0x4F04)	overlay_interrupt_control	0000 0000 0000 0ddd	X

DEWARP_SS Register List

Table 8: DEWARP_SS Registers List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R16384 (R0x4000)	dewarp_control	d000 0000 0000 0ddd	0 (0x0000)
R16424 (R0x4028)	cpxc_fpme_l	dddd dddd dddd dddd	0 (0x0000)
R16426 (R0x402A)	cpxc_fpme_h	dddd dddd dddd dddd	0 (0x0000)

Variable List and Default Values

Monitor Variable List

Table 9: 0: Monitor Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0x8000 VAR(0x00,0x0000)	mon_major_version	dddd dddd dddd dddd	0 (0x0000)
0x8002 VAR(0x00,0x0002)	mon_minor_version	dddd dddd dddd dddd	0 (0x0000)
0x8004 VAR(0x00,0x0004)	mon_release_version	dddd dddd dddd dddd	0 (0x0000)
0x8006 VAR(0x00,0x0006)	mon_heartbeat	dddd dddd dddd dddd	0 (0x0000)

Binning Off Context Variable List

Table 10: 6: Binning Off Context Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0x9800 VAR(0x06,0x0000)	bin_off_config_ae_track_algo_enter	dddd dddd dddd dddd	0 (0x0000)
0x9802 VAR(0x06,0x0002)	bin_off_config_ae_track_algo_run	dddd dddd dddd dddd	15 (0x000F)
0x9804 VAR(0x06,0x0004)	bin_off_config_awb_algo_enter	dddd dddd dddd dddd	0 (0x0000)
0x9806 VAR(0x06,0x0006)	bin_off_config_awb_algo_run	dddd dddd dddd dddd	255 (0x00FF)
0x9808 VAR(0x06,0x0008)	bin_off_config_awb_awb_xshift	dddd dddd dddd dddd	27 (0x001B)
0x980A VAR(0x06,0x000A)	bin_off_config_awb_awb_yshift	dddd dddd dddd dddd	31 (0x001F)
0x980C VAR(0x06,0x000C)	bin_off_config_ll_algo_enter	dddd dddd dddd dddd	0 (0x0000)
0x980E VAR(0x06,0x000E)	bin_off_config_ll_algo_run	dddd dddd dddd dddd	125 (0x007D)
0x9810 VAR(0x06,0x0010)	bin_off_config_stat_algo_enter	dddd dddd dddd dddd	65535 (0xFFFF)
0x9812 VAR(0x06,0x0012)	bin_off_config_stat_algo_run	dddd dddd dddd dddd	65535 (0xFFFF)
0x9814 VAR(0x06,0x0014)	bin_off_config_sysctl_algo_enter	dddd dddd dddd dddd	2 (0x0002)
0x9816 VAR(0x06,0x0016)	bin_off_config_sysctl_algo_run	dddd dddd dddd dddd	124 (0x007C)

AE_Rule Variable List

Table 11: 9: AE_Rule Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xA404 VAR(0x09,0x0004)	ae_rule_algo	dddd dddd dddd dddd	4 (0x0004)
0xA408 VAR(0x09,0x0008)	ae_rule_ae_weight_table_0_0	dddd dddd dddd dddd	100 (0x0064)
0xA40A VAR(0x09,0x000A)	ae_rule_ae_weight_table_0_1	dddd dddd dddd dddd	100 (0x0064)
0xA40C VAR(0x09,0x000C)	ae_rule_ae_weight_table_0_2	dddd dddd dddd dddd	100 (0x0064)
0xA40E VAR(0x09,0x000E)	ae_rule_ae_weight_table_0_3	dddd dddd dddd dddd	100 (0x0064)
0xA410 VAR(0x09,0x0010)	ae_rule_ae_weight_table_0_4	dddd dddd dddd dddd	100 (0x0064)
0xA412 VAR(0x09,0x0012)	ae_rule_ae_weight_table_1_0	dddd dddd dddd dddd	100 (0x0064)
0xA414 VAR(0x09,0x0014)	ae_rule_ae_weight_table_1_1	dddd dddd dddd dddd	100 (0x0064)
0xA416 VAR(0x09,0x0016)	ae_rule_ae_weight_table_1_2	dddd dddd dddd dddd	100 (0x0064)
0xA418 VAR(0x09,0x0018)	ae_rule_ae_weight_table_1_3	dddd dddd dddd dddd	100 (0x0064)
0xA41A VAR(0x09,0x001A)	ae_rule_ae_weight_table_1_4	dddd dddd dddd dddd	100 (0x0064)
0xA41C VAR(0x09,0x001C)	ae_rule_ae_weight_table_2_0	dddd dddd dddd dddd	100 (0x0064)
0xA41E VAR(0x09,0x001E)	ae_rule_ae_weight_table_2_1	dddd dddd dddd dddd	100 (0x0064)
0xA420 VAR(0x09,0x0020)	ae_rule_ae_weight_table_2_2	dddd dddd dddd dddd	100 (0x0064)
0xA422 VAR(0x09,0x0022)	ae_rule_ae_weight_table_2_3	dddd dddd dddd dddd	100 (0x0064)
0xA424 VAR(0x09,0x0024)	ae_rule_ae_weight_table_2_4	dddd dddd dddd dddd	100 (0x0064)
0xA426 VAR(0x09,0x0026)	ae_rule_ae_weight_table_3_0	dddd dddd dddd dddd	100 (0x0064)
0xA428 VAR(0x09,0x0028)	ae_rule_ae_weight_table_3_1	dddd dddd dddd dddd	100 (0x0064)
0xA42A VAR(0x09,0x002A)	ae_rule_ae_weight_table_3_2	dddd dddd dddd dddd	100 (0x0064)
0xA42C VAR(0x09,0x002C)	ae_rule_ae_weight_table_3_3	dddd dddd dddd dddd	100 (0x0064)
0xA42E VAR(0x09,0x002E)	ae_rule_ae_weight_table_3_4	dddd dddd dddd dddd	100 (0x0064)
0xA430 VAR(0x09,0x0030)	ae_rule_ae_weight_table_4_0	dddd dddd dddd dddd	100 (0x0064)
0xA432 VAR(0x09,0x0032)	ae_rule_ae_weight_table_4_1	dddd dddd dddd dddd	100 (0x0064)

Table 11: 9: AE_Rule Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xA434 VAR(0x09,0x0034)	ae_rule_ae_weight_table_4_2	dddd dddd dddd dddd	100 (0x0064)
0xA436 VAR(0x09,0x0036)	ae_rule_ae_weight_table_4_3	dddd dddd dddd dddd	100 (0x0064)
0xA438 VAR(0x09,0x0038)	ae_rule_ae_weight_table_4_4	dddd dddd dddd dddd	100 (0x0064)

AE_Track Variable List

Table 12: 10: AE_Track Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xA800 VAR(0x0A,0x0000)	ae_track_status	dddd dddd dddd dddd	0 (0x0000)
0xA802 VAR(0x0A,0x0002)	ae_track_mode	dddd dddd dddd dddd	83 (0x0053)
0xA804 VAR(0x0A,0x0004)	ae_track_algo	dddd dddd dddd dddd	0 (0x0000)
0xA806 VAR(0x0A,0x0006)	ae_track_current_black_level	dddd dddd dddd dddd	8 (0x0008)
0xA808 VAR(0x0A,0x0008)	ae_track_black_clipping_gate	dddd dddd dddd dddd	4 (0x0004)
0xA80A VAR(0x0A,0x000A)	ae_track_max_black_level	dddd dddd dddd dddd	64 (0x0040)
0xA80C VAR(0x0A,0x000C)	ae_track_black_level_damping	dddd dddd dddd dddd	3 (0x0003)
0xA812 VAR(0x0A,0x0012)	ae_track_target	dddd dddd dddd dddd	75 (0x004B)
0xA814 VAR(0x0A,0x0014)	ae_track_gate	dddd dddd dddd dddd	4 (0x0004)
0xA816 VAR(0x0A,0x0016)	ae_track_current_average_y	dddd dddd dddd dddd	0 (0x0000)
0xA818 VAR(0x0A,0x0018)	ae_track_ae_tracking_damping	dddd dddd dddd dddd	16 (0x0010)
0xA81A VAR(0x0A,0x001A)	ae_track_jump_divisor	dddd dddd dddd dddd	3 (0x0003)
0xA824 VAR(0x0A,0x0024)	ae_track_current_fdperiod	dddd dddd dddd dddd	262 (0x0106)
0xA826 VAR(0x0A,0x0026)	ae_track_current_max_fdzone	dddd dddd dddd dddd	2 (0x0002)
0xA82A VAR(0x0A,0x002A)	ae_track_fdzone	dddd dddd dddd dddd	1 (0x0001)
0xA830 VAR(0x0A,0x0030)	ae_track_zone	dddd dddd dddd dddd	1 (0x0001)
0xA832 VAR(0x0A,0x0032)	ae_track_virt_dgain	dddd dddd dddd dddd	128 (0x0080)

Table 12: 10: AE_Track Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xA834 VAR(0x0A,0x0034)	ae_track_virt_again	dddd dddd dddd dddd	32 (0x0020)
0xA838 VAR(0x0A,0x0038)	ae_track_virt_column_gain	dddd dddd dddd dddd	0 (0x0000)
0xA83A VAR(0x0A,0x003A)	ae_track_dcggain	dddd dddd dddd dddd	0 (0x0000)
0xA83C VAR(0x0A,0x003C)	ae_track_virt_int_time	dddd dddd dddd dddd dddd dddd dddd dddd	0 (0x00000000)
0xA840 VAR(0x0A,0x0040)	ae_track_int_time_pclk	dddd dddd dddd dddd	0 (0x0000)
0xA842 VAR(0x0A,0x0042)	ae_track_int_time_lines	dddd dddd dddd dddd	0 (0x0000)

AWB VariableList

Table 13: 11:AWB Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xAC00 VAR(0x0B,0x0000)	awb_status	dddd dddd dddd dddd	0 (0x0000)
0xAC02 VAR(0x0B,0x0002)	awb_mode	dddd dddd dddd dddd	10 (0x000A)
0xAC04 VAR(0x0B,0x0004)	awb_algo	dddd dddd dddd dddd	0 (0x0000)
0xAC0A VAR(0x0B,0x000A)	awb_ccm_0	dddd dddd dddd dddd	0 (0x0000)
0xAC0C VAR(0x0B,0x000C)	awb_ccm_1	dddd dddd dddd dddd	0 (0x0000)
0xAC0E VAR(0x0B,0x000E)	awb_ccm_2	dddd dddd dddd dddd	0 (0x0000)
0xAC10 VAR(0x0B,0x0010)	awb_ccm_3	dddd dddd dddd dddd	0 (0x0000)
0xAC12 VAR(0x0B,0x0012)	awb_ccm_4	dddd dddd dddd dddd	0 (0x0000)
0xAC14 VAR(0x0B,0x0014)	awb_ccm_5	dddd dddd dddd dddd	0 (0x0000)
0xAC16 VAR(0x0B,0x0016)	awb_ccm_6	dddd dddd dddd dddd	0 (0x0000)
0xAC18 VAR(0x0B,0x0018)	awb_ccm_7	dddd dddd dddd dddd	0 (0x0000)
0xAC1A VAR(0x0B,0x001A)	awb_ccm_8	dddd dddd dddd dddd	0 (0x0000)
0xAC1C VAR(0x0B,0x001C)	awb_ccm_9	dddd dddd dddd dddd	0 (0x0000)
0xAC1E VAR(0x0B,0x001E)	awb_ccm_10	dddd dddd dddd dddd	0 (0x0000)

Table 13: 11:AWB Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xAC32 VAR(0x0B,0x0032)	awb_saturation	dddd dddd dddd dddd	128 (0x0080)
0xAC36 VAR(0x0B,0x0036)	awb_ccmposition	dddd dddd dddd dddd	64 (0x0040)
0xAC38 VAR(0x0B,0x0038)	awb_r_ratio_lower	dddd dddd dddd dddd	98 (0x0062)
0xAC3A VAR(0x0B,0x003A)	awb_r_ratio_upper	dddd dddd dddd dddd	104 (0x0068)
0xAC3C VAR(0x0B,0x003C)	awb_b_ratio_lower	dddd dddd dddd dddd	98 (0x0062)
0xAC3E VAR(0x0B,0x003E)	awb_b_ratio_upper	dddd dddd dddd dddd	104 (0x0068)
0xAC40 VAR(0x0B,0x0040)	awb_r_scene_ratio_lower	dddd dddd dddd dddd	50 (0x0032)
0xAC42 VAR(0x0B,0x0042)	awb_r_scene_ratio_upper	dddd dddd dddd dddd	200 (0x00C8)
0xAC44 VAR(0x0B,0x0044)	awb_b_scene_ratio_lower	dddd dddd dddd dddd	35 (0x0023)
0xAC46 VAR(0x0B,0x0046)	awb_b_scene_ratio_upper	dddd dddd dddd dddd	200 (0x00C8)
0xAC48 VAR(0x0B,0x0048)	awb_r_ratio_pre_awb	dddd dddd dddd dddd	100 (0x0064)
0xAC4A VAR(0x0B,0x004A)	awb_b_ratio_pre_awb	dddd dddd dddd dddd	100 (0x0064)
0xAC4C VAR(0x0B,0x004C)	awb_r_ratio_post_awb	dddd dddd dddd dddd	100 (0x0064)
0xAC4E VAR(0x0B,0x004E)	awb_b_ratio_post_awb	dddd dddd dddd dddd	100 (0x0064)

Stat Variable List

Table 14: 14: Stat Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xB878 VAR(0x0E,0x0078)	stat_inv_brightness_metric	dddd dddd dddd dddd	0 (0x0000)
0xB87A VAR(0x0E,0x007A)	stat_gain_metric	dddd dddd dddd dddd	0 (0x0000)

Low Light Variable List

Table 15: Low Light Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xBC02 VAR(0x0F,0x0002)	ll_mode	dddd dddd dddd dddd	3 (0x0003)
0xBC04 VAR(0x0F,0x0004)	ll_algo	dddd dddd dddd dddd	0 (0x0000)
0xBC06 VAR(0x0F,0x0006)	ll_cluster_dc_th	dddd dddd dddd dddd	1 (0x0001)
0xBC08 VAR(0x0F,0x0008)	ll_gamma_select	dddd dddd dddd dddd	0 (0x0000)
0xBC0A VAR(0x0F,0x000A)	ll_gamma_position	dddd dddd dddd dddd	0 (0x0000)
0xBC0C VAR(0x0F,0x000C)	ll_gamma_contrast_curve_0	dddd dddd dddd dddd	0 (0x0000)
0xBC0E VAR(0x0F,0x000E)	ll_gamma_contrast_curve_1	dddd dddd dddd dddd	20 (0x0014)
0xBC10 VAR(0x0F,0x0010)	ll_gamma_contrast_curve_2	dddd dddd dddd dddd	32 (0x0020)
0xBC12 VAR(0x0F,0x0012)	ll_gamma_contrast_curve_3	dddd dddd dddd dddd	53 (0x0035)
0xBC14 VAR(0x0F,0x0014)	ll_gamma_contrast_curve_4	dddd dddd dddd dddd	88 (0x0058)
0xBC16 VAR(0x0F,0x0016)	ll_gamma_contrast_curve_5	dddd dddd dddd dddd	117 (0x0075)
0xBC18 VAR(0x0F,0x0018)	ll_gamma_contrast_curve_6	dddd dddd dddd dddd	142 (0x008E)
0xBC1A VAR(0x0F,0x001A)	ll_gamma_contrast_curve_7	dddd dddd dddd dddd	163 (0x00A3)
0xBC1C VAR(0x0F,0x001C)	ll_gamma_contrast_curve_8	dddd dddd dddd dddd	181 (0x00B5)
0xBC1E VAR(0x0F,0x001E)	ll_gamma_contrast_curve_9	dddd dddd dddd dddd	197 (0x00C5)
0xBC20 VAR(0x0F,0x0020)	ll_gamma_contrast_curve_10	dddd dddd dddd dddd	211 (0x00D3)
0xBC22 VAR(0x0F,0x0022)	ll_gamma_contrast_curve_11	dddd dddd dddd dddd	221 (0x00DD)
0xBC24 VAR(0x0F,0x0024)	ll_gamma_contrast_curve_12	dddd dddd dddd dddd	230 (0x00E6)
0xBC26 VAR(0x0F,0x0026)	ll_gamma_contrast_curve_13	dddd dddd dddd dddd	237 (0x00ED)
0xBC28 VAR(0x0F,0x0028)	ll_gamma_contrast_curve_14	dddd dddd dddd dddd	242 (0x00F2)
0xBC2A VAR(0x0F,0x002A)	ll_gamma_contrast_curve_15	dddd dddd dddd dddd	246 (0x00F6)
0xBC2C VAR(0x0F,0x002C)	ll_gamma_contrast_curve_16	dddd dddd dddd dddd	249 (0x00F9)
0xBC2E VAR(0x0F,0x002E)	ll_gamma_contrast_curve_17	dddd dddd dddd dddd	252 (0x00FC)

Table 15: Low Light Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xBC30 VAR(0x0F,0x0030)	ll_gamma_contrast_curve_18	dddd dddd dddd dddd	255 (0x00FF)
0xBC32 VAR(0x0F,0x0032)	ll_gamma_nrcurve_0	dddd dddd dddd dddd	0 (0x0000)
0xBC34 VAR(0x0F,0x0034)	ll_gamma_nrcurve_1	dddd dddd dddd dddd	20 (0x0014)
0xBC36 VAR(0x0F,0x0036)	ll_gamma_nrcurve_2	dddd dddd dddd dddd	38 (0x0026)
0xBC38 VAR(0x0F,0x0038)	ll_gamma_nrcurve_3	dddd dddd dddd dddd	61 (0x003D)
0xBC3A VAR(0x0F,0x003A)	ll_gamma_nrcurve_4	dddd dddd dddd dddd	95 (0x005F)
0xBC3C VAR(0x0F,0x003C)	ll_gamma_nrcurve_5	dddd dddd dddd dddd	120 (0x0078)
0xBC3E VAR(0x0F,0x003E)	ll_gamma_nrcurve_6	dddd dddd dddd dddd	138 (0x008A)
0xBC40 VAR(0x0F,0x0040)	ll_gamma_nrcurve_7	dddd dddd dddd dddd	152 (0x0098)
0xBC42 VAR(0x0F,0x0042)	ll_gamma_nrcurve_8	dddd dddd dddd dddd	166 (0x00A6)
0xBC44 VAR(0x0F,0x0044)	ll_gamma_nrcurve_9	dddd dddd dddd dddd	178 (0x00B2)
0xBC46 VAR(0x0F,0x0046)	ll_gamma_nrcurve_10	dddd dddd dddd dddd	188 (0x00BC)
0xBC48 VAR(0x0F,0x0048)	ll_gamma_nrcurve_11	dddd dddd dddd dddd	198 (0x00C6)
0xBC4A VAR(0x0F,0x004A)	ll_gamma_nrcurve_12	dddd dddd dddd dddd	208 (0x00D0)
0xBC4C VAR(0x0F,0x004C)	ll_gamma_nrcurve_13	dddd dddd dddd dddd	216 (0x00D8)
0xBC4E VAR(0x0F,0x004E)	ll_gamma_nrcurve_14	dddd dddd dddd dddd	225 (0x00E1)
0xBC50 VAR(0x0F,0x0050)	ll_gamma_nrcurve_15	dddd dddd dddd dddd	233 (0x00E9)
0xBC52 VAR(0x0F,0x0052)	ll_gamma_nrcurve_16	dddd dddd dddd dddd	241 (0x00F1)
0xBC54 VAR(0x0F,0x0054)	ll_gamma_nrcurve_17	dddd dddd dddd dddd	248 (0x00F8)
0xBC56 VAR(0x0F,0x0056)	ll_gamma_nrcurve_18	dddd dddd dddd dddd	255 (0x00FF)
0xBC58 VAR(0x0F,0x0058)	ll_tclimit	dddd dddd dddd dddd	36 (0x0024)
0xBC5A VAR(0x0F,0x005A)	ll_tcbase	dddd dddd dddd dddd	8 (0x0008)
0xBC5C VAR(0x0F,0x005C)	ll_start_tcauto_limiter	dddd dddd dddd dddd	45 (0x002D)
0xBC5E VAR(0x0F,0x005E)	ll_stop_tcauto_limiter	dddd dddd dddd dddd	220 (0x00DC)

Table 15: Low Light Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xBC60 VAR(0x0F,0x0060)	ll_tonal_curve_high	dddd dddd dddd dddd	127 (0x007F)
0xBC62 VAR(0x0F,0x0062)	ll_tonal_curve_med	dddd dddd dddd dddd	127 (0x007F)
0xBC64 VAR(0x0F,0x0064)	ll_tonal_curve_low	dddd dddd dddd dddd	127 (0x007F)

Cam1Control Variable List

Table 16: 18: Cam1Control Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC800 VAR(0x12,0x0000)	cam1_sensor_0_y_addr_start	dddd dddd dddd dddd	12 (0x000C)
0xC802 VAR(0x12,0x0002)	cam1_sensor_0_x_addr_start	dddd dddd dddd dddd	16 (0x0010)
0xC804 VAR(0x12,0x0004)	cam1_sensor_0_y_addr_end	dddd dddd dddd dddd	499 (0x01F3)
0xC806 VAR(0x12,0x0006)	cam1_sensor_0_x_addr_end	dddd dddd dddd dddd	663 (0x0297)
0xC80A VAR(0x12,0x000A)	cam1_sensor_0_read_mode	dddd dddd dddd dddd	65 (0x0041)
0xC812 VAR(0x12,0x0012)	cam1_sensor_0_frame_length_lines	dddd dddd dddd dddd	525 (0x020D)
0xC814 VAR(0x12,0x0014)	cam1_sensor_0_line_length_pck	dddd dddd dddd dddd	858 (0x035A)
0xC816 VAR(0x12,0x0016)	cam1_sensor_0_fine_correction	dddd dddd dddd dddd	49 (0x0031)
0xC81A VAR(0x12,0x001A)	cam1_sensor_0_awb_hg_window_xstart	dddd dddd dddd dddd	0 (0x0000)
0xC81C VAR(0x12,0x001C)	cam1_sensor_0_awb_hg_window_ystart	dddd dddd dddd dddd	0 (0x0000)
0xC81E VAR(0x12,0x001E)	cam1_sensor_0_awb_hg_window_xend	dddd dddd dddd dddd	646 (0x0286)
0xC820 VAR(0x12,0x0020)	cam1_sensor_0_awb_hg_window_yend	dddd dddd dddd dddd	486 (0x01E6)
0xC822 VAR(0x12,0x0022)	cam1_sensor_0_ae_initial_window_xstart	dddd dddd dddd dddd	4 (0x0004)
0xC824 VAR(0x12,0x0024)	cam1_sensor_0_ae_initial_window_ystart	dddd dddd dddd dddd	4 (0x0004)
0xC826 VAR(0x12,0x0026)	cam1_sensor_0_ae_initial_window_xend	dddd dddd dddd dddd	132 (0x0084)
0xC828 VAR(0x12,0x0028)	cam1_sensor_0_ae_initial_window_yend	dddd dddd dddd dddd	100 (0x0064)
0xC82A VAR(0x12,0x002A)	cam1_sensor_0_fdperiod_0	dddd dddd dddd dddd	262 (0x0106)

Table 16: 18: Cam1Control Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC82C VAR(0x12,0x002C)	cam1_sensor_0_fdperiod_1	dddd dddd dddd dddd	315 (0x013B)
0xC82E VAR(0x12,0x002E)	cam1_sensor_0_max_fdzone_0	dddd dddd dddd dddd	2 (0x0002)
0xC830 VAR(0x12,0x0030)	cam1_sensor_0_max_fdzone_1	dddd dddd dddd dddd	1 (0x0001)
0xC86C VAR(0x12,0x006C)	cam1_analog_gain	dddd dddd dddd dddd	32 (0x0020)
0xC86E VAR(0x12,0x006E)	cam1_analog_red_gain	dddd dddd dddd dddd	32 (0x0020)
0xC870 VAR(0x12,0x0070)	cam1_analog_green1gain	dddd dddd dddd dddd	32 (0x0020)
0xC872 VAR(0x12,0x0072)	cam1_analog_green2gain	dddd dddd dddd dddd	32 (0x0020)
0xC874 VAR(0x12,0x0074)	cam1_analog_blue_gain	dddd dddd dddd dddd	32 (0x0020)
0xC876 VAR(0x12,0x0076)	cam1_digital_gain	dddd dddd dddd dddd	128 (0x0080)
0xC87A VAR(0x12,0x007A)	cam1_min_analog_gain	dddd dddd dddd dddd	1 (0x0001)
0xC87C VAR(0x12,0x007C)	cam1_max_analog_gain	dddd dddd dddd dddd	504 (0x01F8)
0xC87E VAR(0x12,0x007E)	cam1_dgain_red	dddd dddd dddd dddd	128 (0x0080)
0xC880 VAR(0x12,0x0080)	cam1_dgain_green1	dddd dddd dddd dddd	128 (0x0080)
0xC882 VAR(0x12,0x0082)	cam1_dgain_green2	dddd dddd dddd dddd	128 (0x0080)
0xC884 VAR(0x12,0x0084)	cam1_dgain_blue	dddd dddd dddd dddd	128 (0x0080)
0xC886 VAR(0x12,0x0086)	cam1_dgain_second	dddd dddd dddd dddd	128 (0x0080)
0xC888 VAR(0x12,0x0088)	cam1_virt_int_time	dddd dddd dddd dddd	0 (0x0000)
0xC88A VAR(0x12,0x008A)	cam1_coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
0xC88C VAR(0x12,0x008C)	cam1_fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
0xC88E VAR(0x12,0x008E)	cam1_first_black_level	dddd dddd dddd dddd	42 (0x002A)
0xC890 VAR(0x12,0x0090)	cam1_second_black_level	dddd dddd dddd dddd	8 (0x0008)
0xC892 VAR(0x12,0x0092)	cam1_sensor_x_offset	dddd dddd dddd dddd	16 (0x0010)
0xC894 VAR(0x12,0x0094)	cam1_sensor_y_offset	dddd dddd dddd dddd	12 (0x000C)
0xC896 VAR(0x12,0x0096)	cam1_flicker_mode	dddd dddd dddd dddd	0 (0x0000)

Table 16: 18: Cam1Control Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC898 VAR(0x12,0x0098)	cam1_aet_black_clipping_target	dddd dddd dddd dddd	1024 (0x0400)
0xC89A VAR(0x12,0x009A)	cam1_aet_skip_frames	dddd dddd dddd dddd	1 (0x0001)
0xC89C VAR(0x12,0x009C)	cam1_aet_target_fdzone	dddd dddd dddd dddd	2 (0x0002)
0xC89E VAR(0x12,0x009E)	cam1_aet_target_again	dddd dddd dddd dddd	64 (0x0040)
0xC8A0 VAR(0x12,0x00A0)	cam1_aet_ae_min_virt_int_time_pclk	dddd dddd dddd dddd	32 (0x0020)
0xC8A2 VAR(0x12,0x00A2)	cam1_aet_ae_min_virt_dgain	dddd dddd dddd dddd	128 (0x0080)
0xC8A4 VAR(0x12,0x00A4)	cam1_aet_ae_max_virt_dgain	dddd dddd dddd dddd	128 (0x0080)
0xC8A6 VAR(0x12,0x00A6)	cam1_aet_ae_min_virt_again	dddd dddd dddd dddd	32 (0x0020)
0xC8A8 VAR(0x12,0x00A8)	cam1_aet_ae_max_virt_again	dddd dddd dddd dddd	7500 (0x1D4C)
0xC8AC VAR(0x12,0x00AC)	cam1_aet_ae_virt_gain_th_cg	dddd dddd dddd dddd	128 (0x0080)
0xC8AE VAR(0x12,0x00AE)	cam1_aet_ae_virt_gain_th_dcg	dddd dddd dddd dddd	256 (0x0100)
0xC8BE VAR(0x12,0x00BE)	cam1_aet_ext_gain_setup_0	dddd dddd dddd dddd	0 (0x0000)
0xC8CE VAR(0x12,0x00CE)	cam1_awb_ccm_l_0	dddd dddd dddd dddd	473 (0x01D9)
0xC8D0 VAR(0x12,0x00D0)	cam1_awb_ccm_l_1	dddd dddd dddd dddd	65285 (0xFF05)
0xC8D2 VAR(0x12,0x00D2)	cam1_awb_ccm_l_2	dddd dddd dddd dddd	63 (0x003F)
0xC8D4 VAR(0x12,0x00D4)	cam1_awb_ccm_l_3	dddd dddd dddd dddd	65475 (0xFFC3)
0xC8D6 VAR(0x12,0x00D6)	cam1_awb_ccm_l_4	dddd dddd dddd dddd	306 (0x0132)
0xC8D8 VAR(0x12,0x00D8)	cam1_awb_ccm_l_5	dddd dddd dddd dddd	39 (0x0027)
0xC8DA VAR(0x12,0x00DA)	cam1_awb_ccm_l_6	dddd dddd dddd dddd	65461 (0xFFB5)
0xC8DC VAR(0x12,0x00DC)	cam1_awb_ccm_l_7	dddd dddd dddd dddd	65188 (0xFEA4)
0xC8DE VAR(0x12,0x00DE)	cam1_awb_ccm_l_8	dddd dddd dddd dddd	706 (0x02C2)
0xC8E0 VAR(0x12,0x00E0)	cam1_awb_ccm_l_9	dddd dddd dddd dddd	17 (0x0011)
0xC8E2 VAR(0x12,0x00E2)	cam1_awb_ccm_l_10	dddd dddd dddd dddd	82 (0x0052)
0xC8E4 VAR(0x12,0x00E4)	cam1_awb_ccm_rl_0	dddd dddd dddd dddd	65423 (0xFF8F)

Table 16: 18: Cam1Control Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC8E6 VAR(0x12,0x00E6)	cam1_awb_ccm_rl_1	dddd dddd dddd dddd	168 (0x00A8)
0xC8E8 VAR(0x12,0x00E8)	cam1_awb_ccm_rl_2	dddd dddd dddd dddd	65480 (0xFFC8)
0xC8EA VAR(0x12,0x00EA)	cam1_awb_ccm_rl_3	dddd dddd dddd dddd	18 (0x0012)
0xC8EC VAR(0x12,0x00EC)	cam1_awb_ccm_rl_4	dddd dddd dddd dddd	15 (0x000F)
0xC8EE VAR(0x12,0x00EE)	cam1_awb_ccm_rl_5	dddd dddd dddd dddd	65502 (0xFFDE)
0xC8F0 VAR(0x12,0x00F0)	cam1_awb_ccm_rl_6	dddd dddd dddd dddd	84 (0x0054)
0xC8F2 VAR(0x12,0x00F2)	cam1_awb_ccm_rl_7	dddd dddd dddd dddd	160 (0x00A0)
0xC8F4 VAR(0x12,0x00F4)	cam1_awb_ccm_rl_8	dddd dddd dddd dddd	65290 (0xFF0A)
0xC8F6 VAR(0x12,0x00F6)	cam1_awb_ccm_rl_9	dddd dddd dddd dddd	17 (0x0011)
0xC8F8 VAR(0x12,0x00F8)	cam1_awb_ccm_rl_10	dddd dddd dddd dddd	65492 (0xFFD4)
0xC8FA VAR(0x12,0x00FA)	cam1_awb_ll_ccm_0	dddd dddd dddd dddd	77 (0x004D)
0xC8FC VAR(0x12,0x00FC)	cam1_awb_ll_ccm_1	dddd dddd dddd dddd	150 (0x0096)
0xC8FE VAR(0x12,0x00FE)	cam1_awb_ll_ccm_2	dddd dddd dddd dddd	29 (0x001D)
0xC900 VAR(0x12,0x0100)	cam1_awb_ll_ccm_3	dddd dddd dddd dddd	77 (0x004D)
0xC902 VAR(0x12,0x0102)	cam1_awb_ll_ccm_4	dddd dddd dddd dddd	150 (0x0096)
0xC904 VAR(0x12,0x0104)	cam1_awb_ll_ccm_5	dddd dddd dddd dddd	29 (0x001D)
0xC906 VAR(0x12,0x0106)	cam1_awb_ll_ccm_6	dddd dddd dddd dddd	77 (0x004D)
0xC908 VAR(0x12,0x0108)	cam1_awb_ll_ccm_7	dddd dddd dddd dddd	150 (0x0096)
0xC90A VAR(0x12,0x010A)	cam1_awb_ll_ccm_8	dddd dddd dddd dddd	29 (0x001D)
0xC90C VAR(0x12,0x010C)	cam1_awb_ccmposition_min	dddd dddd dddd dddd	0 (0x0000)
0xC90E VAR(0x12,0x010E)	cam1_awb_ccmposition_max	dddd dddd dddd dddd	127 (0x007F)
0xC910 VAR(0x12,0x0110)	cam1_awb_awb_xscale	dddd dddd dddd dddd	3 (0x0003)
0xC912 VAR(0x12,0x0112)	cam1_awb_awb_yscale	dddd dddd dddd dddd	2 (0x0002)
0xC914 VAR(0x12,0x0114)	cam1_awb_awb_weights_0	dddd dddd dddd dddd	18627 (0x48C3)

Table 16: 18: Cam1Control Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC916 VAR(0x12,0x0116)	cam1_awb_awb_weights_1	dddd dddd dddd dddd	60589 (0xECAD)
0xC918 VAR(0x12,0x0118)	cam1_awb_awb_weights_2	dddd dddd dddd dddd	65431 (0xFF97)
0xC91A VAR(0x12,0x011A)	cam1_awb_awb_weights_3	dddd dddd dddd dddd	6301 (0x189D)
0xC91C VAR(0x12,0x011C)	cam1_awb_awb_weights_4	dddd dddd dddd dddd	37123 (0x9103)
0xC91E VAR(0x12,0x011E)	cam1_awb_awb_weights_5	dddd dddd dddd dddd	45054 (0xAFFE)
0xC920 VAR(0x12,0x0120)	cam1_awb_awb_weights_6	dddd dddd dddd dddd	16431 (0x402F)
0xC922 VAR(0x12,0x0122)	cam1_awb_awb_weights_7	dddd dddd dddd dddd	0 (0x0000)
0xC924 VAR(0x12,0x0124)	cam1_awb_awb_xshift_pre_adj	dddd dddd dddd dddd	58 (0x003A)
0xC926 VAR(0x12,0x0126)	cam1_awb_awb_yshift_pre_adj	dddd dddd dddd dddd	58 (0x003A)
0xC928 VAR(0x12,0x0128)	cam1_stat_luma_thresh_low	dddd dddd dddd dddd	16 (0x0010)
0xC92A VAR(0x12,0x012A)	cam1_stat_luma_thresh_high	dddd dddd dddd dddd	240 (0x00F0)
0xC92C VAR(0x12,0x012C)	cam1_stat_gain_metric_predivider	dddd dddd dddd dddd	17 (0x0011)
0xC92E VAR(0x12,0x012E)	cam1_stat_brightness_metric_predivider	dddd dddd dddd dddd	10 (0x000A)
0xC930 VAR(0x12,0x0130)	cam1_ll_start_brightness	dddd dddd dddd dddd	40 (0x0028)
0xC932 VAR(0x12,0x0132)	cam1_ll_stop_brightness	dddd dddd dddd dddd	200 (0x00C8)
0xC934 VAR(0x12,0x0134)	cam1_ll_start_saturation	dddd dddd dddd dddd	128 (0x0080)
0xC936 VAR(0x12,0x0136)	cam1_ll_end_saturation	dddd dddd dddd dddd	48 (0x0030)
0xC93C VAR(0x12,0x013C)	cam1_ll_ll_start_0	dddd dddd dddd dddd	8 (0x0008)
0xC93E VAR(0x12,0x013E)	cam1_ll_ll_start_1	dddd dddd dddd dddd	2 (0x0002)
0xC940 VAR(0x12,0x0140)	cam1_ll_ll_start_2	dddd dddd dddd dddd	2 (0x0002)
0xC942 VAR(0x12,0x0142)	cam1_ll_ll_stop_0	dddd dddd dddd dddd	104 (0x0068)
0xC944 VAR(0x12,0x0144)	cam1_ll_ll_stop_1	dddd dddd dddd dddd	1 (0x0001)
0xC946 VAR(0x12,0x0146)	cam1_ll_ll_stop_2	dddd dddd dddd dddd	9 (0x0009)
0xC948 VAR(0x12,0x0148)	cam1_ll_nr_start_0	dddd dddd dddd dddd	12 (0x000C)

Table 16: 18: Cam1Control Variable List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xC94A VAR(0x12,0x014A)	cam1_ll_nr_start_1	dddd dddd dddd dddd	12 (0x000C)
0xC94C VAR(0x12,0x014C)	cam1_ll_nr_start_2	dddd dddd dddd dddd	12 (0x000C)
0xC94E VAR(0x12,0x014E)	cam1_ll_nr_start_3	dddd dddd dddd dddd	12 (0x000C)
0xC950 VAR(0x12,0x0150)	cam1_ll_nr_stop_0	dddd dddd dddd dddd	40 (0x0028)
0xC952 VAR(0x12,0x0152)	cam1_ll_nr_stop_1	dddd dddd dddd dddd	40 (0x0028)
0xC954 VAR(0x12,0x0154)	cam1_ll_nr_stop_2	dddd dddd dddd dddd	40 (0x0028)
0xC956 VAR(0x12,0x0156)	cam1_ll_nr_stop_3	dddd dddd dddd dddd	40 (0x0028)
0xC958 VAR(0x12,0x0158)	cam1_ll_start_gamma_bm	dddd dddd dddd dddd	40 (0x0028)
0xC95A VAR(0x12,0x015A)	cam1_ll_stop_gamma_bm	dddd dddd dddd dddd	200 (0x00C8)
0xC95C VAR(0x12,0x015C)	cam1_ll_start_gain_metric	dddd dddd dddd dddd	150 (0x0096)
0xC95E VAR(0x12,0x015E)	cam1_ll_stop_gain_metric	dddd dddd dddd dddd	250 (0x00FA)
0xC960 VAR(0x12,0x0160)	cam1_ll_x0	dddd dddd dddd dddd	64 (0x0040)
0xC962 VAR(0x12,0x0162)	cam1_ll_k_r_l	dddd dddd dddd dddd	128 (0x0080)
0xC964 VAR(0x12,0x0164)	cam1_ll_k_g_l	dddd dddd dddd dddd	128 (0x0080)
0xC966 VAR(0x12,0x0166)	cam1_ll_k_b_l	dddd dddd dddd dddd	128 (0x0080)
0xC968 VAR(0x12,0x0168)	cam1_ll_k_r_r	dddd dddd dddd dddd	128 (0x0080)
0xC96A VAR(0x12,0x016A)	cam1_ll_k_g_r	dddd dddd dddd dddd	128 (0x0080)
0xC96C VAR(0x12,0x016C)	cam1_ll_k_b_r	dddd dddd dddd dddd	128 (0x0080)
0xC96E VAR(0x12,0x016E)	cam1_sys_uv_color_boost	dddd dddd dddd dddd	3 (0x0003)

SysCtrl Variable List

Table 17: 23: SysCtrl Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xDC28 VAR(0x17,0x0028)	sys_refresh_mask	dddd dddd dddd dddd	0 (0x0000)

Comand Handler Variable List

Table 18: 31: Command Handler Variable List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Variable	Name	Data Format (Binary)	Default Value Dec(Hex)
0xFC00 VAR(0x1F,0x0000)	cmd_handler_params_pool_0	dddd dddd dddd dddd	0 (0x0000)
0xFC02 VAR(0x1F,0x0002)	cmd_handler_params_pool_1	dddd dddd dddd dddd	0 (0x0000)
0xFC04 VAR(0x1F,0x0004)	cmd_handler_params_pool_2	dddd dddd dddd dddd	0 (0x0000)
0xFC06 VAR(0x1F,0x0006)	cmd_handler_params_pool_3	dddd dddd dddd dddd	0 (0x0000)
0xFC08 VAR(0x1F,0x0008)	cmd_handler_params_pool_4	dddd dddd dddd dddd	0 (0x0000)
0xFC0A VAR(0x1F,0x000A)	cmd_handler_params_pool_5	dddd dddd dddd dddd	0 (0x0000)
0xFC0C VAR(0x1F,0x000C)	cmd_handler_params_pool_6	dddd dddd dddd dddd	0 (0x0000)
0xFC0E VAR(0x1F,0x000E)	cmd_handler_params_pool_7	dddd dddd dddd dddd	0 (0x0000)

Register Descriptions

Core Register Descriptions

Table 19: 0: Core RegisterDescriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12288 R0x3000	15:0	0x2281	model_id_ (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].				
12290 R0x3002	15:0	0x000C	y_addr_start_ (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. This value must be even.				
12292 R0x3004	15:0	0x0010	x_addr_start_ (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. This value must be even.				
12294 R0x3006	15:0	0x01F3	y_addr_end_ (R/W)	Y	YM
	The last row of visible pixels to be read out. This value must be odd.				
12296 R0x3008	15:0	0x0297	x_addr_end_ (R/W)	Y	N
	The last column of visible pixels to be read out. This value must be odd.				
12298 R0x300A	15:0	0x020D	frame_length_lines_ (R/W)	Y	YM
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines.				
12300 R0x300C	15:0	0x035A	line_length_pck_ (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time.				
12304 R0x3010	15:0	0x0031	fine_correction (R/W)	N	Y
	Fine integration time correction factor. This is an offset that is applied to the programmed value of fine_integration_time such that the actual integration time matches the integration time equation. This register should not be modified under normal operation.				
12306 R0x3012	15:0	0x0010	coarse_integration_time_ (R/W)	Y	N
	Integration time specified in multiples of line_length_pck_.				
12308 R0x3014	15:0	0x00A4	fine_integration_time_ (R/W)	Y	N
	Integration time specified as a number of pixel clocks.				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12314 R0x301A	15:0	0x10D8	reset_register (R/W)		
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0001	Reserved		
	11	X	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	reset_register_gpi_en 0 = the primary input buffers associated with the GPI0 and GPI1 inputs are powered down and the GPI cannot be used. 1 = the input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0001	reset_register_parallel_en For sensors with parallel output, this bit acts as the parallel enable.	N	N
	6	0x0001	reset_register_drive_pins For sensors with parallel output, this bit acts as the drive pins control.	N	N
	5	0x0000	reset_register_reg_rd_en Enable signal to allow read from fuse ID registers.	N	N
	4	0x0001	reset_register_stdby_eof 0 = Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1 = Transition to standby is synchronized to the end of a frame.	N	Y
	3	0x0001	reset_register_lock_reg Many SMIA registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	reset_register_stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N
	1	0x0000	reset_register_restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row (if Standby EOF =0) or at the end of the current frame (if Standby EOF = 1) and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time. A consequence of setting this bit is that the frame-to-frame delay may be shorter than the value programmed in frame_length_lines.	N	Y
	0	0x0000	reset_register_reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y
12318 R0x301E	15:0	0x002A	data_pedestal_ (R/W)	N	Y
	Constant offset that is added to the ADC output for all visible pixels in order to set the black level to a value greater than 0. Read-only. Can be made read/write by clearing R0x301A-B[3].				
12320 R0x3020	15:0	0x0000	software_reset_ (R/W)	N	Y
	This bit is an alias of R0x301A-B[0].				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12322 R0x3022	15:0	0x0000	grouped_parameter_hold_ (R/W)		
	15:9	X	Reserved		
	8	0x0000	alias_grouped_parameter_hold_ This bit is an alias of R0x301A-B[15].	N	N
	7:1	X	Reserved		
	0	0x0000	mask_corrupted_frames_ This bit is an alias of R0x301A-B[9].	N	N
	This bit is an alias of R0x301A-B[9].				
12324 R0x3024	15:0	0x0000	pixel_order_ (RO)	N	N
	00 = First row is GreenR/Red, first pixel is GreenR 01 = First row is GreenR/Red, first pixel is Red 02 = First row is Blue/GreenB, first pixel is Blue 03 = First row is Blue/GreenB, first pixel is GreenB The value in this register changes as a function of R0x3040-1[1:0].				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12326 R0x3026	15:0	0xFC7F	gpi_status (R/W)		
	15:13	0x0007	gpi_status_standby_pin_select Associate the standby function with an active-high input pin 0 = associate with GPI0 1 = associate with GPI1 2-6= RESERVED 7 = standby function cannot be controlled by any pin Must be set to 7 if R0x301A-B[8]=0.	N	N
	12:10	0x0007	gpi_status_oe_n_pin_select Associate the output-enable function with an active-low input pin 0 = associate with GPI0 1 = associate with GPI1 2-6 = RESERVED 7 = output-enable function is not controlled by any pin Must be set to 7 if R0x301A-B[8]=0.	N	N
	9:7	X	Reserved		
	6:4	0x0007	gpi_status_saddr_pin_select Associate the SADDR function with an active-high input pin 0 = associate with GPI0 1 = associate with GPI1 2 = associate with GPI2 3 = associate with GPI3 4-6 = RESERVED 7 = SADDR function is not controlled by any pin Must be set to 7 if R0x301A-B[8]=0.	N	N
	3	RO	gpi_status_gpi3 Read-only. Return the current state of the GPI3 input pin. Invalid if Reg0x301A-B[8]=0.	N	N
	2	RO	gpi_status_gpi2 Read-only. Return the current state of the GPI2 input pin. Invalid if Reg0x301A-B[8]=0.	N	N
	1	RO	gpi_status_gpi1 Read-only. Return the current state of the GPI1 input pin. Invalid if Reg0x301A-B[8]=0.	N	N
	0	RO	gpi_status_gpi0 Read-only. Return the current state of the GPI0 input pin. Invalid if R0x301A-B[8]=0.	N	N
12338 R0x3032	15:0	0x0100	digital_gain_greenr_ (R/W)	Y	N
	Digital gain applied to green pixels on red/green rows of the pixel array. The value is an unsigned 8.8 fixed-point format. Bits [10:8] are significant and are an alias of R0x3056-7[11:9].				
12340 R0x3034	15:0	0x0100	digital_gain_red_ (R/W)	Y	N
	Digital gain applied to red pixels of the pixel array. The value is an unsigned 8.8 fixed-point format. Bits [10:8] are significant and are an alias of R0x305A-B[11:9].				
12342 R0x3036	15:0	0x0100	digital_gain_blue_ (R/W)	Y	N
	Digital gain applied to blue pixels of the pixel array. The value is an unsigned 8.8 fixed-point format. Bits [10:8] are significant and are an alias of R0x3058-9[11:9].				
12344 R0x3038	15:0	0x0100	digital_gain_greenb_ (R/W)	Y	N
	Digital gain applied to green pixels on blue/green rows of the pixel array. The value is an unsigned 8.8 fixed-point format. Bits [10:8] are significant and are an alias of R0x305C-D[11:9].				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12348 R0x303C	15:0	0x0000	frame_status (RO)		
	15:2	X	Reserved		
	1	RO	frame_status_standby This bit tells you whether the sensor is in standby state. When the mode_select register has been written with 0 (enter standby system state), it takes a finite time for the sensor to actually enter the standby system state - upto one row time or one frame time, depending upon the state of bit R0x301A-B[4]. This bit can be polled to determine when the transition to the standby state has actually occurred.	N	N
	0	RO	frame_status_framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N
12352 R0x3040	15:0	0x0041	read_mode (R/W)		
	15	0x0000	read_mode_vert_flip 0 = Normal readout 1 = Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Setting this bit will change the bayer pixel order (see R0x3024).	Y	YM
	14	0x0000	read_mode_horiz_mirror 0 = Normal readout 1 = Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the bayer pixel order (see R0x3024).	Y	YM
	13:12	X	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8:6	0x0001	read_mode_x_odd_inc Increment applied to odd addresses in X (column) direction. 1= Normal readout 3 = Read out alternate pixel pairs to halve the amount of horizontal data in a frame.	Y	YM
	5:0	0x0001	read_mode_y_odd_inc Increment applied to odd addresses in Y (row) direction. 1= Normal readout 3 = Read out alternate pixel pairs to halve the amount of vertical data in a frame.	Y	YM
12374 R0x3056	15:0	0x1030	green1_gain (R/W)		
	15	X	Reserved		
	14:12	0x0001	green1_gain_digital_gain Digital Gain. Legal values 1-7.	Y	N
	11:8	X	Reserved		
	7:6	0x0000	green1_gain_analog_gain If bits[7:6]=N, then analog gain = (2^N) * initial gain.	Y	N
	5:0	0x0030	green1_gain_initial_gain Initial gain = bits [5:0] * 1/32.	Y	N
	Default value corresponds to a digital gain of 1x and an analogue gain of 1.5x.				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12376 R0x3058	15:0	0x1030	blue_gain (R/W)		
	15	X	Reserved		
	14:12	0x0001	blue_gain_digital_gain Digital Gain. Legal values 1-7.	Y	N
	11:8	X	Reserved		
	7:6	0x0000	blue_gain_analog_gain If bits[7:6]=N, then analog gain = (2^N) * initial gain.	Y	N
	5:0	0x0030	blue_gain_initial_gain Initial gain = bits [5:0] * 1/32.	Y	N
	Default value corresponds to a digital gain of 1x and an analogue gain of 1.5x.				
12378 R0x305A	15:0	0x1030	red_gain (R/W)		
	15	X	Reserved		
	14:12	0x0001	red_gain_digital_gain Digital Gain. Legal values 1-7.	Y	N
	11:8	X	Reserved		
	7:6	0x0000	red_gain_analog_gain If bits[7:6]=N, then analog gain = (2^N) * initial gain.	Y	N
	5:0	0x0030	red_gain_initial_gain Initial gain = bits [5:0] * 1/32.	Y	N
	Default value corresponds to a digital gain of 1x and an analogue gain of 1.5x.				
12380 R0x305C	15:0	0x1030	green2_gain (R/W)		
	15	X	Reserved		
	14:12	0x0001	green2_gain_digital_gain Digital Gain. Legal values 1-7.	Y	N
	11:8	X	Reserved		
	7:6	0x0000	green2_gain_analog_gain If bits[7:6]=N, then analog gain = (2^N) * initial gain.	Y	N
	5:0	0x0030	green2_gain_initial_gain Initial gain = bits [5:0] * 1/32.	Y	N
	Default value corresponds to a digital gain of 1x and an analogue gain of 1.5x.				
12382 R0x305E	15:0	0x1030	global_gain (R/W)		
	15	X	Reserved		
	14:12	0x0001	global_gain_digital_gain Digital Gain. Legal values 1-7.	Y	N
	11:8	X	Reserved		
	7:6	0x0000	global_gain_analog_gain If bits[7:6]=N, then analog gain = (2^N) * initial gain.	Y	N
	5:0	0x0030	global_gain_initial_gain Initial gain = bits [5:0] * 1/32.	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.				

Table 19: 0: Core RegisterDescriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12400 R0x3070	15:0	0x0000	test_pattern_mode_ (R/W)	N	Y
	0 = Normal operation: Generate output data from pixel array 1 = Solid color test pattern. 2 = 100% color bar test pattern 3 = Fade to grey color bar test pattern 4 = PN9 Link integrity test pattern 256 = Marching 1's test pattern (10 bit) 257 = Marching 1's test pattern (8 bit) other = Reserved.				
12402 R0x3072	15:0	0x0000	test_data_red_ (R/W)	N	Y
	The value for red pixels in the bayer data used for the solid color test pattern and the test cursors.				
12404 R0x3074	15:0	0x0000	test_data_greenr_ (R/W)	N	Y
	The value for green pixels in red/green rows of the bayer data used for the solid color test pattern and the test cursors.				
12406 R0x3076	15:0	0x0000	test_data_blue_ (R/W)	N	Y
	The value for blue pixels in the bayer data used for the solid color test pattern and the test cursors.				
12408 R0x3078	15:0	0x0000	test_data_greenb_ (R/W)	N	Y
	The value for green pixels in blue/green rows of the bayer data used for the solid color test pattern and the test cursors.				
12448 R0x30A0	15:0	0x0001	x_even_inc_ (RO)	N	N
	Read-only.				
12450 R0x30A2	15:0	0x0001	x_odd_inc_ (R/W)	Y	YM
	This register field is an alias of R0x3040-1[7:5]				
12452 R0x30A4	15:0	0x0001	y_even_inc_ (RO)	N	N
	Read-only.				
12454 R0x30A6	15:0	0x0001	y_odd_inc_ (R/W)	Y	YM
	This register field is an alias of R0x3040-1[4:2]				
12788 R0x31F4	15:0	0x0000	fuse_id1 (R/W)	N	N
	Bits 15:0 of the fused chip ID. Read protected. Set reset_register[5] to get read access to register. Read/Write (the programmed value can be over-written and will be restored on reset)				
12790 R0x31F6	15:0	0x0000	fuse_id2 (R/W)	N	N
	Bits 31:16 of the fused chip ID. Read protected. Set reset_register[5] to get read access to register. Read/Write (the programmed value can be over-written and will be restored on reset)				
12792 R0x31F8	15:0	0x0000	fuse_id3 (R/W)	N	N
	Bits 47:32 of the fused chip ID. Read protected. Set reset_register[5] to get read access to register. Read/Write (the programmed value can be over-written and will be restored on reset)				
12794 R0x31FA	15:0	0x0000	fuse_id4 (R/W)	N	N
	Bits 63:48 of the fused chip ID. Read protected. Set reset_register[5] to get read access to register. Read/Write (the programmed value can be over-written and will be restored on reset)				

1: SOC1 Register Descriptions

Table 20: 1: SOC1 Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
12816 R0x3210	15:0	0x00B0	color_pipeline_control (R/W)
	15:11	X	Reserved
	10	0x0000	Reserved
	9:8	X	Reserved
	7	0x0001	gamma_en Enable gamma correction. 1= enable gamma correction. 0=disable gamma_correction
	6	X	Reserved
	5	0x0001	en_ccm Enable color correction
	4	0x0001	en_ap enable 2D aperture correction
	3	0x0000	pga_enable Enable pixel shading correction. All coefficients and other configuration settings (including other fields in this register) must be set up before enabling shading correction. Internal use only.
	2:0	X	Reserved
12884 R0x3254	15:0	0x0000	first_color (R/W)
	Color of first pixel into colorpipe. 0: G1 1: R 2: B 3: G2 Legal values: [0, 3].		
12908 R0x326C	15:0	0x1208	aperture_parameters_2d (R/W)
	15	X	Reserved
	14	0x0000	ap_abs force aperture gain be positive, if set to 1
	13:11	0x0002	ap_gain_exp 2D aperture gain's exponent Legal values: [0, 7].
	10:8	0x0002	ap_gain_mant 2D aperture gain Legal values: [0, 7].
	7:0	0x0008	ap_knee 2D aperture threshold Legal values: [0, 255].

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
12910 R0x326E	15:0	0x0080	low_pass_yuv_filter (R/W)
	15:8	X	Reserved
	7	0x0001	en_dis B/W filter enable switch
	6	0x0000	th_mode switch for adaptive Y filter threshold
	5	0x0000	eny_i2c enable y permanently
	4:3	0x0000	y_mode y filter mode 0- no filter 1- median 3 2- median 5 Legal values: [0, 2].
	2:0	0x0000	uv_mode uv filter mode 0- no filter 1- use 11110 as filter weight 2- use 01100 as filter weight 3- use 01210 as filter weight 4- use 12221 as filter weight 5- use median 3 6- use median 5 Legal values: [0, 6].
12912 R0x3270	15:0	0x07AA	threshold_for_y_filter_r_channel (R/W)
	15:12	X	Reserved
	11:7	0x000F	u_th U threshold Legal values: [0, 31].
	6:0	0x002A	r_th Y Filter_R channel 4:0- threshold value for R channel 5- if set to 1, enable control signal for R channel 6- if set to 1, invert control signal for R channel Legal values: [0, 127].
12914 R0x3272	15:0	0x07E4	threshold_for_y_filter_g_channel (R/W)
	15:12	X	Reserved
	11:7	0x000F	v_th V threshold Legal values: [0, 31].
	6:0	0x0064	g_th Y Filter_G channel 4:0- threshold value for G channel 5- if set to 1, enable control signal for G channel 6- if set to 1, invert control signal for G channel Legal values: [0, 127].

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
12916 R0x3274	15:0	0x002A	threshold_for_y_filter_b_channel (R/W)
	15:7	X	Reserved
	6:0	0x002A	b_th Y Filter_B channel 4:0- threshold value for B channel 5- if set to 1, enable control signal for B channel 6- if set to 1, invert control signal for B channel Legal values: [0, 127].
12918 R0x3276	15:0	0x0000	black_level_to_ccm (R/W)
	Second Black Level prior to CCM Legal values: [0, 1023].		
12922 R0x327A	15:0	0x00A8	red_offset (R/W)
	Offset subtracted from red pixels. This register contains the value for Red pixels subtracted by IFP from raw pixel values before applying lens shading correction and digital gains. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. Typically, the subtracted value should be equal to the black level targeted by the sensor. This value is subtracted from all test patterns as well. Legal values: [0, 511].		
12924 R0x327C	15:0	0x00A8	green1_offset (R/W)
	Offset subtracted from green1 pixels. This register contains the value for Green1 pixels subtracted by IFP from raw pixel values before applying lens shading correction and digital gains. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. Typically, the subtracted value should be equal to the black level targeted by the sensor. This value is subtracted from all test patterns as well. Legal values: [0, 511].		
12926 R0x327E	15:0	0x00A8	green2_offset (R/W)
	Offset subtracted from green2 pixels. This register contains the value for Green2 pixels subtracted by IFP from raw pixel values before applying lens shading correction and digital gains. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. Typically, the subtracted value should be equal to the black level targeted by the sensor. This value is subtracted from all test patterns as well. Legal values: [0, 511].		
12928 R0x3280	15:0	0x00A8	blue_offset (R/W)
	Offset subtracted from blue pixels. This register contains the value for Blue pixels subtracted by IFP from raw pixel values before applying lens shading correction and digital gains. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. Typically, the subtracted value should be equal to the black level targeted by the sensor. This value is subtracted from all test patterns as well. Legal values: [0, 511].		
12986 R0x32BA	15:0	0x0000	red_offset_to_ccm (R/W)
	Red offset, Signed value with 8-bit integer and 2-bit fractional Legal values: [-512, 511].		
12988 R0x32BC	15:0	0x0000	green_offset_to_ccm (R/W)
	Green offset, Signed value with 8-bit integer and 2-bit fractional Legal values: [-512, 511].		
12990 R0x32BE	15:0	0x0000	blue_offset_to_ccm (R/W)
	Blue offset, Signed value with 8-bit integer and 2-bit fractional Legal values: [-512, 511].		

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
12992 R0x32C0	15:0	0x3923	ccm_exp_low_byte (R/W)
	15	X	Reserved
	14:12	0x0003	ccm_cc5_exp CCM Exponent for CC5 Legal values: [0, 4].
	11:9	0x0004	ccm_cc4_exp CCM Exponent for CC4 Legal values: [0, 4].
	8:6	0x0004	ccm_cc3_exp CCM Exponent for CC3 Legal values: [0, 4].
	5:3	0x0004	ccm_cc2_exp CCM Exponent for CC2 Legal values: [0, 4].
	2:0	0x0003	ccm_cc1_exp CCM Exponent for CC1 Legal values: [0, 4].
12994 R0x32C2	15:0	0x0724	ccm_exp_high_byte (R/W)
	15:12	X	Reserved
	11:9	0x0003	ccm_cc9_exp CCM Exponent for CC9 Legal values: [0, 4].
	8:6	0x0004	ccm_cc8_exp CCM Exponent for CC8 Legal values: [0, 4].
	5:3	0x0004	ccm_cc7_exp CCM Exponent for CC7 Legal values: [0, 4].
	2:0	0x0004	ccm_cc6_exp CCM Exponent for CC6 Legal values: [0, 4].
12996 R0x32C4	15:0	0xD9EE	ccm_elements_1_and_2 (R/W)
	15:8	0x00D9	ccm_cc2 CCM Elements 2 (C12) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
	7:0	0x00EE	ccm_cc1 CCM Elements 1 (C11) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
12998 R0x32C6	15:0	0x2B1B	ccm_elements_3_and_4 (R/W)
	15:8	0x002B	ccm_cc4 CCM Elements 4 (C21) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
	7:0	0x001B	ccm_cc3 CCM Elements 3 (C13) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13000 R0x32C8	15:0	0x8BEA	ccm_elements_5_and_6 (R/W)
	15:8	0x008B	ccm_cc6 CCM Elements 6 (C23) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
	7:0	0x00EA	ccm_cc5 CCM Elements 5 (C22) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
13002 R0x32CA	15:0	0x7D16	ccm_elements_7_and_8 (R/W)
	15:8	0x007D	ccm_cc8 CCM Elements 8 (C32) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
	7:0	0x0016	ccm_cc7 CCM Elements 7 (C31) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].
13004 R0x32CC	15:0	0x2DC2	ccm_elements_9_and_signs (R/W)
	15:14	X	Reserved
	13	0x0001	ccm_cc8_sign Sign for CCM CC8
	12	0x0000	ccm_cc7_sign Sign for CCM CC7
	11	0x0001	ccm_cc6_sign Sign for CCM CC6
	10	0x0001	ccm_cc4_sign Sign for CCM CC4
	9	0x0000	ccm_cc3_sign Sign for CCM CC3
	8	0x0001	ccm_cc2_sign Sign for CCM CC2
	7:0	0x00C2	ccm_cc9 CCM Elements 9 (C33) C(i,j) = Sign(i,j) * Mantissa(i,j) * 2^ -(Exp(i,j) + 2) Legal values: [0, 255].

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13102 R0x332E	15:0	0x0000	output_format_configuration (R/W)
	15:11	X	Reserved
	10:9	0x0000	fm_proc_bayer_first_color Processed bayer output first color (0:Gr, 1:R, 2:B, 3:Gb) 00 = Green1 01 = Red 10 = Blue 11 = Green2 Legal values: [0, 3].
	8:7	0x0000	fm_rgb_type RGB output format (0:565, 1:555, 2:444x, 3:x444) 00 = 16-bit RGB565 01 = 15-bit RGB555 10 = 12-bit RGB444x 11 = 12-bit RGBx444 Legal values: [0, 3].
	6:5	0x0000	fm_output_format Selects output format (0: YUV, 1: RGB, 2: Pbayer) 00 = YUV 01 = RGB 10 = Processed Bayer Legal values: [0, 2].
	4:3	0x0000	fm_yuv_sampling_mode Select sampling mode for YUV422 (0: even UV, 1: odd UV, 2: even U odd V) 00 = Use even columns for U and V 01 = Use odd columns for U and V 02 = Use current column for U and V Legal values: [0, 2].
	2	0x0000	fm_mono_enable Enable monochrome output. Causes format to only generate luma information.
	1	0x0000	fm_swap_bytes Swap output pixel hi byte with low byte. In YUV mode, swaps chroma with luma. In RGB mode, swaps odd and even bytes.
	0	0x0000	fm_swap_red_blue Swap R/B or Cr/Cb channels In YUV output mode, swaps Cb and Cr channels. In RGB mode, swaps R and B.
	Output Format Configuration		

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13104 R0x3330	15:0	0x0000	output_format_test (R/W)
	15:12	X	Reserved
	11	0x0000	fm_shift_output When enabled this left shifts the pixel data by 3 bits.
	10:9	X	Reserved
	8	0x0000	fm_pga_bypass_enable Enable lens correction bypass. Take output data from lens correction.
	7	0x0000	freeze Freeze update of R0x332E and SOC size registers 1=freeze update of R0x332E and SOC size registers
	6	X	Reserved
	5:3	0x0000	fm_test_ramp_type Test ramp output (0: Off, 1:Col, 2:Row, 3: Frame) 00 = Off 01 = Column 10 = Row 11 = Frame Legal values: [0, 3].
	2	0x0000	fm_disable_cb Disable Cb/B channel 1=disable Cb channel (B in RGB mode)
	1	0x0000	fm_disable_y Disable Y/G channel 1=disable Y channel (G in RGB mode)
	0	0x0000	fm_disable_cr Disable Cr/R channel 1=disable Cr channel (R in RGB mode)
13106 R0x3332	15:0	0x0000	fm_line_count (RO)
	Current line number. Read-only. Legal values: [0, 4095].		
13108 R0x3334	15:0	0x0000	fm_frame_count (RO)
	Frame count since reset. Counter wraps around at 16-bit boundary. Read-only. Legal values: [0, 65535].		
13180 R0x337C	15:0	0x0006	yuv_ycbcr_control (R/W)
	15:4	X	Reserved
	3	0x0000	fm_clip Clip Y in 16-235; U and V in 16-238
	2	0x0001	fm_auv_offset Add 128 to U and V
	1	0x0001	select_601 coefficient control 0- YUV (BT-709) coefficients 1- YCbCr (BT-601) coefficients
	0	0x0000	fm_normalize Normalize Y in 16-235; U and V in 16-238

Table 20: 1: SOC1 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13182 R0x337E	15:0	0x0000	y_rgb_offset (R/W)
	15:8	0x0000	fm_y_offset Y offset Legal values: [0, 255].
	7:0	0x0000	fm_rgb_offset RGB offset Legal values: [0, 255].
13300 R0x33F4	15:0	0x0003	kernel_config (R/W)
	15:8	X	Reserved
	7	0x0000	Reserved
	6	0x0000	dc_cluster_enable Defect correction cluster defect enable. When set to 1 this bit enables 2D two pixel cluster defect correction. Defect correction must be enabled (dc_enable = 1) for this bit to have any effect. Setting this bit significantly filters the image. This bit should only be set in low light conditions. Legal values: [0,1].
	5	0x0000	nr_force_filter Noise reduction force filter. When set to a 1 forces all eight surrounding pixels to be used during noise reduction, instead of checking for like pixels. This effectively lowers the frequency of the low pass filter. Legal values: [0,1].
	4	X	Reserved
	3	0x0000	nr_enable Noise reduction enable. When set to 1, enable noise reduction algorythm. Legal values: [0,1].
	2	0x0000	dc_matrix_rotate Defect correction matrix rotate. When set to 1, forces defect correction to always use the sqaure pattern, like pixels for defect correction. When set to 0, use square pattern for blue and red pixels but use diamond pattern for green Legal values: [0,1].
	1	0x0001	Reserved
	0	0x0001	dc_enable Defect correction enable. When set to 1, enable 2D single pixel defect correction. Legal values: [0,1].

2: SOC2 Register Descriptions

Table 21: 2: SOC2 Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13888 R0x3640	15:0	0x0010	p_g1_p0q0 (R/W)
	P0 coefficients for Green1. Legal values: [0, 65535].		
13890 R0x3642	15:0	0x0000	p_g1_p0q1 (R/W)
	P0 coefficients for Green1. Legal values: [0, 65535].		
13892 R0x3644	15:0	0x0000	p_g1_p0q2 (R/W)
	P0 coefficients for Green1. Legal values: [0, 65535].		
13894 R0x3646	15:0	0x0000	p_g1_p0q3 (R/W)
	P0 coefficients for Green1. Legal values: [0, 65535].		
13896 R0x3648	15:0	0x0000	p_g1_p0q4 (R/W)
	P0 coefficients for Green1. Legal values: [0, 65535].		
13898 R0x364A	15:0	0x0010	p_r_p0q0 (R/W)
	P0 coefficients for Red. Legal values: [0, 65535].		
13900 R0x364C	15:0	0x0000	p_r_p0q1 (R/W)
	P0 coefficients for Red. Legal values: [0, 65535].		
13902 R0x364E	15:0	0x0000	p_r_p0q2 (R/W)
	P0 coefficients for Red. Legal values: [0, 65535].		
13904 R0x3650	15:0	0x0000	p_r_p0q3 (R/W)
	P0 coefficients for Red. Legal values: [0, 65535].		
13906 R0x3652	15:0	0x0000	p_r_p0q4 (R/W)
	P0 coefficients for Red. Legal values: [0, 65535].		
13908 R0x3654	15:0	0x0010	p_b_p0q0 (R/W)
	P0 coefficients for Blue. Legal values: [0, 65535].		
13910 R0x3656	15:0	0x0000	p_b_p0q1 (R/W)
	P0 coefficients for Blue. Legal values: [0, 65535].		
13912 R0x3658	15:0	0x0000	p_b_p0q2 (R/W)
	P0 coefficients for Blue. Legal values: [0, 65535].		
13914 R0x365A	15:0	0x0000	p_b_p0q3 (R/W)
	P0 coefficients for Blue. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13916 R0x365C	15:0	0x0000	p_b_p0q4 (R/W)
	P0 coefficients for Blue. Legal values: [0, 65535].		
13918 R0x365E	15:0	0x0010	p_g2_p0q0 (R/W)
	P0 coefficients for Green2. Legal values: [0, 65535].		
13920 R0x3660	15:0	0x0000	p_g2_p0q1 (R/W)
	P0 coefficients for Green2. Legal values: [0, 65535].		
13922 R0x3662	15:0	0x0000	p_g2_p0q2 (R/W)
	P0 coefficients for Green2. Legal values: [0, 65535].		
13924 R0x3664	15:0	0x0000	p_g2_p0q3 (R/W)
	P0 coefficients for Green2. Legal values: [0, 65535].		
13926 R0x3666	15:0	0x0000	p_g2_p0q4 (R/W)
	P0 coefficients for Green2. Legal values: [0, 65535].		
13952 R0x3680	15:0	0x0000	p_g1_p1q0 (R/W)
	P1 coefficients for Green1. Legal values: [0, 65535].		
13954 R0x3682	15:0	0x0000	p_g1_p1q1 (R/W)
	P1 coefficients for Green1. Legal values: [0, 65535].		
13956 R0x3684	15:0	0x0000	p_g1_p1q2 (R/W)
	P1 coefficients for Green1. Legal values: [0, 65535].		
13958 R0x3686	15:0	0x0000	p_g1_p1q3 (R/W)
	P1 coefficients for Green1. Legal values: [0, 65535].		
13960 R0x3688	15:0	0x0000	p_g1_p1q4 (R/W)
	P1 coefficients for Green1. Legal values: [0, 65535].		
13962 R0x368A	15:0	0x0000	p_r_p1q0 (R/W)
	P1 coefficients for Red. Legal values: [0, 65535].		
13964 R0x368C	15:0	0x0000	p_r_p1q1 (R/W)
	P1 coefficients for Red. Legal values: [0, 65535].		
13966 R0x368E	15:0	0x0000	p_r_p1q2 (R/W)
	P1 coefficients for Red. Legal values: [0, 65535].		
13968 R0x3690	15:0	0x0000	p_r_p1q3 (R/W)
	P1 coefficients for Red. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
13970 R0x3692	15:0	0x0000	p_r_p1q4 (R/W)
	P1 coefficients for Red. Legal values: [0, 65535].		
13972 R0x3694	15:0	0x0000	p_b_p1q0 (R/W)
	P1 coefficients for Blue. Legal values: [0, 65535].		
13974 R0x3696	15:0	0x0000	p_b_p1q1 (R/W)
	P1 coefficients for Blue. Legal values: [0, 65535].		
13976 R0x3698	15:0	0x0000	p_b_p1q2 (R/W)
	P1 coefficients for Blue. Legal values: [0, 65535].		
13978 R0x369A	15:0	0x0000	p_b_p1q3 (R/W)
	P1 coefficients for Blue. Legal values: [0, 65535].		
13980 R0x369C	15:0	0x0000	p_b_p1q4 (R/W)
	P1 coefficients for Blue. Legal values: [0, 65535].		
13982 R0x369E	15:0	0x0000	p_g2_p1q0 (R/W)
	P1 coefficients for Green2. Legal values: [0, 65535].		
13984 R0x36A0	15:0	0x0000	p_g2_p1q1 (R/W)
	P1 coefficients for Green2. Legal values: [0, 65535].		
13986 R0x36A2	15:0	0x0000	p_g2_p1q2 (R/W)
	P1 coefficients for Green2. Legal values: [0, 65535].		
13988 R0x36A4	15:0	0x0000	p_g2_p1q3 (R/W)
	P1 coefficients for Green2. Legal values: [0, 65535].		
13990 R0x36A6	15:0	0x0000	p_g2_p1q4 (R/W)
	P1 coefficients for Green2. Legal values: [0, 65535].		
14016 R0x36C0	15:0	0x0000	p_g1_p2q0 (R/W)
	P2 coefficients for Green1. Legal values: [0, 65535].		
14018 R0x36C2	15:0	0x0000	p_g1_p2q1 (R/W)
	P2 coefficients for Green1. Legal values: [0, 65535].		
14020 R0x36C4	15:0	0x0000	p_g1_p2q2 (R/W)
	P2 coefficients for Green1. Legal values: [0, 65535].		
14022 R0x36C6	15:0	0x0000	p_g1_p2q3 (R/W)
	P2 coefficients for Green1. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
14024 R0x36C8	15:0	0x0000	p_g1_p2q4 (R/W)
	P2 coefficients for Green1. Legal values: [0, 65535].		
14026 R0x36CA	15:0	0x0000	p_r_p2q0 (R/W)
	P2 coefficients for Red. Legal values: [0, 65535].		
14028 R0x36CC	15:0	0x0000	p_r_p2q1 (R/W)
	P2 coefficients for Red. Legal values: [0, 65535].		
14030 R0x36CE	15:0	0x0000	p_r_p2q2 (R/W)
	P2 coefficients for Red. Legal values: [0, 65535].		
14032 R0x36D0	15:0	0x0000	p_r_p2q3 (R/W)
	P2 coefficients for Red. Legal values: [0, 65535].		
14034 R0x36D2	15:0	0x0000	p_r_p2q4 (R/W)
	P2 coefficients for Red. Legal values: [0, 65535].		
14036 R0x36D4	15:0	0x0000	p_b_p2q0 (R/W)
	P2 coefficients for Blue. Legal values: [0, 65535].		
14038 R0x36D6	15:0	0x0000	p_b_p2q1 (R/W)
	P2 coefficients for Blue. Legal values: [0, 65535].		
14040 R0x36D8	15:0	0x0000	p_b_p2q2 (R/W)
	P2 coefficients for Blue. Legal values: [0, 65535].		
14042 R0x36DA	15:0	0x0000	p_b_p2q3 (R/W)
	P2 coefficients for Blue. Legal values: [0, 65535].		
14044 R0x36DC	15:0	0x0000	p_b_p2q4 (R/W)
	P2 coefficients for Blue. Legal values: [0, 65535].		
14046 R0x36DE	15:0	0x0000	p_g2_p2q0 (R/W)
	P2 coefficients for Green2. Legal values: [0, 65535].		
14048 R0x36E0	15:0	0x0000	p_g2_p2q1 (R/W)
	P2 coefficients for Green2. Legal values: [0, 65535].		
14050 R0x36E2	15:0	0x0000	p_g2_p2q2 (R/W)
	P2 coefficients for Green2. Legal values: [0, 65535].		
14052 R0x36E4	15:0	0x0000	p_g2_p2q3 (R/W)
	P2 coefficients for Green2. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
14054 R0x36E6	15:0	0x0000	p_g2_p2q4 (R/W)
	P2 coefficients for Green2. Legal values: [0, 65535].		
14080 R0x3700	15:0	0x0000	p_g1_p3q0 (R/W)
	P3 coefficients for Green1. Legal values: [0, 65535].		
14082 R0x3702	15:0	0x0000	p_g1_p3q1 (R/W)
	P3 coefficients for Green1. Legal values: [0, 65535].		
14084 R0x3704	15:0	0x0000	p_g1_p3q2 (R/W)
	P3 coefficients for Green1. Legal values: [0, 65535].		
14086 R0x3706	15:0	0x0000	p_g1_p3q3 (R/W)
	P3 coefficients for Green1. Legal values: [0, 65535].		
14088 R0x3708	15:0	0x0000	p_g1_p3q4 (R/W)
	P3 coefficients for Green1. Legal values: [0, 65535].		
14090 R0x370A	15:0	0x0000	p_r_p3q0 (R/W)
	P3 coefficients for Red. Legal values: [0, 65535].		
14092 R0x370C	15:0	0x0000	p_r_p3q1 (R/W)
	P3 coefficients for Red. Legal values: [0, 65535].		
14094 R0x370E	15:0	0x0000	p_r_p3q2 (R/W)
	P3 coefficients for Red. Legal values: [0, 65535].		
14096 R0x3710	15:0	0x0000	p_r_p3q3 (R/W)
	P3 coefficients for Red. Legal values: [0, 65535].		
14098 R0x3712	15:0	0x0000	p_r_p3q4 (R/W)
	P3 coefficients for Red. Legal values: [0, 65535].		
14100 R0x3714	15:0	0x0000	p_b_p3q0 (R/W)
	P3 coefficients for Blue. Legal values: [0, 65535].		
14102 R0x3716	15:0	0x0000	p_b_p3q1 (R/W)
	P3 coefficients for Blue. Legal values: [0, 65535].		
14104 R0x3718	15:0	0x0000	p_b_p3q2 (R/W)
	P3 coefficients for Blue. Legal values: [0, 65535].		
14106 R0x371A	15:0	0x0000	p_b_p3q3 (R/W)
	P3 coefficients for Blue. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
14108 R0x371C	15:0	0x0000	p_b_p3q4 (R/W)
	P3 coefficients for Blue. Legal values: [0, 65535].		
14110 R0x371E	15:0	0x0000	p_g2_p3q0 (R/W)
	P3 coefficients for Green2. Legal values: [0, 65535].		
14112 R0x3720	15:0	0x0000	p_g2_p3q1 (R/W)
	P3 coefficients for Green2. Legal values: [0, 65535].		
14114 R0x3722	15:0	0x0000	p_g2_p3q2 (R/W)
	P3 coefficients for Green2. Legal values: [0, 65535].		
14116 R0x3724	15:0	0x0000	p_g2_p3q3 (R/W)
	P3 coefficients for Green2. Legal values: [0, 65535].		
14118 R0x3726	15:0	0x0000	p_g2_p3q4 (R/W)
	P3 coefficients for Green2. Legal values: [0, 65535].		
14144 R0x3740	15:0	0x0000	p_g1_p4q0 (R/W)
	P4 coefficients for Green1. Legal values: [0, 65535].		
14146 R0x3742	15:0	0x0000	p_g1_p4q1 (R/W)
	P4 coefficients for Green1. Legal values: [0, 65535].		
14148 R0x3744	15:0	0x0000	p_g1_p4q2 (R/W)
	P4 coefficients for Green1. Legal values: [0, 65535].		
14150 R0x3746	15:0	0x0000	p_g1_p4q3 (R/W)
	P4 coefficients for Green1. Legal values: [0, 65535].		
14152 R0x3748	15:0	0x0000	p_g1_p4q4 (R/W)
	P4 coefficients for Green1. Legal values: [0, 65535].		
14154 R0x374A	15:0	0x0000	p_r_p4q0 (R/W)
	P4 coefficients for Red. Legal values: [0, 65535].		
14156 R0x374C	15:0	0x0000	p_r_p4q1 (R/W)
	P4 coefficients for Red. Legal values: [0, 65535].		
14158 R0x374E	15:0	0x0000	p_r_p4q2 (R/W)
	P4 coefficients for Red. Legal values: [0, 65535].		
14160 R0x3750	15:0	0x0000	p_r_p4q3 (R/W)
	P4 coefficients for Red. Legal values: [0, 65535].		

Table 21: 2: SOC2 Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
14162 R0x3752	15:0	0x0000	p_r_p4q4 (R/W)
	P4 coefficients for Red. Legal values: [0, 65535].		
14164 R0x3754	15:0	0x0000	p_b_p4q0 (R/W)
	P4 coefficients for Blue. Legal values: [0, 65535].		
14166 R0x3756	15:0	0x0000	p_b_p4q1 (R/W)
	P4 coefficients for Blue. Legal values: [0, 65535].		
14168 R0x3758	15:0	0x0000	p_b_p4q2 (R/W)
	P4 coefficients for Blue. Legal values: [0, 65535].		
14170 R0x375A	15:0	0x0000	p_b_p4q3 (R/W)
	P4 coefficients for Blue. Legal values: [0, 65535].		
14172 R0x375C	15:0	0x0000	p_b_p4q4 (R/W)
	P4 coefficients for Blue. Legal values: [0, 65535].		
14174 R0x375E	15:0	0x0000	p_g2_p4q0 (R/W)
	P4 coefficients for Green2. Legal values: [0, 65535].		
14176 R0x3760	15:0	0x0000	p_g2_p4q1 (R/W)
	P4 coefficients for Green2. Legal values: [0, 65535].		
14178 R0x3762	15:0	0x0000	p_g2_p4q2 (R/W)
	P4 coefficients for Green2. Legal values: [0, 65535].		
14180 R0x3764	15:0	0x0000	p_g2_p4q3 (R/W)
	P4 coefficients for Green2. Legal values: [0, 65535].		
14182 R0x3766	15:0	0x0000	p_g2_p4q4 (R/W)
	P4 coefficients for Green2. Legal values: [0, 65535].		
14208 R0x3780	15:0	0x0048	pga_control (R/W)
	15:9	X	Reserved
	8:6	0x0001	Reserved
	5:3	0x0001	Reserved
	2	0x0000	pga_flip_v This bit enables the vertical flip of the sensor. 0 = Normal 1 = Vertical Flip
	1	0x0000	pga_mirror_h This bit enables the horizontal mirror of the sensor. 0 = Normal 1 = Horizontal Mirror
	0	X	Reserved

SYSCTL Register Descriptions

Table 22: SYSCTL Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
0 R0x0000	15:0	0x2281	k22b_chip_id (RO)
	k22b/soc356 ident code Read-only.		
16 R0x0010	15:0	0x0212	pll_dividers (R/W)
	15:14	X	Reserved
	13:8	0x0002	n PLL n divider ratio
	7:0	0x0012	m PLL m divider ratio
	PLL dividers for n and m		
18 R0x0012	15:0	0x0000	pll_p_dividers (R/W)
	15:14	X	Reserved
	13:12	0x0000	word_clock_divider PLL word clock divisor
	11:8	0x0000	p3 PLL bit clock divider ratio p1
	7:4	RO	p2 Reserved
	3:0	RO	p1 Reserved
	PLL dividers for p and word clock		

Table 22: SYSCTL Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
20 R0x0014	15:0	0x5846	pll_control (R/W)
	15	RO	pll_lock PLL lock Read-only.
	14	0x0001	clockin_bias_en XTAL pad bias resistor enable
	13	X	Reserved
	12	0x0001	sel_lock_det Select pll_lock to control PLL bypass
	11	0x0001	test_reset PLL reset_tc
	10	0x0000	test_bypass PLL test_bypass
	9	0x0000	clk_mux PLL sel_word_clock
	8	0x0000	reset_cntr PLL counter reset
	7:4	0x0004	pfd PLL pfd tuning control
	3:2	0x0001	lock_mode PLL lock detector mode
	1	0x0001	pll_enable PLL enable
	0	0x0000	pll_bypass Bypass PLL
	PLL Control Status Register		
26 R0x001A	15:0	0x0000	reset_and_misc_control (R/W)
	15	0x0000	en_dbl_buf sel_testp and sel_vsrc not sync'd to fen
	14	0x0000	Reserved
	13:12	0x0000	sel_vsrc LSB selects video sources, 1=testp , 0=sensor. MSB testp enable
	11:1	X	Reserved
	0	0x0000	reset_soc_i2c Soft system reset.
	Miscellaneous Control bits		

Table 22: SYSCTL Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
48 R0x0030	15:0	0x0400	pad_slew (R/W)
	15	X	Reserved
	14:12	0x0000	Reserved
	11	X	Reserved
	10:8	0x0004	slew_pixclk Slew rate control for PIXCLK pad.
	7	X	Reserved
	6:4	0x0000	slew_spi Slew rate control for SPI_SCLK, SPI_SDO, SPI_CS_N pads.
	3	X	Reserved
	2:0	0x0000	slew_dout Slew rate control for FRAME_VALID, LINE_VALID, DOUT7-DOUT0, DOUT_LSB1, DOUT_LSB0 pads.
	Slew rate control for pads		
50 R0x0032	15:0	0x00D1	pad_control (R/W)
	15	0x0000	oe_lsb1_pads Output enable for dout_lsb1 pad (also known as GPIO[3])
	14	0x0000	oe_lsb0_pads Output enable for dout_lsb0 pad (also known as GPIO[2])
	13	0x0000	oe_data_pads Output enable for pixclk and dout[7:0] pads (aka GPO[8:0])
	12	0x0000	oe_fvlv_pads Output enable for frame_valid and line_valid pads (aka GPIO[1:0])
	11:10	X	Reserved
	9	0x0000	oe_spi_pads Output enable for SPI pads
	8	X	Reserved
	7	0x0001	ipd_lsb1_pads Power down for dout_lsb1 pad (also known as GPIO[3])
	6	0x0001	ipd_lsb0_pads Power down for dout_lsb0 pad (also known asGPIO[2])
	5	X	Reserved
	4	0x0001	ipd_fvlv_pads Power down for frame_valid and line_valid pads (aka GPIO[1:0])
	3:1	X	Reserved
	0	0x0001	ipd_din_pads Power down for dinclk and din7-din0 pads (aka GPI[8:0])
	Output Enable and Power Down control for pads		

Table 22: SYSCTL Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
52 R0x0034	15:0	0x0000	pad_gpi_status (RO)
	15:12	RO	gpio_status Status of GPIO[3:0] Read-only.
	11:9	X	Reserved
	8:0	RO	gpi_status Status of GPI[8:0] Read-only.
	GPI status Read-only.		
64 R0x0040	15:0	0x0000	command_register (R/W)
	15	0x0000	doorbell doorbell bit. Set only from I^2C, Set/Clear from ICB
	14:0	0x0000	host_command Host command
	Host Command Register		

XDMA Registers

Table 23: XDMA Registers
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
2434 R0x0982	15:0	0x0000	access_ctl_stat (R/W)
	15:8	X	Reserved
	7:6	0x0000	phy_region 00: Physical access to Patch RAM 01: UNDEFINED 10: Physical access to SFR address space 11: Physical access to Overlay RAM When physical_access_state=11, this field determines which memory region will be accessed. When physical_access_state=10, the Patch RAM is implicitly selected.
	5	X	Reserved
	4	RO	byte_access_state Read-only copy of logical_byte_access (in Logical Access state) or physical_byte_access (in Physical Access state) 1: Byte Access state 0: Word Access state (2 bytes) Read-only.
	3:2	RO	physical_access_state 11: Physical Access state 10: Logical Access state 0x: Indeterminate (DMA address is invalid). The DMA address will be invalid if Logical Access state is established before the tabptr SFR has been initialised. Read-only.
	1	RO	upper_32k_access_state Physical address[15] for current access. In Logical Access state (physical_access_state=10), this bit provides debug information: after at least one data access has been performed, this bit represents the physical address[15] of the variables base for the current driver number. In Physical Access state (physical_access_state=11), this bit is a read-only copy of en_upper_32k_phy_access. Read-only.
	0	0x0000	en_upper_32k_phy_access This bit provides physical address[15] for physical address accesses. physical address[14:0] are provided by R0x098A
	Controls the access and conveys access status		

Table 23: XDMA Registers (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
2442 R0x098A	15:0	0x0000	physical_address_access (R/W)
	15	0x0000	physical_byte_access In Physical Access state the state of this bit affects the behavior of Indirect data accesses (reads and writes to the mcu_variable_dataN registers). This bit has no effect on the behavior of Direct data accesses (reads and writes to I2C addresses above 0x7FFF). 1: Byte Access 0: Word Access (2 bytes)
	14:0	0x0000	physical_address physical_address[14:0] for current access. physical_address[15] is set by R0x0982[0]. Legal values: [0, 32767].
	Address of physical access; Used for Patch RAM uploads. A write to this address establishes the Physical Access state (See R0x0982[2]). When the Logical Access state is established, a read from this register and from R0x0982[1] provides debug information: after at least one data access has been performed, this bit represents the physical address of the variables base for the current driver number.		
2446 R0x098E	15:0	0x0000	logical_address_access (R/W)
	15	0x0000	logical_byte_access In Logical Access state the state of this bit affects the behavior of Indirect data accesses (reads and writes to the mcu_variable_dataN registers). This bit has no effect on the behavior of Direct data accesses (reads and writes to I2C addresses above 0x7FFF). 1: Byte Access 0: Word Access (2 bytes)
	14:10	0x0000	logical_access_drv_num Address of logical access driver number - logical_address[14:10]. Base address of this driver's variables can be obtained by adding 2*logical_access_drv_num to the value of the tabptr SFR. Physical address of re-directed location can be obtained by adding this offset to the SFR 0x50 return value. Legal values: [0, 31].
	9:0	0x0000	logical_access_offset Address of logical access offset - logical_address[9:0]. Physical address can be obtained by adding this offset to the base address of the selected driver's variables (the driver is selected by logical_access_drv_num). Legal values: [0, 1023].
	Address of logical access; Used for camera control (i.e. register/variable updates) by user. A write to this address establishes the Logical Access state (See R0x0982[2]).		
2448 R0x0990	15:0	0x0000	mcu_variable_data0 (R/W)
	DMA word 0 (Indirect data access) Legal values: [0, 65535].		
2450 R0x0992	15:0	0x0000	mcu_variable_data1 (R/W)
	DMA word 1 (Indirect data access) Legal values: [0, 65535].		
2452 R0x0994	15:0	0x0000	mcu_variable_data2 (R/W)
	DMA word 2 (Indirect data access) Legal values: [0, 65535].		
2454 R0x0996	15:0	0x0000	mcu_variable_data3 (R/W)
	DMA word 3 (Indirect data access) Legal values: [0, 65535].		

Table 23: XDMA Registers (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
2456 R0x0998	15:0	0x0000	mcu_variable_data4 (R/W)
	DMA word 4 (Indirect data access) Legal values: [0, 65535].		
2458 R0x099A	15:0	0x0000	mcu_variable_data5 (R/W)
	DMA word 5 (Indirect data access) Legal values: [0, 65535].		
2460 R0x099C	15:0	0x0000	mcu_variable_data6 (R/W)
	DMA word 6 (Indirect data access) Legal values: [0, 65535].		
2462 R0x099E	15:0	0x0000	mcu_variable_data7 (R/W)
	DMA word 7 (Indirect data access) Legal values: [0, 65535].		

TX_SS Register Descriptions

Table 24: TX_SS Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
15360 R0x3C00	15:0	0x1000	parallel_bus_ctrl (R/W)
	15:13	X	Reserved
	12	0x0001	bt656_fvlv_en 0: When outputting bt656 format data (parallel_bus_sel = 5, 6 or 7) gpio_out[1:0] are output on FRAME_VALID and LINE_VALID 1: When outputting bt656 format data (parallel_bus_sel = 5, 6 or 7) frame_ and line_valid strobes are regenerated from the bt656 data and are output on FRAME_VALID and LINE_VALID
	11:9	X	Reserved
	8	0x0000	pixclk_gate 0: PIXCLK is free running for all data formats 1: PIXCLK is output only when FV and LV are asserted
	7:5	X	Reserved
	4	0x0000	Reserved
	3	X	Reserved
	2:0	0x0000	parallel_bus_sel Select data source for output to parallel bus 0: gpo 1: rx_ss 2: cpipe_ss 3: Reserved 4: Reserved 5: Reserved 6: overlay_ssReserved 7: NTSC/PAL test pattern Legal values: [0, 7].
	Select data source for output to parallel bus		

Table 24: TX_SS Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
15362 R0x3C02	15:0	0x0000	gpo (R/W)
	15:12	0x0000	gpio_out Data to be output on pads {DOUT_LSB1, DOUT_LSB0, FRAME_VALID, LINE_VALID} when enabled as general purpose outputs Legal values: [0, 15].
	11:9	X	Reserved
	8:0	0x0000	gpo_out Data to be output on pads {PIXCLK, DOUT[7:0]} when enabled as general purpose outputs Legal values: [0, 511].
	General purpose output data		
15368 R0x3C08	15:0	0x2001	tvenc_ctrl_1 (R/W)
	15:14	X	Reserved
	13	0x0001	ntsc_test_pat_sel Test pattern to output if op_test_pat = 1 1: output EIA colour bars (NTSC) 0: output EBU colour bars (PAL)
	12	0x0000	op_test_pat Output select 0: output video data from sensor 1: output EIA(NTSC)/EBU(PAL) colour bars
	11:9	X	Reserved
	8	0x0000	sch Subcarrier horizontal sync phase control 0: subcarrier reset every 4 fields for NTSC and every 8 fields for PAL 1: subcarrier free running
	7:5	X	Reserved
	4	0x0000	ped_en Pedestal enable - when set a pedestal of 7.5 IRE is added to the composite video analogue output
	3:1	X	Reserved
	0	0x0001	pwdcv DAC power down control 0: enable DAC 1: power down DAC
	AVS TV encoder control register (1)		

Table 24: TX_SS Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
15370 R0x3C0A	15:0	0x0000	tvenc_ctrl_2 (R/W)
	15:14	X	Reserved
	13	0x0000	bw Monochrome display 0: colour display 1: monochrome display
	12	0x0000	ydly Luma delay control 0: luma output not delayed 1: luma output delayed by 74ns
	11:10	X	Reserved
	9:8	0x0000	bgt Brightness control 0: brightness control off 1: moderate brightness gain 2: most brightness gain 3: least brightness gain Legal values: [0, 3].
	7:6	X	Reserved
	5:4	0x0000	con Contrast control 0: contrast control off 1: 15/16 * luma gain 2: 14/16 * luma gain 3: 17/16 * luma gain Legal values: [0, 3] .
	3:2	X	Reserved
	1:0	0x0000	fsel Chroma filter selection 0: automatic bandwidth assignment 1: 0.675 MHz bandwidth 2: 1.36 MHz bandwidth 3: 2 MHz bandwidth Legal values: [0, 3].
	AVS TV encoder control register (2)		

OVERLAY_SS Register Descriptions

Table 25: OVERLAY_SS Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
20224 R0x4F00	15:0	0xC000	overlay_status (RO)
	15	RO	horizontal_sync Horizontal sync - default value is undetermined Read-only. Volatile.
	14	RO	vertical_sync Vertical sync Read-only. Volatile.
	13:6	X	Reserved
	5	RO	character_gen_active Active bit for Character Gen (active when one of the characters enable bits is set) Read-only. Volatile.
	4:0	RO	buffer_active Active bit for buffers 4 to 0 (active during active video) Read-only. Volatile. Legal values: [0, 63].
	Internal status monitor		
20226 R0x4F02	15:0	0x0000	overlay_control (R/W)
	15	0x0000	overlay_enable Enable the whole Overlay module. This bits when disabled/enabled is field synchronised for the RLE buffers Writes are synchronized to frame boundaries.
	14:1	X	Reserved
	0	0x0000	external_input_enable Select source image (BT656 input) 0: Internal 1: External
	Internal control		
20228 R0x4F04	15:0	X	overlay_interrupt_control (R/W)
	15:3	X	Reserved
	2	X	Reserved
	1	X	Reserved
	0	X	Reserved
	Interrupt source control		

DEWARP_SS Register Descriptions

Table 26: DEWARP_SS Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name
16384 R0x4000	15:0	0x0000	dewarp_control (R/W)
	15	0x0000	dewarp_en DeWarp Enable Control Bit 0 = DeWarp Disabled 1 = DeWarp Enabled Once all of the registers have been programmed, the DeWarp unit can be enabled. The dewarp unit can be disabled at anytime and dewarp will continue to output two fields. At the end of two fields the dewarp_busy signal will go low (also reported in bit 15 of the dewarp_status register) and then the registers can be reprogrammed. After disabling DeWarp and while dewarp_busy is active high, registers must not be modified.
	14:3	X	Reserved
	2	0x0000	Reserved
	1	0x0000	pal_en Video Type Mode 0 = NTSC 1 = PAL To be set to the correct mode, dependant on the sensor output mode.
	0	0x0000	debug_en Debug Mode 0 = Disabled 1 = Enabled When enabled the interlaced video output on the data_656_out output port is stopped and progressive video output is available on the debug_* ports. Registers require the correct settings for progressive debug output.
	DeWarp Control Register		
16424 R0x4028	15:0	0x0000	cpxc_fpme_l (R/W)
	15:0	0x0000	cpxc_fpme_l_value Legal values: [0, 65536].
	FloatingPoint mantissa exponent low word horizontal perspective correction centre (in camera space)		
16426 R0x402A	15:0	0x0000	cpxc_fpme_h (R/W)
	15:0	0x0000	cpxc_fpme_h_value Legal values: [0, 65536].
	FloatingPoint mantissa exponent high word formatted horizontal perspective correction centre (in camera space)		

Variable Descriptions

Monitor Variable Descriptions

Table 27: 0: Monitor Variables
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0x8000 VAR(0x00,0x0000)	15:0	0x0000	mon_major_version (R/W)
	Firmware major version (5=Rev1, 6=Rev2)		
0x8002 VAR(0x00,0x0002)	15:0	0x0000	mon_minor_version (R/W)
	Firmware minor version (6=Rev1, 17=Rev2)		
0x8004 VAR(0x00,0x0004)	15:0	0x0000	mon_release_version (R/W)
	Firmware release code		
0x8006 VAR(0x00,0x0006)	15:0	0x0000	mon_heartbeat (R/W)
	Sequencer frame counter (heartbeat) - incremented each sensor frame when system in SYS_STATE_STREAMING state		

Binning Off Context Variable Descriptions

Table 28: 6: Binning Off Context Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0x9800 VAR(0x06,0x0000)	15:0	0x0000	bin_off_config_ae_track_algo_enter (R/W)
	7:4	X	Reserved
	3	0x00	bin_off_config_ae_track_algo_enter_set_extgains Execute Set Extended Gains Routine Changes take effect during Vertical Blanking.
	2	0x00	bin_off_config_ae_track_algo_enter_calc_blacklevel Execute Set Blacklevel Routine Changes take effect during Vertical Blanking.
	1	0x00	bin_off_config_ae_track_algo_ent_adjust_brightness Execute Adjust Brightness Routine Changes take effect during Vertical Blanking.
	0	0x00	bin_off_config_ae_track_algo_enter_set_target_avgy Execute Set Target Average Y routine Changes take effect during Vertical Blanking.
	This variable configures the auto exposure tracking driver in ENTER state.		

Table 28: 6: Binning Off Context Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0x9802 VAR(0x06,0x0002)	15:0	0x000F	bin_off_config_ae_track_algo_run (R/W)
	7:4	X	Reserved
	3	0x01	bin_off_config_ae_track_algo_run_set_extgains Execute Set Extended Gains Routine Changes take effect during Vertical Blanking.
	2	0x01	bin_off_config_ae_track_algo_run_calc_blacklevel Execute Set Blacklevel Routine Changes take effect during Vertical Blanking.
	1	0x01	bin_off_config_ae_track_algo_run_adjust_brightnes Execute Adjust Brightness Routine Changes take effect during Vertical Blanking.
	0	0x01	bin_off_config_ae_track_algo_run_set_target_avgy Execute Set Target Average Y routine Changes take effect during Vertical Blanking.
	This variable configures the auto exposure tracking driver in RUN state.		
0x9804 VAR(0x06,0x0004)	15:0	0x0000	bin_off_config_awb_algo_enter (R/W)
	7	0x00	bin_off_config_awb_algo_enter_calc_ratios Calculate pre-AWB ratios from stats Changes take effect during Vertical Blanking.
	6	X	Reserved
	5	0x00	bin_off_config_awb_algo_enter_norm_ccm_matrix Execute Normalize CCM Matrix routine Changes take effect during Vertical Blanking.
	4	0x00	bin_off_config_awb_algo_enter_calc_ccm_matrix Execute Calc CCM Matrix Changes take effect during Vertical Blanking.
	3	0x00	bin_off_config_awb_algo_enter_calc_ccm_position Execute Calc CCM Matrix Position Changes take effect during Vertical Blanking.
	2	0x00	bin_off_config_awb_algo_enter_set_ccm_ll_matrix Execute Set CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	1	0x00	bin_off_config_awb_algo_enter_setup_ccm_ll_matrix Execute Setup CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	0	X	Reserved
	This variable configures the auto white balance driver in ENTER state.		

Table 28: 6: Binning Off Context Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0x9806 VAR(0x06,0x0006)	15:0	0x00FF	bin_off_config_awb_algo_run (R/W)
	7	0x01	bin_off_config_awb_algo_run_calc_ratios Calculate pre-AWB ratios from stats Changes take effect during Vertical Blanking.
	6	X	Reserved
	5	0x01	bin_off_config_awb_algo_run_norm_ccm_matrix Execute Normalize CCM Matrix routine Changes take effect during Vertical Blanking.
	4	0x01	bin_off_config_awb_algo_run_calc_ccm_matrix Execute Calc CCM Matrix Changes take effect during Vertical Blanking.
	3	0x01	bin_off_config_awb_algo_run_calc_ccm_position Execute Calc CCM Matrix Position Changes take effect during Vertical Blanking.
	2	0x01	bin_off_config_awb_algo_run_set_ccm_ll_matrix Execute Set CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	1	0x01	bin_off_config_awb_algo_run_setup_ccm_ll_matrix Execute Setup CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	0	X	Reserved
	This variable configures the auto white balance driver in RUN state.		
0x9808 VAR(0x06,0x0008)	15:0	0x001B	bin_off_config_awb_awb_xshift (R/W)
	This variable specifies the shift parameter in the x direction for the AWB statistics.		
0x980A VAR(0x06,0x000A)	15:0	0x001F	bin_off_config_awb_awb_yshift (R/W)
	This variable specifies the shift parameter in the y direction for the AWB statistics.		
0x980C VAR(0x06,0x000C)	15:0	0x0000	bin_off_config_ll_algo_enter (R/W)
	7	X	Reserved
	6	0x00	bin_off_config_ll_algo_enter_setnoise This routines calculates the noise reduction thresholds Changes take effect during Vertical Blanking.
	5	0x00	bin_off_config_ll_algo_enter_setsaturation This routine calculates the awb_desaturation and awb_saturation values Changes take effect during Vertical Blanking.
	4	0x00	bin_off_config_ll_algo_enter_setkernel This routine sets the Aperture 2D and the Defect cluster correction parameters Changes take effect during Vertical Blanking.
	3	0x00	bin_off_config_ll_algo_enter_settonal This routine writes physically to the Color Pipe registers to set up the Tonal curve Changes take effect during Vertical Blanking.
	2	0x00	bin_off_config_ll_algo_enter_setgamma This routine calculates the Gamma curve depending on the current scene Changes take effect during Vertical Blanking.
	1	X	Reserved
	0	0x00	bin_off_config_ll_algo_enter_autotc This routine corrects Tonal Curve (only upwards) depending on the histogram results Changes take effect during Vertical Blanking.
	This variable sets the low light driver in ENTER state.		

Table 28: 6: Binning Off Context Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0x980E VAR(0x06,0x000E)	15:0	0x007D	bin_off_config_ll_algo_run (R/W)
	7	X	Reserved
	6	0x01	bin_off_config_ll_algo_run_setnoise This routines calculates the noise reduction thresholds Changes take effect during Vertical Blanking.
	5	0x01	bin_off_config_ll_algo_run_setsaturation This routine calculates the awb_saturation values Changes take effect during Vertical Blanking.
	4	0x01	bin_off_config_ll_algo_run_setkernel This routine sets the Aperture 2D and the Defect cluster correction parameters Changes take effect during Vertical Blanking.
	3	0x01	bin_off_config_ll_algo_run_settonal This routine writes physically to the Color Pipe registers to set up the Tonal curve Changes take effect during Vertical Blanking.
	2	0x01	bin_off_config_ll_algo_run_setgamma This routine calculates the Gamma curve depending on the current scene Changes take effect during Vertical Blanking.
	1	X	Reserved
	0	0x01	bin_off_config_ll_algo_run_autotc This routine corrects Tonal Curve (only upwards) depending on the histogram results Changes take effect during Vertical Blanking.
	This variable sets the low light driver in RUN state.		
0x9810 VAR(0x06,0x0010)	15:0	0xFFFF	bin_off_config_stat_algo_enter (R/W)
	This variable configures the statistics driver in ENTER state.		
0x9812 VAR(0x06,0x0012)	15:0	0xFFFF	bin_off_config_stat_algo_run (R/W)
	This variable configures the statistics driver in RUN state.		
0x9814 VAR(0x06,0x0014)	15:0	0x0002	bin_off_config_sysctl_algo_enter (R/W)
	This variable configures the system control driver in ENTER state.		
0x9816 VAR(0x06,0x0016)	15:0	0x007C	bin_off_config_sysctl_algo_run (R/W)
	This variable configures the system control driver RUN state.		

AE_Rule Variable Descriptions

Table 29: 9: AE_Rule Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA404 VAR(0x09,0x0004)	15:0	0x0004	ae_rule_algo (R/W)
	7:4	X	Reserved
	3	0x00	ae_rule_exec_rule_weightedy AE Rule Algo - Exec Weighted Luma Algorithm
	2	0x00	ae_rule_exec_rule_avgy Selects the auto-exposure average-luma calculation algorithm: 0x0: Average scene brightness, 0x1: Weighted average scene brightness, 0x2: Evaluative average scene brightness with backlight detection Changes take effect during Vertical Blanking.
	1:0	X	Reserved
	Current Used Algorithm		

Table 29: 9: AE_Rule Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA408 VAR(0x09,0x0008)	15:0	0x0064	ae_rule_ae_weight_table_0_0 (R/W)
	Window weight for row 0, column 0 Changes take effect during Vertical Blanking.		
0xA40A VAR(0x09,0x000A)	15:0	0x0064	ae_rule_ae_weight_table_0_1 (R/W)
	Window weight for row 0, column 1 Changes take effect during Vertical Blanking.		
0xA40C VAR(0x09,0x000C)	15:0	0x0064	ae_rule_ae_weight_table_0_2 (R/W)
	Window weight for row 0, column 2 Changes take effect during Vertical Blanking.		
0xA40E VAR(0x09,0x000E)	15:0	0x0064	ae_rule_ae_weight_table_0_3 (R/W)
	Window weight for row 0, column 3 Changes take effect during Vertical Blanking.		
0xA410 VAR(0x09,0x0010)	15:0	0x0064	ae_rule_ae_weight_table_0_4 (R/W)
	Window weight for row 0, column 4 Changes take effect during Vertical Blanking.		
0xA412 VAR(0x09,0x0012)	15:0	0x0064	ae_rule_ae_weight_table_1_0 (R/W)
	Window weight for row 1, column 0 Changes take effect during Vertical Blanking.		
0xA414 VAR(0x09,0x0014)	15:0	0x0064	ae_rule_ae_weight_table_1_1 (R/W)
	Window weight for row 1, column 1 Changes take effect during Vertical Blanking.		
0xA416 VAR(0x09,0x0016)	15:0	0x0064	ae_rule_ae_weight_table_1_2 (R/W)
	Window weight for row 1, column 2 Changes take effect during Vertical Blanking.		
0xA418 VAR(0x09,0x0018)	15:0	0x0064	ae_rule_ae_weight_table_1_3 (R/W)
	Window weight for row 1, column 3 Changes take effect during Vertical Blanking.		
0xA41A VAR(0x09,0x001A)	15:0	0x0064	ae_rule_ae_weight_table_1_4 (R/W)
	Window weight for row 1, column 4 Changes take effect during Vertical Blanking.		
0xA41C VAR(0x09,0x001C)	15:0	0x0064	ae_rule_ae_weight_table_2_0 (R/W)
	Window weight for row 2, column 0 Changes take effect during Vertical Blanking.		
0xA41E VAR(0x09,0x001E)	15:0	0x0064	ae_rule_ae_weight_table_2_1 (R/W)
	Window weight for row 2, column 1 Changes take effect during Vertical Blanking.		
0xA420 VAR(0x09,0x0020)	15:0	0x0064	ae_rule_ae_weight_table_2_2 (R/W)
	Window weight for row 2, column 2 Changes take effect during Vertical Blanking.		
0xA422 VAR(0x09,0x0022)	15:0	0x0064	ae_rule_ae_weight_table_2_3 (R/W)
	Window weight for row 2, column 3 Changes take effect during Vertical Blanking.		
0xA424 VAR(0x09,0x0024)	15:0	0x0064	ae_rule_ae_weight_table_2_4 (R/W)
	Window weight for row 2, column 4 Changes take effect during Vertical Blanking.		
0xA426 VAR(0x09,0x0026)	15:0	0x0064	ae_rule_ae_weight_table_3_0 (R/W)
	Window weight for row 3, column 0 Changes take effect during Vertical Blanking.		

Table 29: 9: AE_Rule Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA428 VAR(0x09,0x0028)	15:0	0x0064	ae_rule_ae_weight_table_3_1 (R/W)
	Window weight for row 3, column 1 Changes take effect during Vertical Blanking.		
0xA42A VAR(0x09,0x002A)	15:0	0x0064	ae_rule_ae_weight_table_3_2 (R/W)
	Window weight for row 3, column 2 Changes take effect during Vertical Blanking.		
0xA42C VAR(0x09,0x002C)	15:0	0x0064	ae_rule_ae_weight_table_3_3 (R/W)
	Window weight for row 3, column 3 Changes take effect during Vertical Blanking.		
0xA42E VAR(0x09,0x002E)	15:0	0x0064	ae_rule_ae_weight_table_3_4 (R/W)
	Window weight for row 3, column 4 Changes take effect during Vertical Blanking.		
0xA430 VAR(0x09,0x0030)	15:0	0x0064	ae_rule_ae_weight_table_4_0 (R/W)
	Window weight for row 4, column 0 Changes take effect during Vertical Blanking.		
0xA432 VAR(0x09,0x0032)	15:0	0x0064	ae_rule_ae_weight_table_4_1 (R/W)
	Window weight for row 4, column 1 Changes take effect during Vertical Blanking.		
0xA434 VAR(0x09,0x0034)	15:0	0x0064	ae_rule_ae_weight_table_4_2 (R/W)
	Window weight for row 4, column 2 Changes take effect during Vertical Blanking.		
0xA436 VAR(0x09,0x0036)	15:0	0x0064	ae_rule_ae_weight_table_4_3 (R/W)
	Window weight for row 4, column 3 Changes take effect during Vertical Blanking.		
0xA438 VAR(0x09,0x0038)	15:0	0x0064	ae_rule_ae_weight_table_4_4 (R/W)
	Window weight for row 4, column 4 Changes take effect during Vertical Blanking.		

AE_Track Variable Descriptions

Table 30: 10: AE_Track Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA800 VAR(0x0A,0x0000)	15:0	0x0000	ae_track_status (R/W)
	7:4	X	Reserved
	3	0x00	ae_track_ae_status_ready This status bit reports that the AE algorithm has settled and no limits have been reached Updates on Vertical Blanking.
	2	0x00	ae_track_ae_status_skip_frame AE Track Status- AE is skipping this frame due to change to integration time Updates on Vertical Blanking.
	1	0x00	ae_track_ae_status_limithigh AE Track Status- AE has reached upper boundary Updates on Vertical Blanking.
	0	0x00	ae_track_ae_status_limitlow AE Track Status- AE has reached lower boundary Updates on Vertical Blanking.
	Current Status of Driver		
0xA802 VAR(0x0A,0x0002)	15:0	0x0053	ae_track_mode (R/W)
	7	0x00	ae_track_ae_mode_dcg_priority enable DCG over CG Priority Changes take effect during Vertical Blanking.
	6	0x00	ae_track_ae_mode_cgx50_on enable column gain x5 Changes take effect during Vertical Blanking.
	5	0x00	ae_track_ae_mode_cgx40_on enable column gain x4 Changes take effect during Vertical Blanking.
	4	0x00	ae_track_ae_mode_cgx30_on enable column gain x3 Changes take effect during Vertical Blanking.
	3	0x00	ae_track_ae_mode_cgx20_on enable column gain x2 Changes take effect during Vertical Blanking.
	2	0x00	ae_track_ae_mode_cgx15_on enable column gain x1.5 Changes take effect during Vertical Blanking.
	1	0x00	ae_track_ae_mode_cgx10_on enable column gain x1 Changes take effect during Vertical Blanking.
	0	0x00	ae_track_ae_mode_dcg_on enable DCG Changes take effect during Vertical Blanking.
	Currrent Driver Mode		

Table 30: 10: AE_Track Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA804 VAR(0x0A,0x0004)	15:0	0x0000	ae_track_algo (R/W)
	7:4	X	Reserved
	3	0x00	ae_track_exec_set_extgains Execute Set Extended Gains Routine Changes take effect during Vertical Blanking.
	2	0x00	ae_track_exec_calc_blacklevel Execute Set Blacklevel Routine Changes take effect during Vertical Blanking.
	1	0x00	ae_track_exec_adjust_brightness Execute Adjust Brightness Routine Changes take effect during Vertical Blanking.
	0	0x00	ae_track_exec_set_target_avgy Execute Set Target Average Y routine Changes take effect during Vertical Blanking.
	Current Used Algorithm. This variable provides the algorithms currently being used. The algorithms need to be enabled on the Binning Off Context Variables page.		
0xA806 VAR(0x0A,0x0006)	15:0	0x0008	ae_track_current_black_level (R/W)
	Current Subtracted Blacklevel Updates on Vertical Blanking.		
0xA808 VAR(0x0A,0x0008)	15:0	0x0004	ae_track_black_clipping_gate (R/W)
	Threshold for every bin in the histogram to be considered black Changes take effect during Vertical Blanking.		
0xA80A VAR(0x0A,0x000A)	15:0	0x0040	ae_track_max_black_level (R/W)
	Maximum Black Level Subtraction. Note that the total histogram range is 10 bits but the max black level max value is 8 bit Changes take effect during Vertical Blanking.		
0xA80C VAR(0x0A,0x000C)	15:0	0x0003	ae_track_black_level_damping (R/W)
	Dampening speed for ae_track_current_black_level changes Changes take effect during Vertical Blanking.		
0xA812 VAR(0x0A,0x0012)	15:0	0x004B	ae_track_target (R/W)
	Target brightness that AE_TRACK tries to reach. Normally provided by AE_RULE driver.		
0xA814 VAR(0x0A,0x0014)	15:0	0x0004	ae_track_gate (R/W)
	AE_TRACK does not modify the brightness if the current average luma is within the target luma +/- gate Changes take effect during Vertical Blanking.		
0xA816 VAR(0x0A,0x0016)	15:0	0x0000	ae_track_current_average_y (R/W)
	Current average brightness Updates on Vertical Blanking.		
0xA818 VAR(0x0A,0x0018)	15:0	0x0010	ae_track_ae_tracking_damping (R/W)
	Dampening speed for changes. This damping filter is only active when the brightness is setlled and average luma is equal to target luma +/- gate Changes take effect during Vertical Blanking.		
0xA81A VAR(0x0A,0x001A)	15:0	0x0003	ae_track_jump_divisor (R/W)
	This value is used to control the speed for AE to reach the target luma. Internally this divides the distance between the current average luma and the target luma in steps, so the smaller the value the faster the Auto Exposure. Changes take effect during Vertical Blanking.		

Table 30: 10: AE_Track Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xA824 VAR(0x0A,0x0024)	15:0	0x0106	ae_track_current_fdperiod (R/W)
	Updated from the CAM page depending on 50Hz or 60Hz configuration. This value is updated after a config change Updates after setting sys_refresh_mask = 3		
0xA826 VAR(0x0A,0x0026)	15:0	0x0002	ae_track_current_max_fdzone (R/W)
	Updated from the CAM page depending on 50Hz or 60Hz configuration. This value is updated after a config change Updates after setting sys_refresh_mask = 3.		
0xA82A VAR(0x0A,0x002A)	15:0	0x0001	ae_track_fdzone (R/W)
	Number of FDPeriods used for Integration (was "Index") Updates on Vertical Blanking.		
0xA830 VAR(0x0A,0x0030)	15:0	0x0001	ae_track_zone (R/W)
	There are three 'zones' suppored by the AE Track algorithm: 0x0: zone 0 - the integration time is less than 1 flicker period and analog/digital gains are unity. 0x1: zone 1 - the integration time is a multiple of FDPeriods and analog gain can reach the maximum value. 0x2: zone 2 - only digital gains are used to match the target luma. Updates on Vertical Blanking.		
0xA832 VAR(0x0A,0x0032)	15:0	0x0080	ae_track_virt_dgain (R/W)
	Digital gain when in zone 2		
0xA834 VAR(0x0A,0x0034)	15:0	0x0020	ae_track_virt_again (R/W)
	Internal virtual analog gain. This value is unsigned fixed-point with 5 fractional bits. Updates on Vertical Blanking.		
0xA838 VAR(0x0A,0x0038)	15:0	0x0000	ae_track_virt_column_gain (R/W)
	Indicates which Column Gain factors are currently enabled Updates on Vertical Blanking.		
0xA83A VAR(0x0A,0x003A)	15:0	0x0000	ae_track_dcggain (R/W)
	Indicates if DCG is currently enabled Updates on Vertical Blanking.		
0xA83C VAR(0x0A,0x003C)	31:0	0x00000000	ae_track_virt_int_time (R/W)
	Total integration time in PCLK Updates on Vertical Blanking.		
0xA840 VAR(0x0A,0x0040)	15:0	0x0000	ae_track_int_time_pclk (R/W)
	Fine integration time in PCLK Updates on Vertical Blanking.		
0xA842 VAR(0x0A,0x0042)	15:0	0x0000	ae_track_int_time_lines (R/W)
	Coarse integration time in Lines Updates on Vertical Blanking.		

AWB Variable Descriptions

Table 31: 11: AWB Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xAC00 VAR(0x0B,0x0000)	15:0	0x0000	awb_status (R/W)
	7:6	X	Reserved
	5	0x00	awb_skipping_frame AWB is skipping every other frame. Updates on Vertical Blanking.
	4	0x00	awb_limits_reached AWB has reached gain limits. Updates on Vertical Blanking.
	3	0x00	awb_no_stats AWB has no white balance statistics. Updates on Vertical Blanking.
	2	0x00	awb_new_limits AWB has reset to new limits for CCM position and gains. Updates on Vertical Blanking.
	1	0x00	awb_ccm_limits AWB has reached CCM position limits. Updates on Vertical Blanking.
	0	0x00	awb_steady AWB has reached a steady state. Updates on Vertical Blanking.
	Current Status of Driver		
0xAC02 VAR(0x0B,0x0002)	15:0	0x000A	awb_mode (R/W)
	7:5	X	Reserved
	4	0x00	Reserved
	3	0x00	awb_enable_steady Enables the steady feature. Changes take effect during Vertical Blanking.
	2	0x00	Reserved
	1	0x00	awb_lowlight Enable Dark CCM Support Changes take effect during Vertical Blanking.
	0	0x00	Reserved
	Currrent Driver Mode		

Table 31: 11: AWB Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xAC04 VAR(0x0B,0x0004)	15:0	0x0000	awb_algo (R/W)
	7	0x00	awb_exec_calc_ratios Calculate pre-AWB ratios from stats Changes take effect during Vertical Blanking.
	6	X	Reserved
	5	0x00	awb_exec_norm_ccm_matrix Execute Normalize CCM Matrix routine Changes take effect during Vertical Blanking.
	4	0x00	awb_exec_calc_ccm_matrix Execute Calc CCM Matrix Changes take effect during Vertical Blanking.
	3	0x00	awb_exec_calc_ccm_position Execute Calc CCM Matrix Position Changes take effect during Vertical Blanking.
	2	0x00	awb_exec_set_ccm_ll_matrix Execute Set CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	1	0x00	awb_exec_setup_ccm_ll_matrix Execute Setup CCM Lowlight Matrix Routine Changes take effect during Vertical Blanking.
	0	X	Reserved
	Current Used Algorithm. This variables provides the algorithms currently being used. The algorithms need to be enabled on the Binning Off Context Variables page.		
0xAC0A VAR(0x0B,0x000A)	15:0	0x0000	awb_ccm_0 (R/W)
	Color Correction Matrix value for column 0 and row 0 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC0C VAR(0x0B,0x000C)	15:0	0x0000	awb_ccm_1 (R/W)
	Color Correction Matrix value for column 1 and row 0 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC0E VAR(0x0B,0x000E)	15:0	0x0000	awb_ccm_2 (R/W)
	Color Correction Matrix value for column 2 and row 0 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC10 VAR(0x0B,0x0010)	15:0	0x0000	awb_ccm_3 (R/W)
	Color Correction Matrix value for column 0 and row 1 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC12 VAR(0x0B,0x0012)	15:0	0x0000	awb_ccm_4 (R/W)
	Color Correction Matrix value for column 1 and row 1 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC14 VAR(0x0B,0x0014)	15:0	0x0000	awb_ccm_5 (R/W)
	Color Correction Matrix value for column 2 and row 1 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		

Table 31: 11: AWB Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xAC16 VAR(0x0B,0x0016)	15:0	0x0000	awb_ccm_6 (R/W)
	Color Correction Matrix value for column 0 and row 2 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC18 VAR(0x0B,0x0018)	15:0	0x0000	awb_ccm_7 (R/W)
	Color Correction Matrix value for column 1 and row 2 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC1A VAR(0x0B,0x001A)	15:0	0x0000	awb_ccm_8 (R/W)
	Color Correction Matrix value for column 2 and row 2 This value is signed 2's complement fixed-point with 8 fractional bits. Updates on Vertical Blanking.		
0xAC1C VAR(0x0B,0x001C)	15:0	0x0000	awb_ccm_9 (R/W)
	Red to green gain ratio (CCM)		
0xAC1E VAR(0x0B,0x001E)	15:0	0x0000	awb_ccm_10 (R/W)
	Blue to green gain ratio (CCM)		
0xAC32 VAR(0x0B,0x0032)	15:0	0x0080	awb_saturation (R/W)
	Saturation for the current CCM - where 0x80 corresponds to a 100% saturated CCM. This value is calculated based on the ll_inv_brightness_metric. Updates on Vertical Blanking.		
0xAC36 VAR(0x0B,0x0036)	15:0	0x0040	awb_ccmposition (R/W)
	Position of the current CCM. Updates on Vertical Blanking.		
0xAC38 VAR(0x0B,0x0038)	15:0	0x0062	awb_r_ratio_lower (R/W)
	Lower value for the R/G ratio Threshold. This thresold is used to stop awb calculating new ratios when the difference is small Changes take effect during Vertical Blanking.		
0xAC3A VAR(0x0B,0x003A)	15:0	0x0068	awb_r_ratio_upper (R/W)
	Upper value for the R/G ratio Threshold. This thresold is used to stop awb calculating new ratios when the difference is small Changes take effect during Vertical Blanking.		
0xAC3C VAR(0x0B,0x003C)	15:0	0x0062	awb_b_ratio_lower (R/W)
	Lower value for the B/G ratio Threshold. This thresold is used to stop awb calculating new ratios when the difference is small Changes take effect during Vertical Blanking.		
0xAC3E VAR(0x0B,0x003E)	15:0	0x0068	awb_b_ratio_upper (R/W)
	Upper value for the B/G ratio h This thresold is used to stop awb calculating new ratios when the difference is small Changes take effect during Vertical Blanking.		
0xAC40 VAR(0x0B,0x0040)	15:0	0x0032	awb_r_scene_ratio_lower (R/W)
	Lower Limit value for pre-AWB R/G ratio Changes take effect during Vertical Blanking.		
0xAC42 VAR(0x0B,0x0042)	15:0	0x00C8	awb_r_scene_ratio_upper (R/W)
	Upper Limit value for pre-AWB R/G ratio Changes take effect during Vertical Blanking.		
0xAC44 VAR(0x0B,0x0044)	15:0	0x0023	awb_b_scene_ratio_lower (R/W)
	Lower Limit value for pre-AWB B/G ratio Changes take effect during Vertical Blanking.		

Table 31: 11: AWB Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xAC46 VAR(0x0B,0x0046)	15:0	0x00C8	awb_b_scene_ratio_upper (R/W)
	Upper Limit value for pre-AWB B/G ratio Changes take effect during Vertical Blanking.		
0xAC48 VAR(0x0B,0x0048)	15:0	0x0064	awb_r_ratio_pre_awb (R/W)
	R/G Ratio from the stats if AWB gains were not applied Updates on Vertical Blanking.		
0xAC4A VAR(0x0B,0x004A)	15:0	0x0064	awb_b_ratio_pre_awb (R/W)
	B/G Ratio from the stats if AWB gains were not applied Updates on Vertical Blanking.		
0xAC4C VAR(0x0B,0x004C)	15:0	0x0064	awb_r_ratio_post_awb (R/W)
	R/G Ratio from the stats Updates on Vertical Blanking.		
0xAC4E VAR(0x0B,0x004E)	15:0	0x0064	awb_b_ratio_post_awb (R/W)
	B/G Ratio from the stats Updates on Vertical Blanking.		

Stat Variable Descriptions

Table 32: 14: Stat Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xB878 VAR(0x0E,0x0078)	15:0	0x0000	stat_inv_brightness_metric (R/W)
	Inverted Brightness metric based on Int-Time, Gain, AvgY		
0xB87A VAR(0x0E,0x007A)	15:0	0x0000	stat_gain_metric (R/W)
	Virtual Analog Gain * Virtual Digital Gain		

Low Light Variable Descriptions

Table 33: 15: Low Light Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xBC02 VAR(0x0F,0x0002)	15:0	0x0003	ll_mode (R/W)
	7:3	X	Reserved
	2	0x00	ll_use_ext_gains_for_nr Use the extended gain for Noise Reduction control. This includes desaturation and noise reduction for RGB channels. Changes take effect during Vertical Blanking.
	1	0x00	ll_kill_aperture_enable When this bit is enabled the 2D aperture correction is disabled if ll_inv_brightness_metric < ll_cluster_dc_th_bm Changes take effect during Vertical Blanking.
	0	0x00	Reserved
	Currrent Driver Mode		

Table 33: 15: Low Light Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xBC04 VAR(0x0F,0x0004)	15:0	0x0000	ll_algo (R/W)
	7	0x00	Reserved
	6	0x00	ll_exec_setnoise This routines calculates the noise reduction thresholds Changes take effect during Vertical Blanking.
	5	0x00	ll_exec_setsaturation This routine calculates the awb_desaturation and awb_saturation values Changes take effect during Vertical Blanking.
	4	0x00	ll_exec_setkernel This routine sets the Aperture 2D and the Defect cluster correction parameters Changes take effect during Vertical Blanking.
	3	0x00	ll_exec_settonal This routine writes physically to the Color Pipe registers to set up the Tonal curve Changes take effect during Vertical Blanking.
	2	0x00	ll_exec_setgamma This routine calculates the Gamma curve depending on the current scene Changes take effect during Vertical Blanking.
	1	X	Reserved
	0	0x00	ll_exec_autotc This routine corrects Tonal Curve (only upwards) depending on the histogram results Changes take effect during Vertical Blanking.
	Current Used Algorithm. This variable provides the algorithms currently being used. The algorithms need to be enabled on the Binning Off Context Variables page.		
0xBC06 VAR(0x0F,0x0006)	15:0	0x0001	ll_cluster_dc_th (R/W)
	Threshold for Low Light Cluster Control. If this value is smaller than the Brightness Metric then cluster defect correction is enabled. Changes take effect during Vertical Blanking.		
0xBC08 VAR(0x0F,0x0008)	15:0	0x0000	ll_gamma_select (R/W)
	Gamma control - select automatic or static curves: 0x00: Auto curve 0x01: Contrast curve 0x02: Noise reduction curve Changes take effect during Vertical Blanking.		
0xBC0A VAR(0x0F,0x000A)	15:0	0x0000	ll_gamma_position (R/W)
	The position is calculated using the Brightness Metric Updates on Vertical Blanking.		
0xBC0C VAR(0x0F,0x000C)	15:0	0x0000	ll_gamma_contrast_curve_0 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 0 Changes take effect during Vertical Blanking.		
0xBC0E VAR(0x0F,0x000E)	15:0	0x0014	ll_gamma_contrast_curve_1 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 64 Changes take effect during Vertical Blanking.		
0xBC10 VAR(0x0F,0x0010)	15:0	0x0020	ll_gamma_contrast_curve_2 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 128 Changes take effect during Vertical Blanking.		
0xBC12 VAR(0x0F,0x0012)	15:0	0x0035	ll_gamma_contrast_curve_3 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 256 Changes take effect during Vertical Blanking.		

Table 33: 15: Low Light Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xBC14 VAR(0x0F,0x0014)	15:0	0x0058	ll_gamma_contrast_curve_4 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 512 Changes take effect during Vertical Blanking.		
0xBC16 VAR(0x0F,0x0016)	15:0	0x0075	ll_gamma_contrast_curve_5 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 768 Changes take effect during Vertical Blanking.		
0xBC18 VAR(0x0F,0x0018)	15:0	0x008E	ll_gamma_contrast_curve_6 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 1024 Changes take effect during Vertical Blanking.		
0xBC1A VAR(0x0F,0x001A)	15:0	0x00A3	ll_gamma_contrast_curve_7 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 1280 Changes take effect during Vertical Blanking.		
0xBC1C VAR(0x0F,0x001C)	15:0	0x00B5	ll_gamma_contrast_curve_8 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 1536 Changes take effect during Vertical Blanking.		
0xBC1E VAR(0x0F,0x001E)	15:0	0x00C5	ll_gamma_contrast_curve_9 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 1792 Changes take effect during Vertical Blanking.		
0xBC20 VAR(0x0F,0x0020)	15:0	0x00D3	ll_gamma_contrast_curve_10 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 2048 Changes take effect during Vertical Blanking.		
0xBC22 VAR(0x0F,0x0022)	15:0	0x00DD	ll_gamma_contrast_curve_11 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 2304 Changes take effect during Vertical Blanking.		
0xBC24 VAR(0x0F,0x0024)	15:0	0x00E6	ll_gamma_contrast_curve_12 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 2560 Changes take effect during Vertical Blanking.		
0xBC26 VAR(0x0F,0x0026)	15:0	0x00ED	ll_gamma_contrast_curve_13 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 2816 Changes take effect during Vertical Blanking.		
0xBC28 VAR(0x0F,0x0028)	15:0	0x00F2	ll_gamma_contrast_curve_14 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 3072 Changes take effect during Vertical Blanking.		
0xBC2A VAR(0x0F,0x002A)	15:0	0x00F6	ll_gamma_contrast_curve_15 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 3328 Changes take effect during Vertical Blanking.		
0xBC2C VAR(0x0F,0x002C)	15:0	0x00F9	ll_gamma_contrast_curve_16 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 3584 Changes take effect during Vertical Blanking.		
0xBC2E VAR(0x0F,0x002E)	15:0	0x00FC	ll_gamma_contrast_curve_17 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 3840 Changes take effect during Vertical Blanking.		
0xBC30 VAR(0x0F,0x0030)	15:0	0x00FF	ll_gamma_contrast_curve_18 (R/W)
	Contrast gamma curve knee point. The X coordinate is fixed to 4096 Changes take effect during Vertical Blanking.		
0xBC32 VAR(0x0F,0x0032)	15:0	0x0000	ll_gamma_nrcurve_0 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 0 Changes take effect during Vertical Blanking.		

Table 33: 15: Low Light Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xBC34 VAR(0x0F,0x0034)	15:0	0x0014	ll_gamma_nrcurve_1 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 64 Changes take effect during Vertical Blanking.		
0xBC36 VAR(0x0F,0x0036)	15:0	0x0026	ll_gamma_nrcurve_2 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 128 Changes take effect during Vertical Blanking.		
0xBC38 VAR(0x0F,0x0038)	15:0	0x003D	ll_gamma_nrcurve_3 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 256 Changes take effect during Vertical Blanking.		
0xBC3A VAR(0x0F,0x003A)	15:0	0x005F	ll_gamma_nrcurve_4 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 512 Changes take effect during Vertical Blanking.		
0xBC3C VAR(0x0F,0x003C)	15:0	0x0078	ll_gamma_nrcurve_5 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 768 Changes take effect during Vertical Blanking.		
0xBC3E VAR(0x0F,0x003E)	15:0	0x008A	ll_gamma_nrcurve_6 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 1024 Changes take effect during Vertical Blanking.		
0xBC40 VAR(0x0F,0x0040)	15:0	0x0098	ll_gamma_nrcurve_7 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 1280 Changes take effect during Vertical Blanking.		
0xBC42 VAR(0x0F,0x0042)	15:0	0x00A6	ll_gamma_nrcurve_8 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 1536 Changes take effect during Vertical Blanking.		
0xBC44 VAR(0x0F,0x0044)	15:0	0x00B2	ll_gamma_nrcurve_9 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 1792 Changes take effect during Vertical Blanking.		
0xBC46 VAR(0x0F,0x0046)	15:0	0x00BC	ll_gamma_nrcurve_10 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 2048 Changes take effect during Vertical Blanking.		
0xBC48 VAR(0x0F,0x0048)	15:0	0x00C6	ll_gamma_nrcurve_11 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 2304 Changes take effect during Vertical Blanking.		
0xBC4A VAR(0x0F,0x004A)	15:0	0x00D0	ll_gamma_nrcurve_12 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 2560 Changes take effect during Vertical Blanking.		
0xBC4C VAR(0x0F,0x004C)	15:0	0x00D8	ll_gamma_nrcurve_13 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 2816 Changes take effect during Vertical Blanking.		
0xBC4E VAR(0x0F,0x004E)	15:0	0x00E1	ll_gamma_nrcurve_14 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 3072 Changes take effect during Vertical Blanking.		
0xBC50 VAR(0x0F,0x0050)	15:0	0x00E9	ll_gamma_nrcurve_15 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 3328 Changes take effect during Vertical Blanking.		
0xBC52 VAR(0x0F,0x0052)	15:0	0x00F1	ll_gamma_nrcurve_16 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 3584 Changes take effect during Vertical Blanking.		

Table 33: 15: Low Light Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xBC54 VAR(0x0F,0x0054)	15:0	0x00F8	ll_gamma_nrcurve_17 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 3840 Changes take effect during Vertical Blanking.		
0xBC56 VAR(0x0F,0x0056)	15:0	0x00FF	ll_gamma_nrcurve_18 (R/W)
	Noise reduction gamma curve knee point. The X coordinate is fixed to 4096 Changes take effect during Vertical Blanking.		
0xBC58 VAR(0x0F,0x0058)	15:0	0x0024	ll_tclimit (R/W)
	Limiter for the ll_tonal_curve_med/low values Changes take effect during Vertical Blanking.		
0xBC5A VAR(0x0F,0x005A)	15:0	0x0008	ll_tcbase (R/W)
	Higher values make the TC curve more sensitive to the difference between the highest and the lowest part of the histogram This value is unsigned fixed-point with 3 fractional bits. Changes take effect during Vertical Blanking.		
0xBC5C VAR(0x0F,0x005C)	15:0	0x002D	ll_start_tcauto_limiter (R/W)
	Start point for tonal limits based on ll_inv_brightness_metric Changes take effect during Vertical Blanking.		
0xBC5E VAR(0x0F,0x005E)	15:0	0x00DC	ll_stop_tcauto_limiter (R/W)
	Stop point for tonal limits based on ll_inv_brightness_metric Changes take effect during Vertical Blanking.		
0xBC60 VAR(0x0F,0x0060)	15:0	0x007F	ll_tonal_curve_high (R/W)
	Increase of the high-luma values. The unity for this variable is 0x7F. Numbers above increase the luma output, numbers below decrease it. Note that the luma range is [0, 0x3FF]. Changes take effect during Vertical Blanking.		
0xBC62 VAR(0x0F,0x0062)	15:0	0x007F	ll_tonal_curve_med (R/W)
	Increase of the mid-luma values. The unity for this variable is 0x7F. Numbers above increase the luma output, numbers below decrease it. Note that the luma range is [0, 0x3FF]. This value gets overwritten if "ll_exec_autotc" is enabled Changes take effect during Vertical Blanking.		
0xBC64 VAR(0x0F,0x0064)	15:0	0x007F	ll_tonal_curve_low (R/W)
	Increase of the low-luma values. The unity for this variable is 0x7F. Numbers above increase the luma output, numbers below decrease it Note that the luma range is [0, 0x3FF]. This value gets overwritten if "ll_exec_autotc" is enabled Changes take effect during Vertical Blanking.		

Cam1Control Variable Descriptions

Table 34: 18: Cam1Control Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC800 VAR(0x12,0x0000)	15:0	0x000C	cam1_sensor_0_y_addr_start (R/W)
	The first row of visible pixels to be read out (not counting any dark rows that may be read). Must be an even value. Changes take effect after setting sys_refresh_mask = 3.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC802 VAR(0x12,0x0002)	15:0	0x0010	cam1_sensor_0_x_addr_start (R/W)
	The first column of visible pixels to be read out (not counting any dark columns that may be read). Must be an even value. Changes take effect after setting sys_refresh_mask = 3.		
0xC804 VAR(0x12,0x0004)	15:0	0x01F3	cam1_sensor_0_y_addr_end (R/W)
	The last row of visible pixels to be read out. Must be an odd value. Changes take effect after setting sys_refresh_mask = 3.		
0xC806 VAR(0x12,0x0006)	15:0	0x0297	cam1_sensor_0_x_addr_end (R/W)
	The last column of visible pixels to be read out. Must be an odd value. Changes take effect after setting sys_refresh_mask = 3.		
0xC80A VAR(0x12,0x000A)	15:0	0x0041	cam1_sensor_0_read_mode (R/W)
	15	0x0000	cam1_sensor_0_read_mode_orientation_vert_flip This bit enables the vertical flip of the sensor. Changes take effect after setting sys_refresh_mask = 3. 0 = Normal 1 = Vertical Flip
	14	0x0000	cam1_sensor_0_read_mode_orientation_horiz_mirror This bit enables the horizontal mirror of the sensor. Changes take effect after setting sys_refresh_mask = 3. 0 = Normal 1 = Horizontal Mirror
	13:0	X	Reserved
	Controls the sensor read-mode		
0xC812 VAR(0x12,0x0012)	15:0	0x020D	cam1_sensor_0_frame_length_lines (R/W)
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Changes take effect after setting sys_refresh_mask = 3.		
0xC814 VAR(0x12,0x0014)	15:0	0x035A	cam1_sensor_0_line_length_pck (R/W)
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking. Changes take effect after setting sys_refresh_mask = 3.		
0xC816 VAR(0x12,0x0016)	15:0	0x0031	cam1_sensor_0_fine_correction (R/W)
	Fine Correction (fine integration time) Changes take effect after setting sys_refresh_mask = 3.		
0xC81A VAR(0x12,0x001A)	15:0	0x0000	cam1_sensor_0_awb_hg_window_xstart (R/W)
	Start pixel for the X-coord of AWB, SecondBlacklevel and Tonal Correction histograms windows Changes take effect after setting sys_refresh_mask = 3.		
0xC81C VAR(0x12,0x001C)	15:0	0x0000	cam1_sensor_0_awb_hg_window_ystart (R/W)
	Start pixel for the Y-coord of AWB, SecondBlacklevel and Tonal Correction histograms windows Changes take effect after setting sys_refresh_mask = 3.		
0xC81E VAR(0x12,0x001E)	15:0	0x0286	cam1_sensor_0_awb_hg_window_xend (R/W)
	End pixel for the X-coord of AWB, SecondBlacklevel and Tonal correction histograms windows Changes take effect after setting sys_refresh_mask = 3.		
0xC820 VAR(0x12,0x0020)	15:0	0x01E6	cam1_sensor_0_awb_hg_window_yend (R/W)
	End pixel for the Y-coord of AWB, SecondBlacklevel and Tonal Correction histograms windows Changes take effect after setting sys_refresh_mask = 3.		
0xC822 VAR(0x12,0x0022)	15:0	0x0004	cam1_sensor_0_ae_initial_window_xstart (R/W)
	Start pixel for the X-coord of AE histograms window. This is only the first window of the 5x5 grid Changes take effect after setting sys_refresh_mask = 3.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC824 VAR(0x12,0x0024)	15:0	0x0004	cam1_sensor_0_ae_initial_window_ystart (R/W)
	Start pixel for the Y-coord of AE histograms window. This is only the first window of the 5x5 grid Changes take effect after setting sys_refresh_mask = 3.		
0xC826 VAR(0x12,0x0026)	15:0	0x0084	cam1_sensor_0_ae_initial_window_xend (R/W)
	End pixel for the X-coord of AE histograms window. This is only the first window of the 5x5 grid Changes take effect after setting sys_refresh_mask = 3.		
0xC828 VAR(0x12,0x0028)	15:0	0x0064	cam1_sensor_0_ae_initial_window_yend (R/W)
	End pixel for the Y-coord of AE histograms window. This is only the first window of the 5x5 grid Changes take effect after setting sys_refresh_mask = 3.		
0xC82A VAR(0x12,0x002A)	15:0	0x0106	cam1_sensor_0_fdperiod_0 (R/W)
	Flicker Period for 60Hz specified in lines Changes take effect after setting sys_refresh_mask = 3.		
0xC82C VAR(0x12,0x002C)	15:0	0x013B	cam1_sensor_0_fdperiod_1 (R/W)
	Flicker Period for 50Hz specified in lines Changes take effect after setting sys_refresh_mask = 3.		
0xC82E VAR(0x12,0x002E)	15:0	0x0002	cam1_sensor_0_max_fdzone_0 (R/W)
	Maximum number of Flicker periods (at 60Hz). This value is used by AE to determine which is the minimum frame rate available. Changes take effect after setting sys_refresh_mask = 3.		
0xC830 VAR(0x12,0x0030)	15:0	0x0001	cam1_sensor_0_max_fdzone_1 (R/W)
	Maximum number of Flicker periods (at 50Hz). This value is used by AE to determine which is the minimum frame rate available. Changes take effect after setting sys_refresh_mask = 3.		
0xC86C VAR(0x12,0x006C)	15:0	0x0020	cam1_analog_gain (R/W)
	Global logical representation of analog gain. Range is 0x0000 to 0x01F8 (1/32x-15.75x) This value is unsigned fixed-point with 5 fractional bits. Updates on Vertical Blanking.		
0xC86E VAR(0x12,0x006E)	15:0	0x0020	cam1_analog_red_gain (R/W)
	Logical representation of red analog gain gain = bits[8:0] * 1/32		
0xC870 VAR(0x12,0x0070)	15:0	0x0020	cam1_analog_green1gain (R/W)
	Logical representation of green1 analog gain gain = bits[8:0] * 1/32		
0xC872 VAR(0x12,0x0072)	15:0	0x0020	cam1_analog_green2gain (R/W)
	Logical representation of green2 analog gain gain = bits[8:0] * 1/32		
0xC874 VAR(0x12,0x0074)	15:0	0x0020	cam1_analog_blue_gain (R/W)
	Logical representation of blue analog gain gain = bits[8:0] * 1/32		
0xC876 VAR(0x12,0x0076)	15:0	0x0080	cam1_digital_gain (R/W)
	Global logical representation of digital gain. Range is 0x0000 to 0x03FF (1/128x - 7.999x) This value is unsigned fixed-point with 7 fractional bits. Updates on Vertical Blanking.		
0xC87A VAR(0x12,0x007A)	15:0	0x0001	cam1_min_analog_gain (R/W)
	Minimum analog gain supported by this sensor		
0xC87C VAR(0x12,0x007C)	15:0	0x01F8	cam1_max_analog_gain (R/W)
	Maximum analog gain supported by this sensor		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC87E VAR(0x12,0x007E)	15:0	0x0080	cam1_dgain_red (R/W)
	Pipeline Digital Gain Red * 1/128 (Max-Gain = 1024 * (1/128))		
0xC880 VAR(0x12,0x0080)	15:0	0x0080	cam1_dgain_green1 (R/W)
	Pipeline Digital Gain Green1 * 1/128		
0xC882 VAR(0x12,0x0082)	15:0	0x0080	cam1_dgain_green2 (R/W)
	Pipeline Digital Gain Green 2 * 1/128		
0xC884 VAR(0x12,0x0084)	15:0	0x0080	cam1_dgain_blue (R/W)
	Pipeline Digital Gain Blue * 1/128		
0xC886 VAR(0x12,0x0086)	15:0	0x0080	cam1_dgain_second (R/W)
	Second Pipeline Digital Gain after PGA		
0xC888 VAR(0x12,0x0088)	15:0	0x0000	cam1_virt_int_time (R/W)
	Virtual Integration time, maintained by AE_Track		
0xC88A VAR(0x12,0x008A)	15:0	0x0010	cam1_coarse_integration_time (R/W)
	Coarse Integration time specified in number of lines Updates on Vertical Blanking.		
0xC88C VAR(0x12,0x008C)	15:0	0x0000	cam1_fine_integration_time (R/W)
	Integration time specified as a number of pixel clocks added to coarseIntegrationTime for total. Updates on Vertical Blanking.		
0xC88E VAR(0x12,0x008E)	15:0	0x002A	cam1_first_black_level (R/W)
	First Black Level Subtraction value (constant)		
0xC890 VAR(0x12,0x0090)	15:0	0x0008	cam1_second_black_level (R/W)
	Second Black Level Subtraction (calculated)		
0xC892 VAR(0x12,0x0092)	15:0	0x0010	cam1_sensor_x_offset (R/W)
	Manufacturing Calibration X Offset		
0xC894 VAR(0x12,0x0094)	15:0	0x000C	cam1_sensor_y_offset (R/W)
	Manufacturing Calibration Y Offset		
0xC896 VAR(0x12,0x0096)	15:0	0x0000	cam1_flicker_mode (R/W)
	Current flicker mode (0=60 Hz, 1 = 50 Hz)		
0xC898 VAR(0x12,0x0098)	15:0	0x0400	cam1_aet_black_clipping_target (R/W)
	Auto-exposure black level clipping target		
0xC89A VAR(0x12,0x009A)	15:0	0x0001	cam1_aet_skip_frames (R/W)
	This specifies the number of frames to skip after adjusting brightness.		
0xC89C VAR(0x12,0x009C)	15:0	0x0002	cam1_aet_target_fdzone (R/W)
	This variable specifies the target FD zone the sensor should stay before increasing the zone. Gains will be increased before zone is increased. This is used in AE zone 1.		
0xC89E VAR(0x12,0x009E)	15:0	0x0040	cam1_aet_target_again (R/W)
	This variable specifies the target analog gain the sensor should stay before increasing. FD zones will be incremented before analog gain is increased. This is used in AE zone 1.		
0xC8A0 VAR(0x12,0x00A0)	15:0	0x0020	cam1_aet_ae_min_virt_int_time_pclk (R/W)
	This value is the number of 2xPCLK for the minimum integration time Changes take effect during Vertical Blanking.		
0xC8A2 VAR(0x12,0x00A2)	15:0	0x0080	cam1_aet_ae_min_virt_dgain (R/W)
	The is the minimum value for the second digital gain. This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC8A4 VAR(0x12,0x00A4)	15:0	0x0080	cam1_aet_ae_max_virt_dgain (R/W)
	The is the maximum value for the second digital gain. This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC8A6 VAR(0x12,0x00A6)	15:0	0x0020	cam1_aet_ae_min_virt_again (R/W)
	The is the minimun value for the virtual analog gain. This value is unsigned fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8A8 VAR(0x12,0x00A8)	15:0	0x1D4C	cam1_aet_ae_max_virt_again (R/W)
	The is the maximum value for the virtual analog gain. This value is unsigned fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8AC VAR(0x12,0x00AC)	15:0	0x0080	cam1_aet_ae_virt_gain_th_cg (R/W)
	The column gain will be enabled if the virtual anlog gain is bigger than this threshold Limitation: this value has to be higher/equal than cam_aet_ae_virt_gain_th_dcg if ae_track_ae_mode_dcg_priority bit is enabled This value is unsigned fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8AE VAR(0x12,0x00AE)	15:0	0x0100	cam1_aet_ae_virt_gain_th_dcg (R/W)
	Threshold to enable high-conversion gain (DCG)		
0xC8BE VAR(0x12,0x00BE)	15:0	0x0000	cam1_aet_ext_gain_setup_0 (R/W)
	Placeholder for variables that might be needed for patching		
0xC8CE VAR(0x12,0x00CE)	15:0	0x01D9	cam1_awb_ccm_l_0 (R/W)
	Red rich CCM value for column 0 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8D0 VAR(0x12,0x00D0)	15:0	0xFF05	cam1_awb_ccm_l_1 (R/W)
	Red rich CCM value for column 1 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8D2 VAR(0x12,0x00D2)	15:0	0x003F	cam1_awb_ccm_l_2 (R/W)
	Red rich CCM value for column 2 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8D4 VAR(0x12,0x00D4)	15:0	0xFFC3	cam1_awb_ccm_l_3 (R/W)
	Red rich CCM value for column 0 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8D6 VAR(0x12,0x00D6)	15:0	0x0132	cam1_awb_ccm_l_4 (R/W)
	Red rich CCM value for column 1 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8D8 VAR(0x12,0x00D8)	15:0	0x0027	cam1_awb_ccm_l_5 (R/W)
	Red rich CCM value for column 2 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC8DA VAR(0x12,0x00DA)	15:0	0xFFB5	cam1_awb_ccm_l_6 (R/W)
	Red rich CCM value for column 0 and row 2 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8DC VAR(0x12,0x00DC)	15:0	0xFEA4	cam1_awb_ccm_l_7 (R/W)
	Red rich CCM value for column 1 and row 2 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8DE VAR(0x12,0x00DE)	15:0	0x02C2	cam1_awb_ccm_l_8 (R/W)
	Red rich CCM value for column 2 and row 2 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8E0 VAR(0x12,0x00E0)	15:0	0x0011	cam1_awb_ccm_l_9 (R/W)
	R/G ratio for the Left CCM This value is unsigned fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8E2 VAR(0x12,0x00E2)	15:0	0x0052	cam1_awb_ccm_l_10 (R/W)
	B/G ratio for the Left CCM This value is unsigned fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8E4 VAR(0x12,0x00E4)	15:0	0xFF8F	cam1_awb_ccm_rl_0 (R/W)
	Blue rich CCM value for column 0 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8E6 VAR(0x12,0x00E6)	15:0	0x00A8	cam1_awb_ccm_rl_1 (R/W)
	Blue rich CCM value for column 1 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8E8 VAR(0x12,0x00E8)	15:0	0xFFC8	cam1_awb_ccm_rl_2 (R/W)
	Blue rich CCM value for column 2 and row 0 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8EA VAR(0x12,0x00EA)	15:0	0x0012	cam1_awb_ccm_rl_3 (R/W)
	Blue rich CCM value for column 0 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8EC VAR(0x12,0x00EC)	15:0	0x000F	cam1_awb_ccm_rl_4 (R/W)
	Blue rich CCM value for column 1 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8EE VAR(0x12,0x00EE)	15:0	0xFFDE	cam1_awb_ccm_rl_5 (R/W)
	Blue rich CCM value for column 2 and row 1 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8F0 VAR(0x12,0x00F0)	15:0	0x0054	cam1_awb_ccm_rl_6 (R/W)
	Blue rich CCM value for column 0 and row 2 This value is signedtwo's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC8F2 VAR(0x12,0x00F2)	15:0	0x00A0	cam1_awb_ccm_rl_7 (R/W)
	Blue rich CCM value for column 1 and row 2 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8F4 VAR(0x12,0x00F4)	15:0	0xFF0A	cam1_awb_ccm_rl_8 (R/W)
	Blue rich CCM value for column 2 and row 2 This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8F6 VAR(0x12,0x00F6)	15:0	0x0011	cam1_awb_ccm_rl_9 (R/W)
	R/G ratio for the Right CCM This value is signed two's complement fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8F8 VAR(0x12,0x00F8)	15:0	0xFFD4	cam1_awb_ccm_rl_10 (R/W)
	B/G ratio for the Right CCM This value is signed two's complement fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC8FA VAR(0x12,0x00FA)	15:0	0x004D	cam1_awb_ll_ccm_0 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8FC VAR(0x12,0x00FC)	15:0	0x0096	cam1_awb_ll_ccm_1 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC8FE VAR(0x12,0x00FE)	15:0	0x001D	cam1_awb_ll_ccm_2 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC900 VAR(0x12,0x0100)	15:0	0x004D	cam1_awb_ll_ccm_3 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC902 VAR(0x12,0x0102)	15:0	0x0096	cam1_awb_ll_ccm_4 (R/W)
	Matrix for low light This value is signed two2's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC904 VAR(0x12,0x0104)	15:0	0x001D	cam1_awb_ll_ccm_5 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC906 VAR(0x12,0x0106)	15:0	0x004D	cam1_awb_ll_ccm_6 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC908 VAR(0x12,0x0108)	15:0	0x0096	cam1_awb_ll_ccm_7 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC90A VAR(0x12,0x010A)	15:0	0x001D	cam1_awb_ll_ccm_8 (R/W)
	Matrix for low light This value is signed two's complement fixed-point with 8 fractional bits. Changes take effect during Vertical Blanking.		
0xC90C VAR(0x12,0x010C)	15:0	0x0000	cam1_awb_ccmposition_min (R/W)
	CCM Position minimum value Changes take effect during Vertical Blanking.		
0xC90E VAR(0x12,0x010E)	15:0	0x007F	cam1_awb_ccmposition_max (R/W)
	CCM Position maximum value Changes take effect during Vertical Blanking.		
0xC910 VAR(0x12,0x0110)	15:0	0x0003	cam1_awb_awb_xscale (R/W)
	Scale parameter in x direction in prob table Changes take effect after setting sys_refresh_mask = 3.		
0xC912 VAR(0x12,0x0112)	15:0	0x0002	cam1_awb_awb_yscale (R/W)
	Scale parameter in y direction in prob table Changes take effect after setting sys_refresh_mask = 3.		
0xC914 VAR(0x12,0x0114)	15:0	0x48C3	cam1_awb_awb_weights_0 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC916 VAR(0x12,0x0116)	15:0	0xECAD	cam1_awb_awb_weights_1 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC918 VAR(0x12,0x0118)	15:0	0xFF97	cam1_awb_awb_weights_2 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC91A VAR(0x12,0x011A)	15:0	0x189D	cam1_awb_awb_weights_3 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC91C VAR(0x12,0x011C)	15:0	0x9103	cam1_awb_awb_weights_4 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC91E VAR(0x12,0x011E)	15:0	0xAFFE	cam1_awb_awb_weights_5 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC920 VAR(0x12,0x0120)	15:0	0x402F	cam1_awb_awb_weights_6 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC922 VAR(0x12,0x0122)	15:0	0x0000	cam1_awb_awb_weights_7 (R/W)
	Table of AWB weights Changes take effect after setting sys_refresh_mask = 3.		
0xC924 VAR(0x12,0x0124)	15:0	0x003A	cam1_awb_awb_xshift_pre_adj (R/W)
	Preadjusted X shift parameter to index into weight table This value is signed 2's complement fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		
0xC926 VAR(0x12,0x0126)	15:0	0x003A	cam1_awb_awb_yshift_pre_adj (R/W)
	Preadjusted Y shift parameter to index into weight table This value is signed 2's complement fixed-point with 5 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC928 VAR(0x12,0x0128)	15:0	0x0010	cam1_stat_luma_thresh_low (R/W)
	Lower luma threshold for pixels used in AWB Changes take effect after setting sys_refresh_mask = 3.		
0xC92A VAR(0x12,0x012A)	15:0	0x00F0	cam1_stat_luma_thresh_high (R/W)
	Upper luma threshold for pixels used in AWB Changes take effect after setting sys_refresh_mask = 3.		
0xC92C VAR(0x12,0x012C)	15:0	0x0011	cam1_stat_gain_metric_predivider (R/W)
	This predivider is needed as the Gain Metric value is expressed in integer format and it can roll over Changes take effect during Vertical Blanking.		
0xC92E VAR(0x12,0x012E)	15:0	0x000A	cam1_stat_brightness_metric_predivider (R/W)
	This predivider is needed as the Brightness Metric value is expressed in integer format and it can roll over Changes take effect during Vertical Blanking.		
0xC930 VAR(0x12,0x0130)	15:0	0x0028	cam1_ll_start_brightness (R/W)
	ll_inv_brightness_metric value to start transition to LowLight corrections Changes take effect during Vertical Blanking.		
0xC932 VAR(0x12,0x0132)	15:0	0x00C8	cam1_ll_stop_brightness (R/W)
	ll_inv_brightness_metric value to stop transition to LowLight corrections Changes take effect during Vertical Blanking.		
0xC934 VAR(0x12,0x0134)	15:0	0x0080	cam1_ll_start_saturation (R/W)
	Start Value for Saturation Changes take effect during Vertical Blanking.		
0xC936 VAR(0x12,0x0136)	15:0	0x0030	cam1_ll_end_saturation (R/W)
	End Value for Saturation Changes take effect during Vertical Blanking.		
0xC93C VAR(0x12,0x013C)	15:0	0x0008	cam1_ll_ll_start_0 (R/W)
	Demosaic setup start point Changes take effect during Vertical Blanking.		
0xC93E VAR(0x12,0x013E)	15:0	0x0002	cam1_ll_ll_start_1 (R/W)
	Aperture knee setup start point Changes take effect during Vertical Blanking.		
0xC940 VAR(0x12,0x0140)	15:0	0x0002	cam1_ll_ll_start_2 (R/W)
	Aperture gain setup start point Changes take effect during Vertical Blanking.		
0xC942 VAR(0x12,0x0142)	15:0	0x0068	cam1_ll_ll_stop_0 (R/W)
	Demosaic setup stop point Changes take effect during Vertical Blanking.		
0xC944 VAR(0x12,0x0144)	15:0	0x0001	cam1_ll_ll_stop_1 (R/W)
	Aperture knee setup stop point Changes take effect during Vertical Blanking.		
0xC946 VAR(0x12,0x0146)	15:0	0x0009	cam1_ll_ll_stop_2 (R/W)
	Aperture gain setup stop point Changes take effect during Vertical Blanking.		
0xC948 VAR(0x12,0x0148)	15:0	0x000C	cam1_ll_nr_start_0 (R/W)
	Noise Setup Start Parameters Red Changes take effect during Vertical Blanking.		
0xC94A VAR(0x12,0x014A)	15:0	0x000C	cam1_ll_nr_start_1 (R/W)
	Noise Setup Start Parameters Green1 Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC94C VAR(0x12,0x014C)	15:0	0x000C	cam1_ll_nr_start_2 (R/W)
	Noise Setup Start Parameters Blue Changes take effect during Vertical Blanking.		
0xC94E VAR(0x12,0x014E)	15:0	0x000C	cam1_ll_nr_start_3 (R/W)
	Noise Setup Start Parameters Green2 Changes take effect during Vertical Blanking.		
0xC950 VAR(0x12,0x0150)	15:0	0x0028	cam1_ll_nr_stop_0 (R/W)
	Noise Setup Stop Parameters Red Changes take effect during Vertical Blanking.		
0xC952 VAR(0x12,0x0152)	15:0	0x0028	cam1_ll_nr_stop_1 (R/W)
	Noise Setup Stop Parameters Green1 Changes take effect during Vertical Blanking.		
0xC954 VAR(0x12,0x0154)	15:0	0x0028	cam1_ll_nr_stop_2 (R/W)
	Noise Setup Stop Parameters Blue Changes take effect during Vertical Blanking.		
0xC956 VAR(0x12,0x0156)	15:0	0x0028	cam1_ll_nr_stop_3 (R/W)
	Noise Setup Stop Parameters Green2 Changes take effect during Vertical Blanking.		
0xC958 VAR(0x12,0x0158)	15:0	0x0028	cam1_ll_start_gamma_bm (R/W)
	ll_inv_brightness_metric value to start transition from contrast enhancement curve. Changes take effect during Vertical Blanking.		
0xC95A VAR(0x12,0x015A)	15:0	0x00C8	cam1_ll_stop_gamma_bm (R/W)
	ll_inv_brightness_metric value to stop transition to noise reduction curve. Changes take effect during Vertical Blanking.		
0xC95C VAR(0x12,0x015C)	15:0	0x0096	cam1_ll_start_gain_metric (R/W)
	Gain Metric value to start transition to LowLight corrections Changes take effect during Vertical Blanking.		
0xC95E VAR(0x12,0x015E)	15:0	0x00FA	cam1_ll_stop_gain_metric (R/W)
	Gain Metric value to stop transition to LowLight corrections Changes take effect during Vertical Blanking.		
0xC960 VAR(0x12,0x0160)	15:0	0x0040	cam1_ll_x0 (R/W)
	CCM position threshold in which to use the tint offsets. Changes take effect during Vertical Blanking.		
0xC962 VAR(0x12,0x0162)	15:0	0x0080	cam1_ll_k_r_l (R/W)
	This is the Tint control for the Red channel in the Left CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC964 VAR(0x12,0x0164)	15:0	0x0080	cam1_ll_k_g_l (R/W)
	This is the Tint control for the Green channel in the Left CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC966 VAR(0x12,0x0166)	15:0	0x0080	cam1_ll_k_b_l (R/W)
	This is the Tint control for the Blue channel in the Left CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		

Table 34: 18: Cam1Control Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xC968 VAR(0x12,0x0168)	15:0	0x0080	cam1_ll_k_r_r (R/W)
	This is the Tint control for the Red channel in the Right CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC96A VAR(0x12,0x016A)	15:0	0x0080	cam1_ll_k_g_r (R/W)
	This is the Tint control for the Green channel in the Right CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC96C VAR(0x12,0x016C)	15:0	0x0080	cam1_ll_k_b_r (R/W)
	This is the Tint control for the Blue channel in the Right CCM This value is unsigned fixed-point with 7 fractional bits. Changes take effect during Vertical Blanking.		
0xC96E VAR(0x12,0x016E)	15:0	0x0003	cam1_sys_uv_color_boost (R/W)
	Color kill saturation point Changes take effect during Vertical Blanking.		

SysCtrl Variable Descriptions

Table 35: 23: SysCtrl Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xDC28 VAR(0x17,0x0028)	15:0	0x0000	sys_refresh_mask (R/W)
	15:2	X	Reserved
	1	0x00	sys_exec_algorithm_restart Sys Refresh Mask - Restart the algorithms
	0	0x00	Reserved
	Mask of functions to be called at end of to refresh sensor registers if Sys Algo - Execute Refresh Routine enabled		

Command Handler Variable Descriptions

Table 36: 31: Command Handler Variable Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xFC00 VAR(0x1F,0x0000)	15:0	0x0000	cmd_handler_params_pool_0 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC02 VAR(0x1F,0x0002)	15:0	0x0000	cmd_handler_params_pool_1 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC04 VAR(0x1F,0x0004)	15:0	0x0000	cmd_handler_params_pool_2 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC06 VAR(0x1F,0x0006)	15:0	0x0000	cmd_handler_params_pool_3 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC08 VAR(0x1F,0x0008)	15:0	0x0000	cmd_handler_params_pool_4 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC0A VAR(0x1F,0x000A)	15:0	0x0000	cmd_handler_params_pool_5 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		

Table 36: 31: Command Handler Variable Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Variable	Bits	Default	Name
0xFC0C VAR(0x1F,0x000C)	15:0	0x0000	cmd_handler_params_pool_6 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		
0xFC0E VAR(0x1F,0x000E)	15:0	0x0000	cmd_handler_params_pool_7 (R/W)
	The Command Handler parameter pool (see Host Command Interface specification for details)		

Revision History

Rev. B 11/10/10

- Applied updated Aptina template

Rev. A 7/31/09

- Initial release

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