MT9V131 Registers

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

MT9V131 Register Reference

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Registers

One type of configuration control is available:

1. Hardware registers

The following convention is used in the text below to designate registers:

R0x12:1, R0x12:1[3:0] or R18:1, R18:1[3:0]

These refer to two-wire accessible register number 18, or 0x12 hexadecimal, located on page 1. [3:0] indicate bits. Registers numbers range 0..255 and bits range 15..0.

How to Access

Registers are accessed as follows:

Registers

Hardware registers are organized into several pages. Page 0 contains sensor controls. Page 1 contains color pipeline controls. The desired page is selected by writing the desired value to R0x01. After that all READs and WRITEs to registers except R0x01, is directed to the selected page. R0x01 is a special register and is present on all pages. See details in following tables for usage of R0x01.

Sensor Core Registers

Table 1: Sensor Core Register List

Register		Description	Default Value	
Dec	Hex		Dec	Hex
0	0x00	Reserved	-	-
1	0x01	Register Address Select	1	0x01
2	0x02	Column Start[1]	18	0x0012
3	0x03	Window Height[1]	487	0x01E7
4	0x04	Window Width[1]	647	0x0287
5	0x05	Horizontal Blanking	38	0x0026
6	0x06	Vertical Blanking[1]	4	0x0004
7	0x07	Output Control[1]	12306	0x3012
8	0X08	Row Start[1]	6	0x0006
9	0x09	Shutter Width[2]	248	0x00F8
10	0x0A	Reserved	0	0x0000
11	0x0B	Reserved	0	0x0000
12	0x0C	Shutter Delay[2]	0	0x0000
13	0x0D	Reserved	0	0x0000
18	0x12	2X Zoom Col Start	176	0x00B0
19	0x13	2X Zoom Row Start	124	0x007C
30	0x1E	Digital Zoom	0	0x0000
32	0x20	Read Mode	4096	0x1000
33	0x21	Reserved	0	0x0000
34	0x22	Reserved	0	0x0000
39	0x27	Reserved	36	0x0024
40	0x28	Reserved	0	0x0000
43	0x2B	Green1 Gain[2]	32	0x0020
44	0x2C	Blue Gain[2]	32	0x0020
45	0x2D	Red Gain[2]	32	0x0020
46	0x2E	Green2 Gain[2]	32	0x0020
47	0x2F	Reserved	63408	0xF7B0
48	0x30	Reserved	30725	0x7805
49	0x31	Reserved	42	0x002A
50	0x32	Reserved	0	0x0000
51	0x33	Reserved	12303	0x300F
52	0x34	Reserved	256	0x0100
53	0x35	Global Gain[2]	32	0x0020
54	0x36	Chip Version (R/O)	33338	0x823A
55	0x37	Reserved	10	0x000A
59	0x3B	Reserved	N/A	
60	0x3C	Reserved	2080	0x0820
61	0x3D	Reserved	1679	0x068F
62	0x3E	Reserved	N/A	
63	0x3F	Reserved	1696	0x06A0
64	0x40	Reserved	480	0x01E0
65	0x41	Reserved	209	0x00D1
66	0x42	Reserved	2178	0x0882

Table 1: Sensor Core Register List (continued)

Register		Description	Default Value	
Dec	Hex		Dec	Hex
88	0x58	Reserved	248	0x00F8
89	0x59	Reserved	1859	0x0743
90	0x5A	Reserved	1063	0x0427
91	0x5B	Reserved	R/O	
92	0x5C	Reserved	R/O	
93	0x5D	Reserved	R/O	
94	0x5E	Reserved	R/O	
95	0x5F	Reserved	41757	0xA31D
96	0x60	Reserved	0	0x0000
97	0x61	Reserved	0	0x0000
98	0x62	Reserved	1048	0x0418
99	0x63	Reserved	0	0x0000
100	0x64	Reserved	0	0x0000
101	0x65	Reserved	0	0x0000
241	0xF1	Reserved	1	0x0001
247	0xF7	Reserved	R/O	
248	0xF8	Reserved	R/O	
249	0xF9	Reserved	44	0x002C
250	0xFA	Reserved	R/O	
251	0xFB	Reserved	R/O	
252	0xFC	Reserved	R/O	
253	0xFD	Reserved	R/O	
255	0xFF	Chip Version (R/O)	33338	0x823A

Notes:
1. Do not change these registers. Contact Aptina support for settings different from defaults.
2. IFP controls these registers when AE, AWB, or flicker avoidance are enabled.

Table 2: Sensor Core Register Description

Register Dec Hex	Bit	Description
Register Address Selector		
1 0X01	0	Selects the IFP/SOC registers (0–170). 001= Select IFP registers—default = 0x01.
	2	Selects the core registers (0–255). 100 = Select core registers.
Window Control These registers control the size of the window. Register values are one less than actual height and width.		
2 0x02	9:0	First column to be read out—default = 0x0012 (18). See R0x08 for row adjustment.
3 0x03	8:0	Window height (number of rows - 1)—default = 0x01E7 (487).
4 0x04	9:0	Window width (number of columns - 1)—default = 0x0287 (647). Minimum value for R0x04 = 0x0009.
Blanking Control These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. Register values are one less than actual height and width.		
5 0x05	9:0	Horizontal blanking (number of columns)—default = 0x0026 (38 pixel clocks). Minimum value for R0x05 = 0x009.
6 0x06	11:0	Vertical Blanking (number of rows -1)—default = 0x0004 (4 rows). Minimum recommended value for R0x06 = 0x0003.
Output Control This register controls various features of the output format for the sensor.		
7 0x07	1:0	Reserved.
	4	Controls internal sampling time. This must be “0” when CLK_IN frequency is greater than 13.5 MHz.
	15:5	Reserved.
Row Start		
8 0x08	8:0	First row to be read out. Default = 0x0006 (6). Minimum value for R0x08 = 0x0004.
Pixel Integration Control		
9 0x09	11:0	Number of rows of integration—default = 0x00F8 (248). These registers (along with the window sizing and blanking registers) control the integration time for the pixels. R0x09: number of rows of integration R0x0C: reset delay, default = 0x0000 (0). This is the number of master clocks that the timing and control logic waits before asserting the reset for a given row. The actual total integration time, t_{INT}, is: t_{INT} = R0x09 x Row Time - Overhead Time - Reset Delay, where: Row Time = (R0x04 + 1 + 113 + R0x05) x 2 master clock periods Overhead Time = K x 57 master clock periods Reset Delay = K x R0x0C master clock periods If the value in R0x0C exceeds (row time - 444)/K master clock cycles, the row time will be extended by (K x R0x0C - (row time - 444)) clock cycles where K = 4 when R0x07[4] = 0 and K = 2 when R0x07[4] = 1 In this expression, the row time term corresponds to the number of rows integrated. The overhead time is the time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay. Typically, the value of R0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If R0x09 is increased beyond the total number of rows per frame, the MT9V131 will add additional blanking rows as needed.

Table 2: Sensor Core Register Description (continued)

Register Dec Hex	Bit	Description
Shutter Delay		
12 0x0C	9:0	Default = 0x0000 (0). This is the number of master clocks x K that the timing and control logic waits before asserting the reset for a given row.
Reset (Soft)		
13 0x0D	0	This register is used to reset the sensor to its default, power-up state. To reset, first write a "1" into bit 0 of this register to put the MT9V131 in reset mode, then write a "0" into bit 0 to resume operation.
2X Zoom		
18 0x12	9:0	Address of starting column in 2X zoom mode. Bit 0 of R0x1E must be set.
19 0x13	8:0	Address of starting row in 2X zoom mode. Bit 0 of R0x1E must be set.
30 0x1E	0	Zoom by 2X. This bit must be set when using R0x12 and R0x13.
Read Mode		
32 0x20	This register is used to control many aspects of the readout of the sensor. To preserve a right-reading image and the correct color order, all four of these bits should be set to "1" to invert the image.	
	5	1 = readout starting 1 column later. 0 = normal readout.
	7	1 = readout starting 1 row later. 0 = normal readout.
	14	1 = read out from right to left (mirrored). 0 = normal readout.
	15	1 = read out from bottom to top (upside down). 0 = normal readout.
Gain Settings The gain is individually controllable for each color in the Bayer pattern, as shown in the register chart. Formula for gain setting: Gain = (Bit [8] + 1) x (Bit [7] + 1) x (Bit [6–0] x 0.03125) Since bit [7] and bit [8] of the gain registers are multiplicative factors for the gain settings, there are alternate ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings: Gain — Increments — Recommended Settings 1.000 to 1.969 — 0.03125 — 0x020 to 0x03F 2.000 to 7.938 — 0.0625 — 0x0A0 to 0x0FF 8.000 to 15.875 — 0.125 — 0x1C0 to 0x1FF		
43 0x2B		Green1 gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
44 0x2C		Blue Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
45 0x2D		Red Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain.)
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).

Table 2: Sensor Core Register Description (continued)

Register Dec Hex	Bit	Description
46 0x2E		Green2 Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain each bit gives 2x gain).
	9,10	Total gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
Global Gain		
53 0x35		Global Gain—default = 0x0020 (32) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in R0x2B.
	6:0	Initial Gain = bits (6:0) x 0.03125
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
Chip Version		
54 0x36	15:0	This read-only register contains the chip identification number. R0xFF (255) is a repeat of this register.
255 0xFF	15:0	Mirrors the chip identification in R0x36.

IFP Register List

Table 3: IFP Register List

Address		Defaults		Description
Dec	Hex	Dec	Hex	
0	0x00			Reserved
1	0x01	1	0x0001	Register Address Space Selection
2	0x02	110	0x006E	Color Correction Register 1
3	0x03	10531	0x2923	Color Correction Register 2
4	0x04	1316	0x0524	Color Correction Register 3
5	0x05	11	0x000B	Aperture Correction (Sharpening)
6	0x06	28686	0x700E	Operating Mode Control
7	0x07	0	0x0000	Image Flow Processor Soft Reset
8	0x08	51200	0xC800	Output Format Control
9	0x09	146	0x0092	Color Correction Register 4
10	0x0A	22	0x0016	Color Correction Register 5
11	0x0B	8	0x0008	Color Correction Register 6
12	0x0C	171	0x00AB	Color Correction Register 7
13	0x0D	147	0x0093	Color Correction Register 8
14	0x0E	88	0x0058	Color Correction Register 9
15	0x0F	77	0x004D	Color Correction Register 10
16	0x10	169	0x00A9	Color Correction Register 11
17	0x11	160	0x00A0	Color Correction Register 12
18	0x12	R/O		White Balance Register 1
19	0x13	R/O		White Balance Register 2
20	0x14	R/O		White Balance Register 3
21	0x15	373	0x0175	Color Correction Register 13
22	0x16	22	0x0016	Color Correction Register 14
23	0x17	67	0x0043	Color Correction Register 15
24	0x18	12	0x000C	Color Correction Register 16
25	0x19	0	0x0000	Color Correction Register 17
26	0x1A	21	0x0015	Color Correction Register 18
27	0x1B	31	0x001F	Color Correction Register 19
28	0x1C	22	0x0016	Color Correction Register 20
29	0x1D	152	0x0098	Color Correction Register 21
30	0x1E	76	0x004C	Color Correction Register 22
31	0x1F	160	0x00A0	AWB Cr/Cb Limits
32	0x20	51220	0xC814	Luminance Range of Pixels Considered in WB Statistics
33	0x21	0	0x0000	AWB Tint add-on color
34	0x22	55648	0xD960	White Balance Register 6
35	0x23	55648	0xD960	White Balance Register 7
36	0x24	32512	0x7F00	Limits on Color Correction Matrix Adjustment by AWB
37	0x25	17684	0x4514	AWB Speed and Color Saturation Control
38	0x26	65283	0xFF03	Horizontal Boundaries of AE Measurement Window
39	0x27	65296	0xFF10	Vertical Boundaries of AE Measurement Window
40	0x28	26624	0x6800	White Balance Register 9
41	0x29	36211	0x8D73	White Balance Register 10
42	0x2A	128	0x0080	STD Limits for Definition of a Monochrome Zone

Table 3: IFP Register List (continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
43	0x2B	30760	0x7828	Horizontal Boundaries of AE Measurement Window for Back Light Compensation
44	0x2C	46140	0xB43C	Vertical Boundaries of AE Measurement Window for Back Light Compensation
45	0x2D	57504	0xE0A0	Boundaries of AWB Measurement Window
46	0x2E	4196	0x1064	AE Target and Accuracy Control
47	0x2F	68	0x0044	AE Speed and Sensitivity Control
48	0x30	R/O		Red AWB Measurement
49	0x31	R/O		Luma AWB Measurement
50	0x32	R/O		Blue AWB Measurement
51	0x33	5230	0x146E	Auto Exposure Register 1
52	0x34	16	0x0010	Luminance Offset Control
53	0x35	61456	0xF010	Clipping Limits for Output Luminance
54	0x36	30736	0x7810	Imager Gain Limits for AE Adjustment
55	0x37	768	0x0300	Shutter Width Limits for AE Adjustment (Day/Night Mode)
56	0x38	1144	0x0478	Auto Exposure Register 3
57	0x39	680	0x02A8	Upper Shutter Delay Limit
58	0x3A	0	0x0000	Output Format Control 2
59	0x3B	1066	0x042A	Black Level Register 1
60	0x3C	1024	0x0400	IFP Black Level Addition
61	0x3D	4570	0x11DA	AE Limits for AE Adjustment
62	0x3E	3327	0x0CFF	Gain Threshold for CCM Adjustment
63	0x3F	0	0x0000	Auto Exposure Register 6
64	0x40	7696	0x1E10	Auto Exposure Register 7
65	0x41	5143	0x1417	ADC Voltage References
66	0x42	26128	0x6610	Auto Exposure Register 9
67	0x43	28010	0x6D6A	Auto Exposure Register 10
68	0x44	29040	0x7170	Auto Exposure Register 11
69	0x45	29811	0x7473	Auto Exposure Register 12
70	0x46	0	0x0000	AE Luminance Threshold for Entering Zone 0
71	0x47	24	0x0018	Defect Correction Register 1
72	0x48	0	0x0000	Test Pattern Generator
74	0x4A	R/O		Reserved
75	0x4B	R/O		Reserved
76	0x4C	R/O		Current Measured Luma
77	0x4D	R/O		Time Averaged Measured Luma
78	0x4E	16	0x0010	Reserved
79	0x4F	R/O		Reserved
82	0x52	R/O		Reserved
83	0x53	7700	0x1E14	Gamma Correction Register 1
84	0x54	17966	0x462E	Gamma Correction Register 2
85	0x55	34666	0x876A	Gamma Correction Register 3
86	0x56	47008	0xB7A0	Gamma Correction Register 4
87	0x57	57548	0xE0CC	Gamma Correction Register 5
88	0x58	0	0x0000	Gamma Correction Register 6

Table 3: IFP Register List (continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
89	0x59	248	0x00F8	Shutter Width For One Frame Integration Time For 60Hz AC
90	0x5A	298	0x012A	Shutter Width For One Frame Integration Time For 50Hz AC
91	0x5B	2	0x0002	Flicker Control
92	0x5C	4366	0x110E	Searched Flicker Period at 60Hz
93	0x5D	5137	0x1411	Searched Flicker Period at 50Hz
94	0x5E	26684	0x683C	Color Correction Register 23
95	0x5F	12296	0x3008	Color Correction Register 24
96	0x60	2	0x0002	Color Correction Register 25
97	0x61	R/O		Reserved
98	0x62	4112	0x1010	AE Digital Gains
99	0x63	R/O		Reserved
100	0x64	5499	0x157B	Reserved
102	0x66	R/O		Reserved
103	0x67	16400	0x4010	AE Digital Gains Limit
104	0x68	17	0x0011	Reserved
105 – 125	0x69 – 0x8D	R/O		Reserved
127	0x7F	N/A		8-bit Serial Interface Helper
128	0x80	6	0x0006	Lens Correction Control
129	0x81	56588	0xDD0C	Lens Shading Parameters
130	0x82	1268	0x04F4	Lens Shading Parameters
131	0x83	15377	0x3C11	Lens Shading Parameters
132	0x84	57868	0xE20C	Lens Shading Parameters
133	0x85	758	0x02F6	Lens Shading Parameters
134	0x86	12817	0x3211	Lens Shading Parameters
135	0x87	56588	0xDD0C	Lens Shading Parameters
136	0x88	244	0x00F4	Lens Shading Parameters
137	0x89	12822	0x3216	Lens Shading Parameters
138	0x8A	34866	0x8832	Lens Shading Parameters
139	0x8B	63453	0xF7DD	Lens Shading Parameters
140	0x8C	15372	0x3C0C	Lens Shading Parameters
141	0x8D	127	0x007F	Lens Shading Parameters
142	0x8E	47646	0x6A1E	Lens Shading Parameters
143	0x8F	63468	0xF7EC	Lens Shading Parameters
144	0x90	14088	0x3708	Lens Shading Parameters
145	0x91	100	0x0064	Lens Shading Parameters
146	0x92	48926	0x6F1E	Lens Shading Parameters
147	0x93	63470	0xF7EE	Lens Shading Parameters
148	0x94	12815	0x320F	Lens Shading Parameters
149	0x95	100	0x0064	Lens Shading Parameters
152	0x98	1040	0x0410	Flash Control
153	0x99	R/O		Line Counter
154	0x9A	R/O		Frame Counter
155	0x9B	R/O		Reserved
156	0x9C	8	0x0008	Reserved

Table 3: IFP Register List (continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
157	0x9D	42158	0xA4AE	Reserved
158	0x9E	R/O		Reserved
165	0xA5	0	0x0000	Horizontal Pan In Decimation
166	0xA6	640	0x0280	Horizontal Zoom In Decimation
167	0xA7	640	0x0280	Horizontal Output Size In Decimation
168	0xA8	0	0x0000	Vertical Pan In Decimation
169	0xA9	480	0x01E0	Vertical Zoom In Decimation
170	0xAA	480	0x01E0	Vertical Output Size In Decimation

IFP Register Description

Table 4: IFP Register Description

Register Dec Hex	Bits	Default Dec(Hex)	Description
1 0x01	7:0	1(0x0001)	Register address space selection.
	This register controls the address space for the two-wire serial interface communications. Set R0x01 = 1 to select IFP address space and R0x01 = 4 for sensor space. R0x01 is always accessible regardless of the page currently selected.		
5 0x05	3:0	11(0x000B)	Aperture correction (sharpening).
	2:0	3	Sharpening factor: 000: No sharpening. 001: 25% sharpening. 010: 50% sharpening. 011: 75% sharpening. 100: 100% sharpening. 101: 125% sharpening. 110: 150% sharpening. 111: 200% sharpening.
	3	1	Automatically reduces sharpness in low light.
6 0x06	15:0	28686(0x700E)	Operating mode control.
	15	0	Reserved.
	14	1	0: Disables auto exposure 1: Enables auto exposure.
	13	1	0: Disables on-the-fly defect correction. 1: Enables on-the-fly defect correction.
	12	1	Enable aperture correction knee.
	11:10	0	Reserved.
	9:8	0	N/A
	7	0	0: Normal operation. 1: ITU_R BT.656 synchronization codes are embedded in the image.
	6:5	0	Reserved.
	4	0	0: Normal color processing. 1: Bypass color correction matrix.
	3:2	3	Back light compensation: 00: AE measurement window is specified by R0x0026 and R0x0027 (large window). 01: AE measurement window is specified by R0x002B and R0x002C (center window). 10 and 11: AE measurement window is a weighted sum of large window and center window with center window given twice the weight.
	1	1	0: Stops AWB at the current values. 1: Enables auto white balance.
	0	0	Reserved.
7 0x07	0	0	Image flow processor soft reset.
	Asserts reset on all IFP registers. Example: Write R0x07 = 1 followed by R0x07 = 0 to reset IFP.		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
8 0x08	15:0	51200	Output format control.
	15:14	1	Reserved.
	13	0	N/A
	12	0	0: Output mode is YCbCr. See also R0x3A[7:6]. This bit is subject to synchronous update, see R0xA5. 1: Output mode is RGB.
	11	1	Enable automatic flicker avoidance.
	10	0	Reserved.
	9	0	Inverts output pixel clock.
	8	0	0: Disables lens shading correction. 1: Enables lens shading correction.
	7	0	Entire image processing is bypassed and raw 8+2 Bayer data output directly.
	6	0	N/A
	5	0	Monochrome. Forces Cr=Cb=128 in YCbCr or R,B = G in RGB mode.
	4	0	Disable Cb. Force output Cb = 128 in YCbCr mode and B = 0 in RGB.
	3	0	Disable Y. Force output Y = 128 in YCbCr mode and G = 0 in RGB.
	2	0	Disable Cr. Forces output Cr = 128 in YCbCr mode and R = 0 in RGB.
	1	0	Toggles the assumption about Bayer CFA (vertical shift). 0: Green comes first. 1: Red or blue comes first.
	0	0	Toggles the assumption about Bayer CFA (horizontal shift). 0: Row containing blue comes first. 1: Row with red comes first.
31 0x1F	7:0	160	AWB Cr/Cb limits.
	7:6	2	Relative limit
	5:0	32	Absolute limit
	In order to avoid skewing WB statistics by deeply saturated colored areas this register allows programming the color range of pixels to be used for WB computation. The chroma check passes if the relative or absolute limits are met. Absolute limit on Cb/Cr values considered by WB: Cb and Cr < 2*R0x1F[5:0]. Relative limit on Cb/Cr values considered by WB: 00: Check disabled 01: Cb and Cr < 0.25 * max(R,G,B) after WB gain 10: Cb and Cr < 0.5 * max(R,G,B) after WB gain 11: Cb and Cr < max(R,G,B) after WB gain		
32 0x20	15:0	51220	Luminance Range of Pixels Considered in WB Statistics
	15:8	200	Upper limit.
	7:0	20	Lower limit.
	To avoid skewing WB statistics by very dark or very bright values, this register allows programming the luminance range of pixels to be used for WB computation.		
33 0x21	15:0	0	AWB tint.
	15:8	0	Red channel add-on.
	7:0	0	Blue channel add-on.
	In the AWB mode, this register specifies gain “add-ons” to the values determined by AWB, allowing to “skew” the overall color of the image.		
36 0x24	14:0	32512	Limits on color correction matrix adjustment by AWB
	14:8	1270	Upper limit.

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
	7:0	0	Lower limit.
	As described in R0x12, AWB determines the best position of the color correction matrix by interpolating between 2 “corner” matrices: one for red-rich illumination and one for blue-rich illumination. The current position of the matrix is expressed as a number from 0 to 127 (0 for red-rich illumination; 127 for blue-rich illumination). R0x24 specifies the limits imposed on the position of the matrix		
37 0x25	14:0	17700	AWB speed and color saturation control.
	14	1	1: Enables automatic color saturation control in low light. The automatic saturation control acts “in addition” to the saturation specified in bits 13:11.
	13:11	0	U/V saturation. Specify overall attenuation of the color saturation: 000: Full color saturation. 001: 75% of full saturation. 010: 50% of full saturation. 011: 37.5% of full saturation. 100: 25% of full saturation. 101: 150% of full saturation. 110: Black and white.
	10:8	5	Reserved.
	6:3	4	AWB speed. 000: Fastest. 111: Slowest.
	2:0	4	AWB reaction delay: 000: Fastest. 111: Slowest.
38 0x26	15:0	65283	Horizontal boundaries of AE measurement window.
	15:8	255	Right window boundary.
	7:0	3	Left window boundary.
	This register specifies left and right boundaries of the window used by AE measurement engine. The values programmed in the registers are desired boundaries divided by four.		
39 0x27	15:0	65296	Vertical boundaries of AE measurement window.
	15:8	255	Top window boundary.
	7:0	16	Bottom window boundary.
	This register specifies top and bottom boundaries of the window used by AE measurement engine. The values programmed in the registers are desired boundaries divided by two.		
42 0x2A	15:0	128	STD Limits for Definition of a Monochrome Zone
	15:8	0	MInimum number of open zones
	7:4	8	Upper limit of STD
	3:0	0	Lower limit of STD
	Current STD is changed incrementally from Min STD to Max STD and depends on current number of open zones in compare with threshold; see R0x28[14].		
43 0x2B	15:0	30760	Horizontal boundaries of AE measurement window for back light compensation.
	15:8	120	Right window boundary.
	7:0	40	Left window boundary.
	This register specifies left and right boundaries of the window used by AE measurement engine in backlight compensation mode, see R0x06[3:2]. The values programmed in the registers are desired boundaries divided by four.		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
44 0x2C	15:0	46140	Vertical boundaries of AE measurement window for back light compensation.
	15:8	180	Bottom window boundary.
	7:0	60	Top window boundary.
	This register specifies top and bottom boundaries of the window used by AE measurement engine in backlight compensation mode, see R0x06[3:2]. The values programmed in the registers are desired boundaries divided by two.		
45 0x2D	15:0	57504	Boundaries of AWB measurement window.
	15:12	14	Bottom window boundary.
	11:8	0	Top window boundary.
	7:4	10	Right window boundary.
	3:0	0	Left window boundary.
	This register specifies the boundaries of the window used by AWB measurement engine. The values programmed in the registers are desired boundaries divided by 32 for vertical limits and by 64 for horizontal.		
46 0x2E	15:0	4196	Auto exposure target and accuracy control.
	15:8	16	Tracking accuracy.
	7:0	100	Target luminance.
	This register specifies luminance target of the auto exposure algorithm and the size of the margin around the target in which no AE adjustment is made.		
47 0x2F	7:0	68	Auto exposure speed and sensitivity control.
	7:6	0	AE step size: 00: Medium speed when going down, slow when going up. 01: Medium speed. 10: Fast speed. 11: Fast when going down, medium when going up.
	5:3	0	AE speed: 000: Fastest. 111: Slowest.
	2:0	4	AE reaction delay: 000: Fastest. 111: Slowest.
48 0x30	7:0	RO	Normalized measure of red channel.
	This register outputs the measure of the red channel of the image as used by the AWB algorithm.		
49 0x31	7:0	RO	Normalized measure of luminance channel.
	This register outputs the measure of the luminance channel of the image as used by the AWB algorithm.		
50 0x32	7:0	RO	Normalized measure of blue channel.
	This register outputs the measure of the blue channel of the image as used by the AWB algorithm.		
52 0x34	15:0	16	Luminance offset control. Use this register to adjust LCD brightness.
	15:8	0	Offset in RGB mode.
	7:0	16	Y offset in YCbCr mode.
	This register specifies constant offset added to the luminance or RGB components prior to the output. Use this register to adjust LCD brightness.		
53 0x35	15:0	61456	Clipping limits for output luminance.
	15:8	240	Highest value of output luminance.
	7:0	16	Lowest value of output luminance.
	This register specifies upper and lower limits to which the output YCbCr data is clipped.		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
54 0x36	15:0	51220	Imager gain limits for AE adjustment
	15:8	120	Upper gain limit
	7:0	16	Lower gain limit
	This register specifies upper and lower imager gain limits for AE algorithm. The values refer to virtual gains rather than the gains that can be programmed in the R0x035. Virtual gains range from 1 to 255 and represent mapping of the actual gain settings into linearly increasing slope (virtual gain of 16 corresponds to actual analog gain of 1 and virtual gain of 255 corresponds to actual analog gain of 15.9375). The actual feasible gain limits are affected by the values programmed in R0x5E and R0x5F. The upper gain limit must be less than 240.		
55 0x37	9:0	768	Shutter width limits for AE adjustment (Day/Night mode)
	9:5	24	HIghest zone
	4:0	0	Lowest zone
	This register sets upper and lower limits on the shutter width used by AE module. All shutter widths that can be used by AE module are divided into 25 zones as follows: Zone 0 includes shutter widths from 1 line times up to ¼ of full frame time (where “full frame” is defined in R0x59, R0x5A), Zone 1 is ¼ of full frame time, Zones 2 through 24 corresponding to shutter widths increasing in ¼ of full frame time increments. If setting of highest zone allows the shutter width to exceed the sum of image array height and vertical blanking (sensor R0x09 > R0x03+R0x06+1), the frame rate will slow down correspondingly. In day mode set highest zone to a lower value to keep the frame rate high. In the night mode set highest zone to a higher value to allow long exposures to improve the image’s signal-to-noise ratio.		
57 0x39	9:0	290	Upper shutter delay limit
	When shutter width is less than 12 lines, AE uses the shutter delay register (R0x00C) to ensure smooth AE behavior. R0x39 is used to calculate correct values for sensor’s R0x00C.		
58 0x3A	7:0	0	Output format control 2.
	7:6	0	RGB output format: 00: 16-bit 565RGB. 01: 15-bit 555RGB. 10: 12-bit 444RGB. 11: 12-bit x444RGB.
	5	0	Output R,G,B or Cr,Y,Cb values are shifted 3 bits up; use with R0x3A[4:3] to test LCDs with low color depth.
	4:3	0	Test ramp output: 00: Off. 01: By column. 10: By row. 11: By frame.
	2	0	Average two nearby chrominance bytes.
	1	0	Swap chrominance byte with luminance byte in YCbCr/YUV output. In RGB, swap odd and even bytes. This bit is subject to synchronous update.
	0	0	In YUV output mode swaps Cb and Cr channels. In RGB, swaps R and B. This bit is subject to synchronous update.
60 0x3C	10:0	1024	IFP black level addition
	10	1	Enable black level addition
	9:0	0	Value of black signal
	This register specifies value of black signal added to raw data after applying lens shading correction and digital gains. Set this value to the black level desired for IFP processing. Setting bit 10 to ‘1’ enables black level addition; setting it to ‘0’ disables black level addition.		
61 0x3D	13:0	4570	ADC limits for AE adjustment
	13	0	Alt. analog gain scheme
	12	1	Change simultaneously

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
	11:8	1	Low VrefLo limit
	7:4	13	Upper VrefHi limit
	3:0	10	Low VrefHi limit
	This register specifies upper and lower imager ADC voltage reference for AE algorithm. When R0x3D[3:0] < R0x3D[7:4], AE can manipulate ADC reference voltages to create additional analog gain		
62 0x3E	11:0	4095	Gain threshold for CCM adjustment
	11:10	13	Select gain type
	9:8	3	Select gain type
	7:0	255	Threshold to disable CCM in the dark
	CCM is allowed to adjust only when R0x34[7:0] is greater than the current virtual analog gain. R0x3E[9:8] and [11:10] select the gain type for R0x33. 00: Virtual analog gain; 01: ADC Vref_lo; 10: Digital gain; 11: LC digital gain.		
65 0x41	7:0	209	ADC voltage references
	7:4	13	Vref_hi (ADC “top” voltage reference)
	3:0	1	Vref_lo (ADC “bottom” voltage reference)
	This register sets the on-chip voltage references The ADC references can be determined from the following formula: Vref_hi = 969mV + 55.368mV * ((Reg0x41, bits 7:4)+6) Default = 0xD = Vref_hi = 2.021V Vref_lo = 969mV + 55.368mV * (Reg0x41, bits 3:0) Default = 0x1 = Vref_lo = 1.024V ADC Vref = Vref_hi - Vref_lo The default programmed value for ADC Vref = 0.997V. This is the recommended operational setting.		
70 0x46	7:0	0	AE luminance threshold for entering zone 0
	In bright indoor conditions this threshold delays reduction of integration time below zone 1. This helps avoiding the appearance of flicker in the image, but the image may become overexposed.		
72 0x48	7:0	0	Test pattern generator.
	7	0	1: Force WB digital gains to 1.0.
	2:0	0	Test pattern selection.
	This register enables color bar test-pattern generation at the input of the image processor. Values greater than "0" turn test pattern generation on. The brightness of the flat-color areas depends on the value programmed in this register.		
76 0x4C	7:0	0	Current measured luma.
	Luma measured by AE engine. See also R0x2E, R0x3F, R0x4D and backlight control in R0x06[3:2].		
77 0x4D	7:0	0	Time-averaged measured luma
	Time-averaged luminance value tracked by autoexposure, see R0x4C.		
89 0x59	11:0	248	Shutter Width For One Frame Integration Time For 60Hz AC
	Shutter Width For One Frame Integration Time For 60Hz AC		
90 0x5A	11:0	248	Shutter Width For One Frame Integration Time For 50Hz AC
	Shutter Width For One Frame Integration Time For 50Hz AC		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
91 0x5B	2:0	2	Flicker control.
	1	1	Manual 50/60 When in "manual" flicker mode (R0x15B[0]=1), this defines which flicker frequency to avoid. 0: 50Hz. 1: 60Hz.
	0	0	0: Auto flicker detection. 1: Manual mode.
92 0x5C	15:0	4366	Searched flicker period at 60Hz
	15:8	17	Max search flicker period
	7:0	14	Min search flicker period
	Searched Flicker Period at 60Hz		
93 0x5D	15:0	5137	Searched flicker period at 50Hz
	15:8	20	Max search flicker period
	7:0	17	Min search flicker period
	Searched Flicker Period at 50Hz		
98 0x62	15:0	4112	AE digital gains.
	15:8	16	Current digital gain applied during lens shading correction.
	7:0	16	Current digital gain applied before lens shading correction.
	When R0x06 [14] = 1, registers are read-only and show current digital gains. When R0x06 [14] = 0, writing into registers sets current digital gains. LC digital gain, R0x62 [15:8], is unity if LC is disabled, R0x08 [8] = 0. The combined gain of R0x62 [15:8] and LC must be less than 16. See also R0x67.		
103 0x67	15:0	16400	AE digital gains limits.
	15:8	64	Maximal digital gain applied during lens shading correction.
	7:0	16	Maximal digital gain applied before lens shading correction.
	Value 16 corresponds real digital gain of 1.0. As AE increases gain in dark conditions, pre-LC gain is used first. Post-LC gain is used only after pre-LC gain reaches its maximum allowed limit. See also R0x62.		
127 0x7F	7:0	0	8-bit, two-wire serial interface helper.
	Internal MT9V131 registers are up to 16 bits wide. To execute 16-bit reads and writes, 8-bit two-wire serial interface devices need special handling by using R0x7F. A 16-bit write is done by writing the upper 8 bits to the desired register and then writing the lower 8 bits to R0x7F. The register is not updated until all 16 bits have been written. It is not possible to just update half a register. To read 8 bytes at a time, read the upper 8 bits from the desired register; then read the lower 8 bits from R0x7F.		
128 0x80	6:0	4095	Lens correction control
	6	3	Enable LC in 2x zoom mode (R0x01E)
	4:2	3	Scale coefficient
	1:0	255	Scale factor LC parameters
	Scale factor for LC parameters. 00: 1 01: 0.5 10: 0.25 11: 0.125 Scale coefficient for cross term. 000: 0 001: 1 010: 2 011: 4		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
129 0x81	15:0	56588	Lens shading parameters
	15:8	221	Red vertical knee point 0
	7:0		Red vertical initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
130 0x82	15:0	1268	Lens shading parameters
	15:8	4	Red vertical knee point 2
	7:0	244	Red vertical knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
131 0x83	15:0	15377	Lens shading parameters
	15:8	60	Red vertical knee point 4
	7:0	17	Red vertical knee point 3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
132 0x84	15:0	57868	Lens shading parameters
	15:8	226	Green vertical knee point 0
	7:0	12	Green vertical initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
133 0x85	15:0	758	Lens shading parameters
	15:8	2	Green vertical knee point 2
	7:0	246	Green vertical knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
134 0x86	15:0	758	Lens shading parameters
	15:8	2	Green vertical knee point 4
	7:0	246	Green vertical knee point 3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
135 0x87	15:0	56588	Lens shading parameters
	15:8	221	Blue vertical knee point 0
	7:0	12	Blue vertical initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
136 0x88	15:0	244	Lens shading parameters
	15:8	0	Blue vertical knee point 2
	7:0	244	Blue vertical knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
137 0x89	15:0	12822	Lens shading parameters
	15:8	50	Blue vertical knee point 4
	7:0	22	Blue vertical knee point 3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
138 0x8A	15:0	34866	Lens shading parameters
	15:8	136	Red horizontal knee point 0
	7:0	50	Red horizontal initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
139 0x8B	15:0	63453	Lens shading parameters
	15:8	247	Red horizontal knee point 2
	7:0	221	Red horizontal knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
140 0x8C	15:0	15372	Lens shading parameters
	15:8	60	Red horizontal knee point 4
	7:0	12	Red horizontal knee point3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
141 0x8D	15:0	127	Lens shading parameters
	15:8	127	Red horizontal knee point 5
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
142 0x8E	15:0	47646	Lens shading parameters
	15:8	186	Green horizontal knee point 0
	7:0	30	Green horizontal initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
143 0x8F	15:0	63486	Lens shading parameters
	15:8	247	Green horizontal knee point 2
	7:0	236	Green horizontal knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
144 0x90	15:0	14088	Lens shading parameters
	15:8	55	Green horizontal knee point 4
	7:0	8	Green horizontal knee point 3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
145 0x91	15:0	100	Lens shading parameters
	15:8	100	Green horizontal knee point 5
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
146 0x92	15:0	48926	Lens shading parameters
	15:8	191	Blue horizontal knee point 0
	7:0	30	Blue horizontal initial value
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
147 0x93	15:0	32750	Lens shading parameters
	15:8	127	Blue horizontal knee point 2
	7:0	238	Blue horizontal knee point 1
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
148 0x94	15:0	12815	Lens shading parameters
	15:8	50	Blue horizontal knee point 4
	7:0	15	Blue horizontal knee point 3
	Negative numbers for derivatives defined in complementary code 0xFF = –1		
149 0x95	15:0	100	Lens shading parameters
	15:8	100	Blue horizontal knee point 5
	Negative numbers for derivatives defined in complementary code 0xFF = –1		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
152 0x98	15:0	1040	Flash control.
	15	R/O	State of the output flash pin.
	14	R/O	1: Flash has fired in current frame.
	13	0	Write'1' to arm flash and set it to fire. Flash will fire after delay set in R0x98[12:11].
	12:11	0	Delay; skips programmed number of frames after arming and before firing.
	10	1	Strobe source select. 0: End of frame enable. 1: End of shutter enable.
	9	0	0: Fire only once per arming. 1: Fire every frame continuously.
	8	0	Invert pin state.
	7:0	16	Strobe duration, x512 CLK_IN. Value of 255 is special, enabling infinite duration.
	The flash control supports both xenon and LED light sources using a dedicated output pad. For xenon flashes, the pad generates a strobe to fire when the imager's shutter is fully open. For LED, the pad can be asserted or de-asserted asynchronously. To turn LED off and on program R0x198 [8]. To fire a xenon flash, arm the strobe trigger by setting R0x198[13] = 1. The strobe will appear when the shutter fully opens. Strobe length is set by R0x198[7:0]. Other available modes include continuous versus single firing and skipping a programmable number of frames after arming and before firing.		
153 0x99	12:0	R/O	Line counter.
	Use line counter to determine the number of line currently being output.		
154 0x9A	15:0	R/O	Frame counter.
	Use frame counter to determine number of frames output so far.		
165 0xA5	15:0	0	Horizontal pan in decimation.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	9:0	0	Horizontal pan.
	Decimation control registers work to downsize output image to any size. The output image size is specified in R0xA7 and R0xAA for horizontal and vertical directions, respectively. For example, to downsize the VGA output to QQVGA, set R0xA7 = 160 and R0xAA = 20. Whenever output image is downsized, the zoom feature becomes available. To zoom in, program R0x00A6 and R0xA9 with the size of window to be decimated. For example, in QQVGA setting R0x00A6 = 320 and R0xA9 = 240 results in 2X zoom. Here the output image of 160 x 120 is created from a pre-decimation window of 320 x 240, instead of the full VGA 640 x 480. Whenever the output image is zoomed, pan controls become available.To pan a zoomed image program, R0xA5 and R0xA8 need to offset the pre-decimation window into the right and bottom, respectively. When implementing a smooth zoom and pan, it is useful to synchronize the update of all decimation registers to avoid jumps in the output video. When writing a batch of decimation settings, set bit 15 of each datum to"1" to freeze the update. Set bit 15 of the last datum in the batch to "0" to enable normal operation. The entire batch of decimation settings will then be synchronously loaded on the next frame start.		
166 0xA6	15:0	640	Horizontal zoom in decimation.
	9:0	640	Horizontal size of window before decimation.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	See R0xA5 for details.		
167 0xA7	15:0	640	Horizontal output size in decimation.
	9:0	640	Horizontal size of output image.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	See R0xA5 for details.		

Table 4: IFP Register Description (continued)

Register Dec Hex	Bits	Default Dec(Hex)	Description
168 0xA8	15:0	0	Vertical pan in decimation.
	8:0	0	Vertical pan.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	See R0xA5 for details.		
169 0xA9	15:0	480	Vertical zoom in decimation.
	8:0	480	Vertical size of window before decimation.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	See R0xA5 for details.		
170 0xAA	15:0	480	Vertical output size in decimation.
	8:0	480	Vertical size of output image.
	15	0	0: Normal operation. 1: Freeze update of decimation parameters.
	See R0xA5 for details.		

Revision History

Rev. B **5/12**

- Updated trademarks
- Applied updated Aptina template

Rev. A **12/09**

- Copied register tables from data sheet to new document

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