1/4-Inch System-On-A-Chip (SOC) VGA NTSC and PAL CMOS Digital Image Sensor

MT9V135 Data Sheet

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

Features

- System-on-a-chip (SOC)—completely integrated camera system
- NTSC and PAL (true two field) analog composite video output
- Low power, interlaced scan CMOS image sensor
- ITU-R BT.656 parallel output (8-bit, interlaced)
- Serial LVDS data output
- Supports use of external devices for addition of custom overlay graphics
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing
- Color recovery and correction, sharpening, gamma, lens shading correction, and on-the-fly defect correction
- Automatic Features: Auto exposure (AE), auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Simple two-wire serial programming interface

Applications

- 900 MHz and 2.4 GHz wireless cameras
- Composite video and digital video out cameras
- CCTV security cameras
- Consumer video products
- Smart cameras
- Evidence quality cameras
- Cameras with the need for active or passive overlay

Data Sheet Applicable To Silicon Revision: Rev4

Table 1: Ordering Information

Part Number	Description
MT9V135C12STC	48-Pin CLCC ES (color)
MT9V135C12STCD ES	48-pin CLCC ES Demo Kit (color)
MT9V135C12STCH ES	48-pin CLCC ES Headboard (color)

Table 2: Key Performance Parameters

Parameter		Typical Value
Optical format		1/4-inch (4:3)
Active imager size		3.63mm(H) x 2.78mm(V) 4.57mm diagonal
Active pixels		640H x 480V
NTSC output		720H x 486V
PAL output		720H x 576V
Pixel size		5.6µm x 5.6µm
Color filter array		RGB paired Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		13.5 Mp/s 27 MHz
Frame rate (VGA 640H x 480V)		30 fps at 27 MHz (NTSC) 25 fps at 27 MHz (PAL)
Integration time		16µs–33ms (NTSC) 16µs–40ms (PAL)
ADC resolution		10-bit, on-chip
Responsivity		5 V/lux-sec (550nm)
Pixel dynamic range		70dB
SNR_{MAX}		39dB
Supply voltage	I/O digital	2.5–3.1V (2.8V nominal)
	Core digital	2.5–3.1V (2.8V nominal)
	Analog	2.5–3.1V (2.8V nominal)
Power consumption[1]	Operating	320mW
	Standby	0.56mW
Operating temperature[1]		–30°C to +70°C
Package		48-pin CLCC

Notes: 1. Measured at 2.8V, 30 fps, 25°C.
2. Customers requiring a similar part with greater temperature range should consider using the MT9V125.

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General Description

The Aptina MT9V135 is a VGA-format, single-chip camera CMOS active-pixel digital image sensor. It captures high-quality color images at VGA resolution and outputs NTSC or PAL interlaced composite video and CCIR 656 digital composite video.

This VGA CMOS image sensor features Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, low-power, and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9V135 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction.

The MT9V135 outputs interlaced-scan images at 30 or 25 fps, supporting both NTSC and PAL video formats.

The image data can be output on any one of three output ports:

- Composite analog video (support for both single-ended and differential-ended)
- Low-voltage differential signalling (LVDS)
- CCIR 656 interlaced digital video in parallel 8-bit format

Functional Overview

The MT9V135 is a fully-automatic, single-chip camera, requiring only a single power supply, lens, and clock source for basic operation. Output video is streamed through the chosen output port. The MT9V135 internal registers are configured using a two-wire serial interface.

The device can be put into a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry into standby mode can be achieved through two-wire serial interface register writes.

The MT9V135 requires an input clock of 27 MHz to support correct NTSC or PAL timing.

Internal Architecture

Internally, the MT9V135 consists of a sensor core and an image flow processor (IFP). The sensor core captures raw images that are then input into the IFP. The IFP is divided in two sections: the color pipe and the camera controller. The color pipe section processes the incoming stream to create interpolated, color-corrected output, and the camera controller section controls the sensor core to maintain the desired exposure and color balance.

The IFP scales the image and an integrated video encoder generates either NTSC or PAL analog composite output. The MT9V135 supports three different output ports: analog composite video out, LVDS serial out, and CCIR 656 interlaced digital video in parallel 8-bit format.

Figure 1 shows the major functional blocks of the MT9V135. Figure 2 demonstrates an MT9V135 usage scenario. A DSP takes the MT9V135's image output, overlays text, and feeds the resulting image back to the MT9V135 to be output as NTSC or PAL.

Figure 1: Functional Block Diagram

Figure 2: Typical Usage Configuration with Overlay

Note: The DSP shown is an external device, it is not part of the MT9V135.

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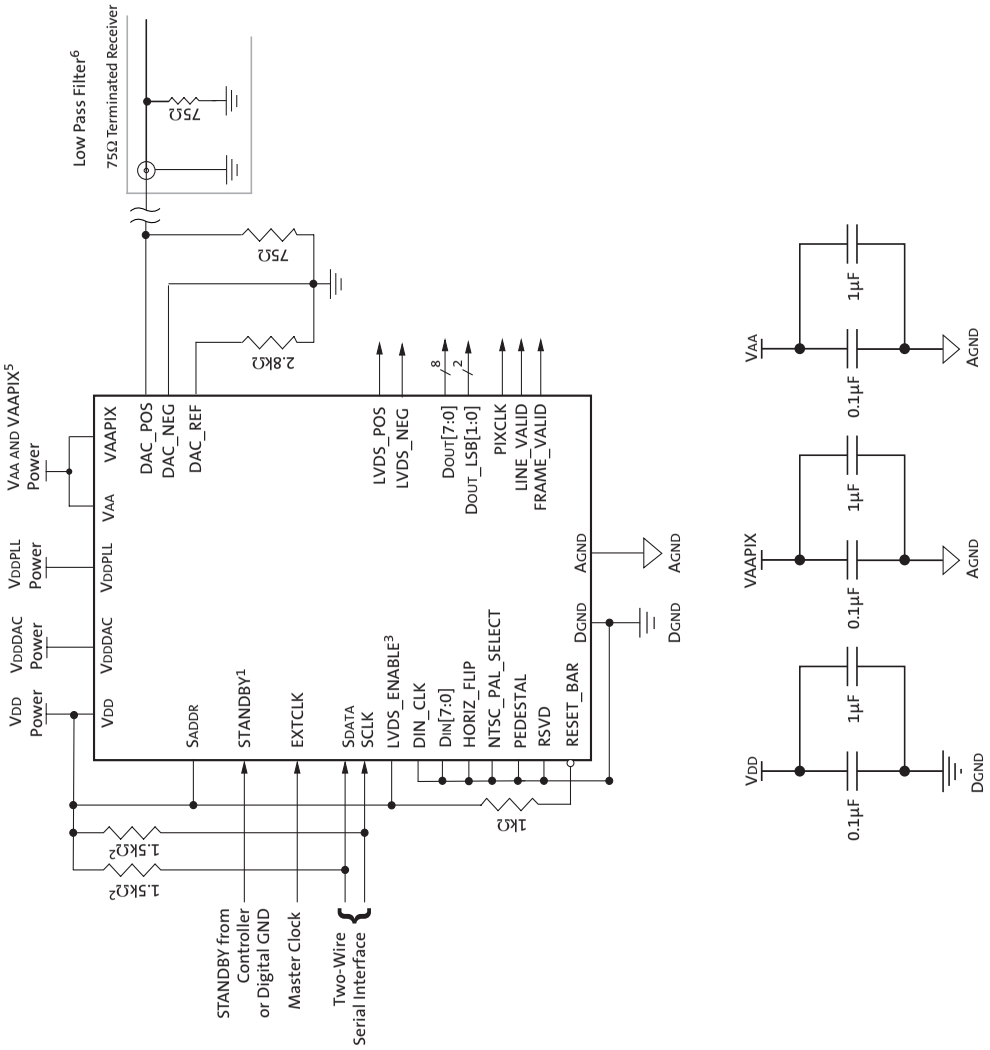
Typical Connections

Figure 3 shows a detailed MT9V135 device configuration. For low-noise operation, the MT9V135 requires separate analog and digital power supplies. Incoming digital and analog ground conductors can be tied together next to the die.

Power supply voltages V_{AA} (the primary analog voltage) and VAAPIX (the main voltage to the pixel array) must be tied together to avoid current loss. Both power supply rails should be decoupled to ground using high quality (X7R dielectric) capacitors. The MT9V135 requires a single external voltage supply level.

Figure 3: Typical Configuration Without Use of Overlay



Notes:
1. STANDBY can be connected directly to the customer's ASIC controller or to DGND, depending on the controller's capability.
2. A 1.5KΩ resistor value is recommended, but may be greater for slower two-wire speed (for example, 100 KB/s).
3. LVDS_ENABLE must be tied HIGH if LVDS is to be used.
4. Pull down DAC_REF with a 2.8KΩ resistor for 1.0V peak-to-peak video output.
5. VAA and VAAPIX must be tied to the same potential for proper operation.
6. Low pass filter (3dB attenuation at 4.2 MHz).

Pin Assignments

Figure 4 shows the location of the pin assignments on the MT9V135.

Figure 4: 48-Pin CLCC Assignment

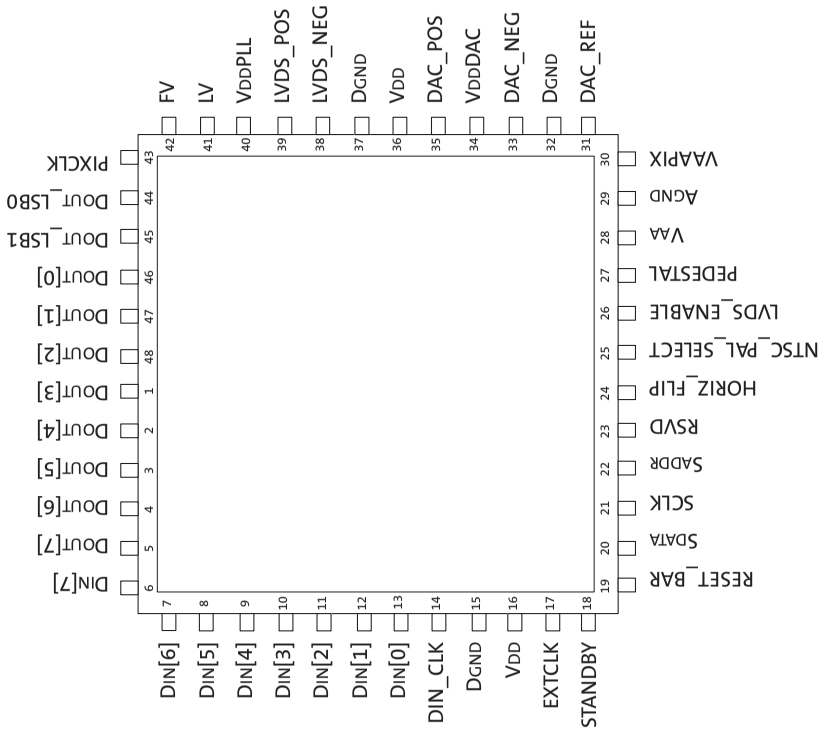


Table 3: Pin Descriptions

Pin Assignment	Name	Type	Description
17	EXTCLK	Input	Master clock in sensor.
19	RESET_BAR	Input	Active LOW: asynchronous reset.
22	SADDR	Input	Two-wire serial interface device ID selection 1:0xBA, 0:0x90.
23	RSVD	Input	Must be attached to DGND.
21	SCLK	Input	Two-wire serial interface clock.

Table 3: Pin Descriptions (continued)

Pin Assignment	Name	Type	Description
18	STANDBY	Input	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
24	HORIZ_FLIP	Input	If "0" at reset: Default horizontal setting. If "1" at reset: Flips the image readout format in the horizontal direction.
25	NTSC_PAL_SELECT	Input	If "0" at reset: Default NTSC mode. If "1" at reset: Default PAL mode.
27	PEDESTAL	Input	If "0" at reset: Does not add pedestal to composite video output. If "1" at reset: Adds pedestal to composite video output. Valid for NTSC only, pull LOW for PAL operation.
26	LVDS_ENABLE	Input	Active HIGH: Enables the LVDS output port. Must be HIGH if LVDS is to be used.
6, 7, 8, 9, 10, 11, 12, 13	DIN[7:0]	Input	External data input port selectable at video encoder input.
14	DIN_CLK	Input	DIN capture clock. (This clock must be synchronous to EXTCLK.)
20	SDATA	Output	Two-wire serial interface data I/O.
5, 4, 3, 2, 1, 48, 47, 46	DOUT[7:0]	Output	Pixel data output DOUT7 (most significant bit [MSB]), DOUT0 (least significant bit [LSB]). Data output [9:2] in sensor stand-alone mode
44	DOUT_LSB0	Output	Sensor stand-alone mode output 0—typically left unconnected for normal SOC operation.
45	DOUT_LSB1	Output	Sensor stand-alone mode output 1—typically left unconnected for normal SOC operation.
42	FRAME_VALID	Output	Active HIGH: FRAME_VALID (FV); indicates active frame.
41	LINE_VALID	Output	Active HIGH: LINE_VALID (LV); indicates active pixel.
43	PIXCLK	Output	Pixel clock output.
35	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single-ended mode.
33	DAC_NEG	Output	Negative video DAC output in differential mode. Tie to GND in single-ended mode
31	DAC_REF	Output	External reference resistor for video DAC.
39	LVDS_POS	Output	LVDS positive output.
38	LVDS_NEG	Output	LVDS negative output.
29	AGND	Supply	Analog ground.
15, 32, 37	DGND	Supply	Digital ground.
28	VAA	Supply	Analog power: 2.5–3.1V (2.8V nominal).
30	VAAPIX	Supply	Pixel array analog power supply: 2.5–3.1V (2.8V nominal).
16, 36	VDD	Supply	Digital power: 2.5–3.1V (2.8V nominal).
34	VDDDAC	Supply	DAC power: 2.5–3.1V (2.8V nominal).
40	VDDPLL	Supply	LVDS PLL power: 2.5–3.1V (2.8V nominal).

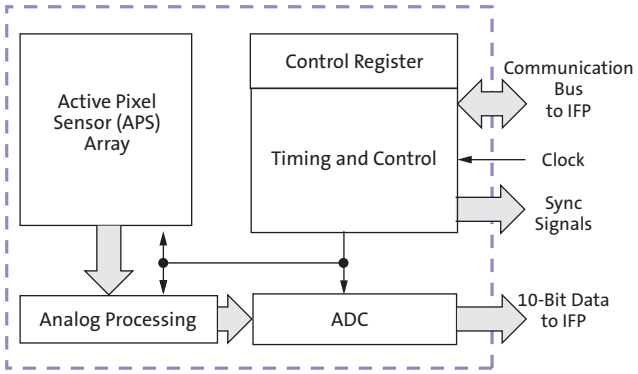
Notes:
1. ALL power pins (V_{DD}/V_{DD}DAC/V_{DD}PLL/V_{AA}/VAAPIX) must be connected to 2.8V (nominal). Power pins cannot be floated.
2. ALL ground pins (A_{GND}/D_{GND}) must be connected to ground. Ground pins cannot be floated.
3. Inputs are not tolerant to signal voltages above 3.1V.
4. All unused inputs must be tied to GND or V_{DD}.
5. V_{AA} and VAAPIX must be tied to the same potential for proper operation.

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array of 695 x 512, an analog readout chain, a 10-bit ADC with programmable gain and black offset, and timing and control as illustrated in Figure 5.

Figure 5: Sensor Core Block Diagram



Pixel Array Structure

The sensor core pixel array is configured as 695 columns by 512 rows, as shown in Figure 6. The first 42 columns and the first 13 rows of pixels are optically black, and can be used to monitor the black level. The last four columns and the last row of pixels are also optically black.

Figure 6: Pixel Array Description

The black row data is used internally for the automatic black level adjustment. However, these black rows can also be read out by setting the sensor to raw data output mode.

There are 649 columns by 498 rows of optically-active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

The one additional active column and two additional active rows are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 7 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right corner. The image is presented in true orientation by the output display.

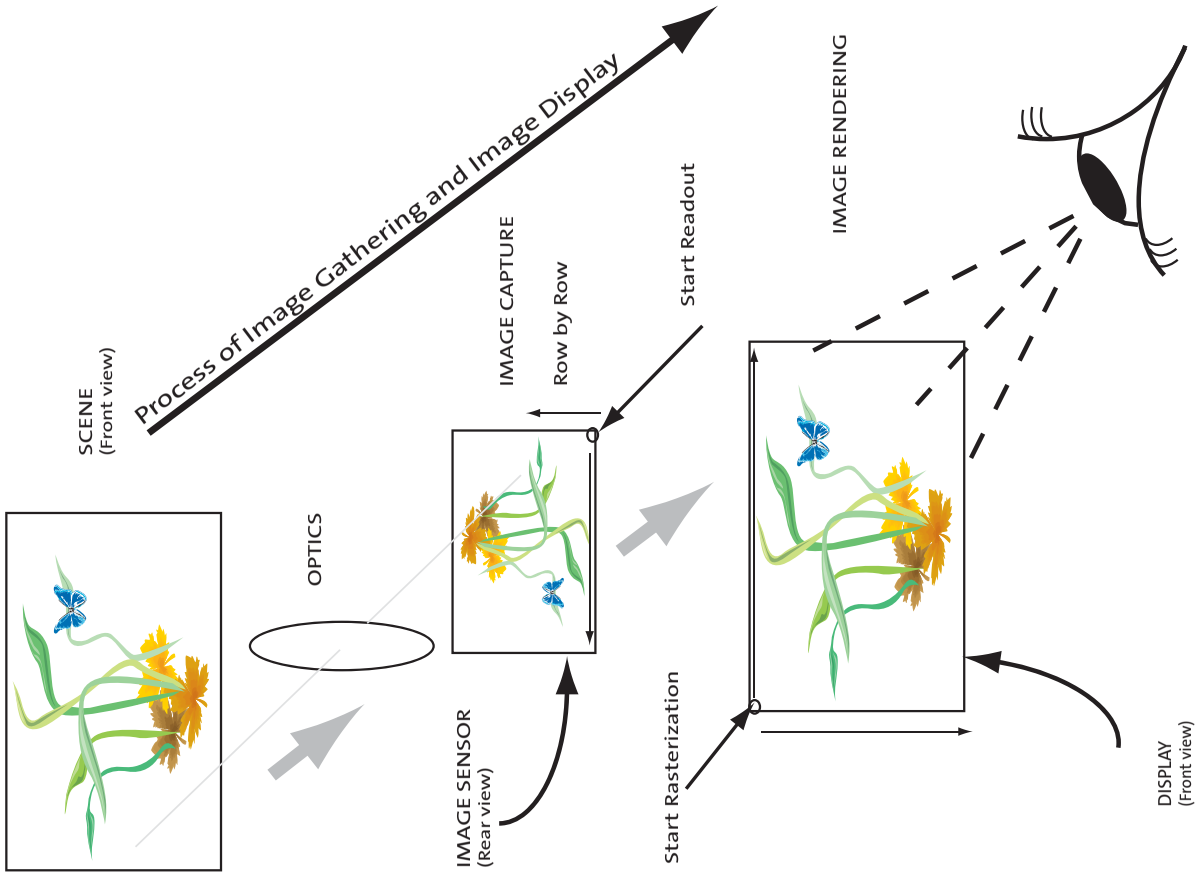


Figure 7: Image Capture Example

The sensor core uses a paired RGB Bayer color pattern, as shown in Figure 8. Row pairs consist of the following: rows 0, 1, rows 2, 3, rows 4, 5, and so on. The even-numbered row pairs (0/1, 4/5, and so on) in the active array contain green and red pixels. The odd-numbered row pairs (2/3, 6/7, and so on) contain blue and green pixels. The odd-numbered columns contain green and blue pixels; even-numbered columns contain red and green pixels.

Figure 8: Pixel Color Pattern Detail (top right corner)

Output Data Format

The sensor core image data is read out in an interlaced scan order. Progressive readout—which is not supported by the color pipe—is an option, but is only intended for raw data output. Valid image data is surrounded by horizontal and vertical blanking, shown in Figure 9 on page 18.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field; 240 image pixels with 24 dark pixels at the top of the image and 24 dark pixels at the bottom of the image field.

Figure 9: Spatial Illustration of Image Readout

$P_{0,0}$ $P_{0,1}$ $P_{0,2}$.....$P_{0,n-1}$ $P_{0,n}$ $P_{2,0}$ $P_{2,1}$ $P_{2,2}$.....$P_{2,n-1}$ $P_{2,n}$ Valid Image Odd Field $P_{m-2,0}$ $P_{m-2,1}$.....$P_{m-2,n-1}$ $P_{m-2,n}$ $P_{m,0}$ $P_{m,1}$.....$P_{m,n-1}$ $P_{m,n}$	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Horizontal Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00
00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Vertical Even Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Vertical/Horizontal Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00
$P_{1,0}$ $P_{1,1}$ $P_{1,2}$.....$P_{1,n-1}$ $P_{1,n}$ $P_{3,0}$ $P_{3,1}$ $P_{3,2}$.....$P_{3,n-1}$ $P_{3,n}$ Valid Image Even Field $P_{m-1,0}$ $P_{m-1,1}$.....$P_{m-1,n-1}$ $P_{m-1,n}$ $P_{m+1,0}$ $P_{m+1,1}$.....$P_{m+1,n-1}$ $P_{m+1,n}$	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Horizontal Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00
00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Vertical Odd Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 Vertical/Horizontal Blanking 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00

Image Flow Processor

The image flow processor (IFP) consists of a color processing pipeline as well as a measurement and control logic block (the camera controller)—see Figure 10 on page 20. The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens.

Next, the data is interpolated to recover missing color components for each pixel. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections, and is formatted for final output.

The measurement and control logic continuously accumulate image brightness and color statistics. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains that are sent to the sensor core through the control bus.

Black Level Conditioning

The sensor core black level calibration works to maintain black pixel values at a constant level, independent of analog gain, reference current, voltage settings, and temperature conditions. If this black level is above zero, it must be reduced before color processing can begin. The black level subtraction block in the IFP re-maps the black level of the sensor to zero prior to lens shading correction. Following lens shading correction, the black level addition block provides capability for another black level adjustment. However, for good contrast, this level should be set to zero.

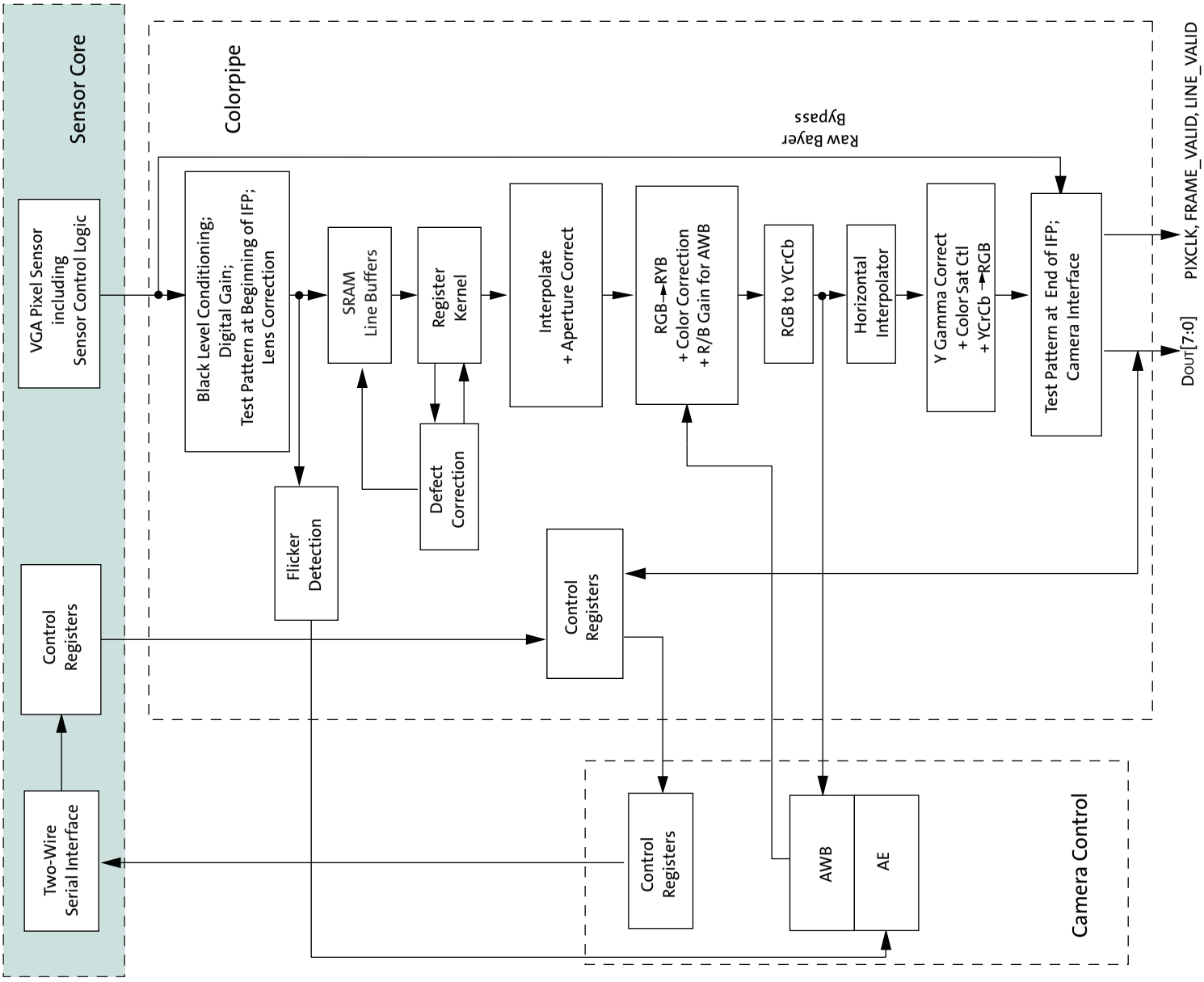
Digital Gain

Controlled by auto exposure logic, the input digital gain stage amplifies the raw image in low-light conditions (range: x1–x8).

Test Pattern

A built-in test pattern generator produces a test image stream that can be multiplexed with the gain stage. The test pattern can be selected through register settings (see R0x148). There is another set of test patterns at the end of the color pipe that can be selected through register R0x19B[5:4]. (See “Register Notation” on page 42.)

Figure 10: IFP Block Diagram



Notes: 1. NTSC encoder/DAC not shown

Lens Shading Correction (LC)

Inexpensive lenses tend to attenuate image intensity near the edges of pixel arrays. Other factors also cause signal and coloration differences across the image. The net result of all these factors is known as lens shading. Lens shading correction (LC) compensates for these differences.

Typically, the profile of lens shading-induced anomalies across the frame is different for each color component. Therefore, LC is independently calibrated for the color channels.

Interpolation and Aperture Correction

A demosaic engine converts the single-color-per-pixel Bayer data from the sensor into RGB (10-bit per color channel). The demosaic algorithm analyzes neighboring pixels to generate a best guess for the missing color components. Edge sharpness is preserved as much as possible.

Aperture correction sharpens the image by an adjustable amount. To avoid amplifying noise, sharpening can be programmed to phase out as light levels drop.

Defect Correction

This device supports 2D defect correction. In 2D defect detection and correction, pixels with values different from their neighbors by greater than a defined threshold are considered defects unless near the image boundary. The approach is termed 2D, as pixels on neighboring lines as well as neighboring pixels on the same line are considered in both detection and correction.

In Figure 10 on page 20, the register kernel gathers same color pixels and send the information to the 2D defect correction engine.

Color Correction

To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation, also known as color separation, is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. The optimal values for the color correction coefficients depend on the spectra of the incident illumination and can be programmed by the user.

Color Saturation Control

For noise reduction, both color saturation and sharpness enhancement can be set by the user or adjusted automatically by tracking the magnitude of the gains used by the auto exposure algorithm.

Automatic White Balance

The MT9V135 has a built-in automatic white balance (AWB) algorithm designed to compensate for the effects of changing scene illumination on the color rendition quality. This sophisticated algorithm consists of three major submodules:

- A measurement engine (ME) performing statistical analysis of the image

- A module selecting the optimal color correction matrix
- A module selecting the analog color channel gains in the sensor core

While the default algorithm settings are adequate in most situations, the user can reprogram base color correction matrices and limit color channel gains. The AWB does not attempt to locate the brightest or grayest elements in the image; it performs in-depth image analysis to differentiate between changes in predominant spectra of illumination and changes in predominant scene colors. Factory defaults are suitable for most applications; however, a wide range of algorithm parameters can be overwritten by the user through the serial interface.

Auto Exposure

The auto exposure algorithm performs automatic adjustments to image brightness by controlling exposure time and analog gains in the sensor core, as well as digital gain applied to the image. The algorithm relies on the auto exposure measurement engine that tracks speed and amplitude changes in the overall luminance of selected windows in the image.

Backlight compensation is achieved by weighting the luminance in the center of the image higher than the luminance on the periphery. Other algorithm features include: fast-fluctuating illumination rejection (time averaging), response-speed control, and controlled sensitivity to small changes.

While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters, as described above. The auto exposure algorithm enables compensation for a broad range of illumination intensities.

Automatic Flicker Detection

Flicker occurs when integration time is not an integer multiple of the period of the light intensity. The automatic flicker detection block does not compensate for the flicker; it reduces flicker occurrence by detecting flicker frequency and adjusting the integration time. For integration times shorter than the light intensity period (10ms for 50Hz environments and 8.33ms for 60Hz environments), flicker is unavoidable.

Gamma Correction

To achieve more life-like quality in an image, the IFP includes gamma correction and color saturation control. Gamma correction operates on the luminance component of the image and enables compensation for nonlinear dependence of the display device output versus the driving signal (for example, monitor brightness versus CRT voltage).

In addition, gamma correction provides range compression, converting 10-bit luminance input to 8-bit output. Pre-gamma image processing generates 10-bit luminance values ranging from 0 to 896. Piecewise linear gamma correction utilized in this imager has 10 linear intervals, with end points corresponding to the following input values:

$$Xi=0\ldots10 = \{0,16,32,64,128,256,384,512,640,768,896\}$$

For each input value *Xi*, the user can program the corresponding output value *Yi*. *Yi* values must be monotonically increasing.

NTSC and PAL Encoder Formats Supported

The MT9V135 has an on-chip video encoder to format the data stream for composite video output in the supported NTSC or PAL formats. The encoder expects CCIR-656 interlaced NTSC or PAL data stream input. By default, the input is taken from the on-chip image stream. Input can also be taken from the external 8-bit DIN[7:0] port for external image processing used with the on-chip video encoder and composite output.

Readout Modes

NTSC and PAL are two of the target output formats for the MT9V135. Table 4 identifies registers used to set NTSC or PAL modes.

Table 4: Readout Mode Register Settings – DOUT Not Qualified
When DOUT is not qualified with FV and LV

Readout Format/ Output Format/ Output Port1	NTSC or PAL2	Hold FV HIGH3	Output Select MUX4	Sensor Stand- Alone Mode5	Enable RGB6	RGB Output Format7	Output Odd Field Resolution	Output Even Field Resolution	Readout Format/ Output Frame Resolution
Interlaced/ CCIR656/ Dout[7:0] & LVDS	0: NTSC	0	0	0	0	0	720 x 244	720 x 243	720 x 487
Interlaced/ CCIR656/ Dout[7:0] & LVDS	1: PAL	0	0	0	0	0	720 x 288	720 x 288	720 x 576

Notes:
1. See "Register Notation" on page 42 for a description of the register notation.
2. R0x115[0]
3. R0x113[7]
4. R0x113[1:0]
5. R0x19B[12]
6. R0x19B[8]
7. R0x19B[7:6]

Table 5 identifies the readout format, output format, and output ports supported by the MT9V135. This table gives output formats supported by the MT9V135. The "DevWare Video Output Mode" column identifies the name used by the Aptina DevWare demonstration program to execute the readout mode. MT9V135 registers that enable these modes are specified in Table 4 on page 25.

Table 5: MT9V135 Readout Modes

Readout Format–Output Format	Parallel DOUT	Composite Analog Out	LVDS	DevWare Video Output Mode
Interlaced–CCIR656	Supported	Supported	Supported	Interlaced/CCIR656

Table 5: MT9V135 Readout Modes

Readout Format–Output Format	Parallel DOUT	Composite Analog Out	LVDS	DevWare Video Output Mode
Interlaced–RGB	Supported	Not supported	Not supported	Interlaced/RGB
Interlaced–Raw Bayer	Supported	Not supported	Not supported	Interlaced/Raw Bayer
Progressive–Raw Paired Bayer	Supported	Not supported	Not supported	Progressive/Raw Paired Bayer

Table 6: Readout Mode Register Settings – DOUT Qualified
When DOUT is qualified with FV and LV

Readout Format/ Output Format/ Output Port[1]	NTSC or PAL[2]	Hold FV High[3]	Output Select MUX[4]	Sensor Stand-alone Mode[5]	Enable RGB[6]	RGB Output Format[7]	Output Odd Field Resolution	Output Even Field Resolution	Output Frame Resolution
Interlaced/ CCIR656/ DOUT[7:0] & LVDS	0: NTSC	1	0	0	0	0	720 x 243	720 x 243	720 x 486
	1: PAL	1	0	0	0	0	720 x 288	720 x 288	720 x 576
Interlaced/ RGB/DOUT[7:0]	x[8]	x	2	0	0	0: RGB 565 1: RGB 555 2: RGB 444x 3: RGB x444	720 x 240	720 x 240	720 x 480
Interlaced/Raw Bayer/ DOUT[9:0]	x	x	2	1	0	0	648 x 248	648 x 248	648 x 596
Progressive/ Raw PAIRED Bayer/ DOUT[9:0]	x	x	2	1	0	0	n/a	n/a	648 x 488

Notes:
1. See "Register Notation" on page 42 for a description of the register notation.
2. R0x113[7]
3. R0x115[1:0]
4. R0x113[1:0]
5. R0x19B[12]
6. R0x19B[8]
7. R0x19B[7:6]
8. x = Don't Care

Readout Formats

Interlaced

The default output format, interlaced format, is required for NTSC or PAL output.

Progressive

Progressive format is used for raw Bayer output.

Output Formats

ITU-R BT.656 and RGB Output

The MT9V135 can output processed video as a standard ITU-R BT.656 (CCIR656) stream, an RGB stream, or as unprocessed Bayer data. The ITU-R BT.656 stream contains YCbCr 4:2:2 data with fixed embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression. RGB functionality provides support for LCD devices.

The MT9V135 can be configured to output 16-bit RGB (RGB565), 15-bit RGB (RGB555), and two types of 12-bit RGB (RGB444). Refer to Table 22 on page 109 and Table 23 on page 109 for details.

Bayer Output

Unprocessed paired Bayer data is generated when bypassing the IFP completely—that is, by simply outputting the sensor-paired Bayer stream as usual, using FV, LV, and PIXCLK to time the data. This mode is called sensor stand-alone mode.

Output Ports

Composite Video Output

The composite video output DAC is external resistor programmable and supports both single-ended and differential output. The DAC is driven by the on-chip video encoder output.

Serial Data Output

The processed image data stream can be output to the LVDS output port.

Parallel Output

Parallel output uses either 8-bit or 10-bit output. Eight-bit output is used for ITU-R BT.656 and RGB output. Ten-bit output is used for raw Bayer output.

Three Common Data Configurations

Figure 11, Figure 12 on page 29, and Figure 13 on page 30 demonstrate common configuration methods for the MT9V135. Figure 11 shows the most common usage mode.

The processed data from the sensor is output in analog composite video (NTSC or PAL) and CCIR 656 format through the analog and parallel data output ports, respectively.

Figure 11: MT9V135 in Analog Composite Video Mode

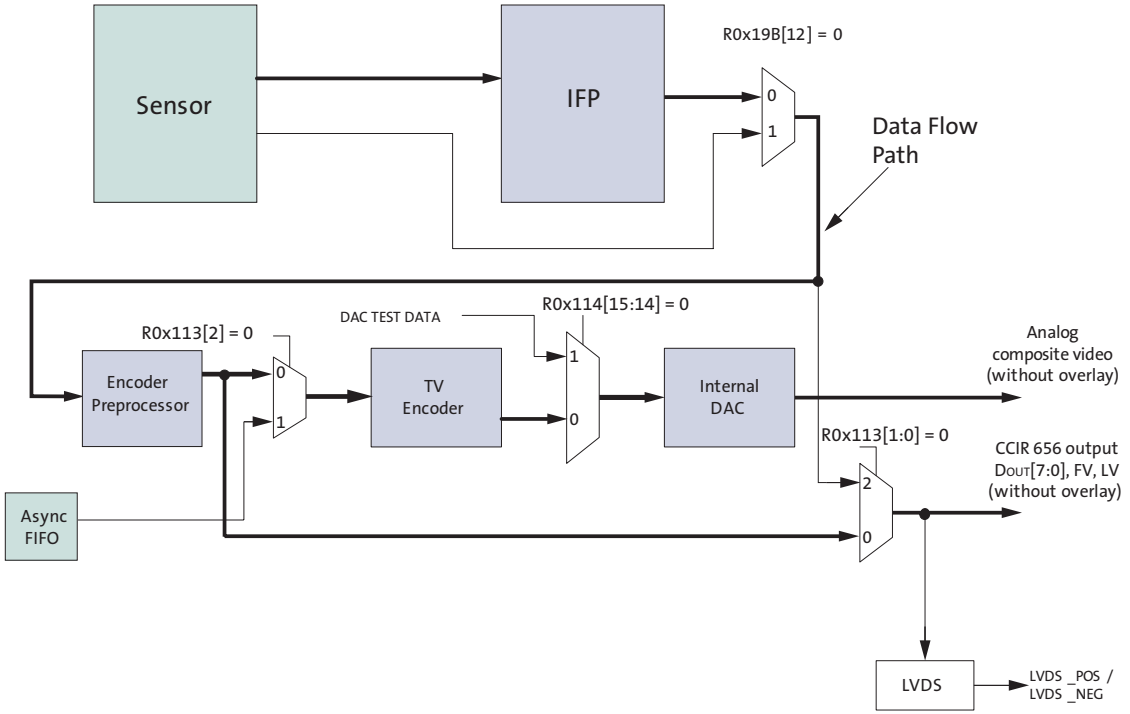


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Figure 12 shows the MT9V135 in sensor stand-alone mode. Raw Bayer data from the sensor bypasses the IFP to be output directly. Only parallel output is available for this mode.

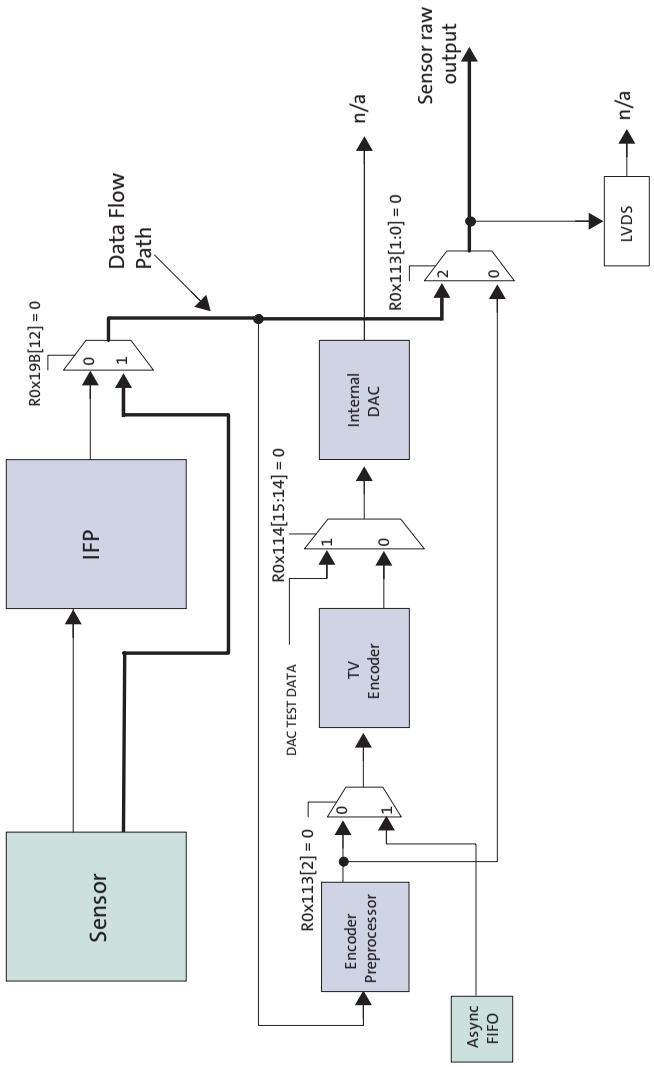


Figure 12: MT9V135 in Sensor Stand-Alone Mode

Figure 13 shows the MT9V135 in overlay output mode that allows the MT9V135 to be configured with an external DSP for text or image overlay.

Processed sensor data in CCIR 656 format is output as parallel data (DOUT[7-0]). This data is input to a user-supplied DSP that overlays text or graphics on the processed sensor image. DSP outputs CCIR 656 image with overlay which is input through the DIN port to be multiplexed at the encoder. This encoded data is output as analog composite video (NTSC or PAL).

Figure 13: MT9V135 in Overlay Output Mode

Sensor Core Modes and Timing

This section provides an overview of usage modes for the MT9V135 sensor core. An overview of typical usage modes for the complete MT9V135 is provided in "Modes and Timing" on page 98.

Readout Format

The sensor core supports two basic readout formats: interlaced and progressive. The interlaced format supports both NTSC and PAL timing. Progressive readout is intended for sensor stand-alone mode only (this is due to the paired Bayer pattern CFA).

Window Control

The window size and position need to be at the default settings for correct NTSC or PAL format support.

Window Start

The row and column start address of the displayed image can be set by R0x001 (row start) and R0x002 (column start).

Window Size

The default sensor resolution is 640 columns and 480 rows (VGA). For NTSC and PAL, this is expanded by the horizontal interpolator module to 720 columns. For proper NTSC or PAL operation, use only the default window size.

Pixel Border

When R0x020, bits[9:8] are both set, a 4-pixel border will be added around the specified image. When enabled, the row and column widths will be 8 pixels larger than the values programmed in the row and column registers. If the border is enabled but not shown in the image (R0x020[9:8] = 01), the horizontal blanking and vertical blanking values will be 8 pixels larger than the values programmed into the blanking registers. For proper NTSC or PAL operation, use only default values in the above mentioned registers.

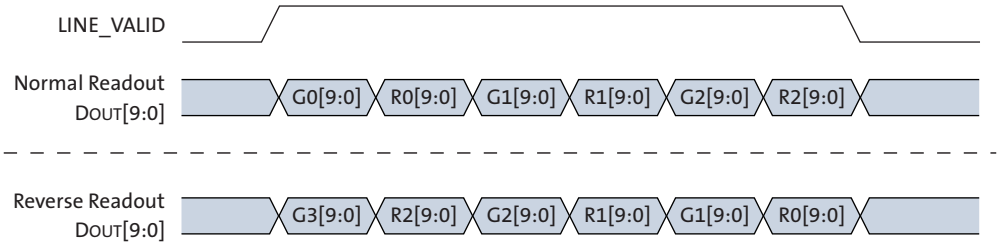
The border is read in an interlaced pattern when in interlaced readout mode. Each field has its own interlaced border on top and bottom of the active array.

Sensor Core Readout Modes

Column Mirror Image

At reset, the HORIZ_FLIP input pin is latched into R0x11E[1]. This bit is XORed with register Rox115[1]. The result determines if horizontal flip is enabled (result = 1) or disabled (result = 0). Figure 14 illustrates the readout order of the columns when they are reversed. The starting color is preserved when mirroring the columns.

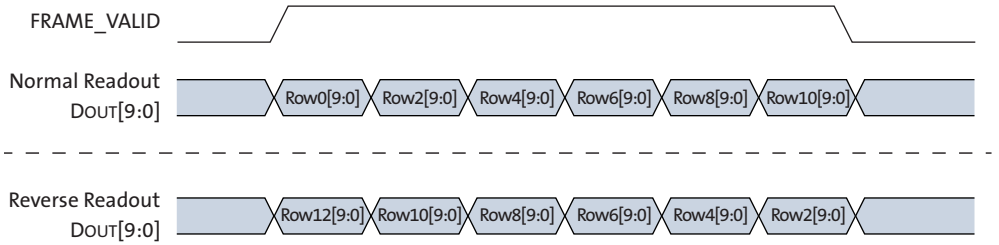
Figure 14: Six Pixels in Normal and Column Mirror Readout Modes



Row Mirror Image

By setting R0x020[0] = 1, the readout order of the rows will be reversed, as shown in Figure 15. The starting color is preserved when mirroring the rows.

Figure 15: Six Rows in Normal and Row Mirror Readout Modes



Frame Rate Control

Operating Mode

Actual frame rates can be tuned by adjusting various sensor parameters. The sensor registers are in address page 0, some of which are shown in Table 7 on page 33.

Typical settings and parameters for NTSC and PAL modes are shown in Table 8 on page 33.

For a given window size, the blanking registers (R0x005, R0x006, R0x011) can be used to set a particular frame rate.

Table 7: Register Address Functions

Register	Function
R0x004	Column width, typically 640 in the MT9V135
R0x003	Row width, typically 480 in the MT9V135
R0x005	Horizontal blanking, default is 210 (units of sensor pixel clocks)
R0x006, R0x011	Vertical blanking (odd/even), default is 14 (odd), 15 (even) (rows including black rows)

The sensor timing (Table 8 on page 33) is shown in terms of pixel clock and master clock cycles. The required master clock frequency is 27 MHz. The vertical blanking and total frame time equations assume that the number of integration rows (R0x009) is less than the number of active rows, plus blanking rows. If this is not the case, the number of integration rows must be used instead to determine the frame time.

In the MT9V135, the sensor core adds four border pixels all the way around the image, taking the active image size to 648 x 488. This is achieved through the default of oversize and show border bits set.

NTSC mode has 525 rows per frame; PAL mode has 625 rows per frame as enumerated below (all values in rows):

$$OddFieldActive + OddFieldVerticalBlanking + EvenFieldActive + EvenFieldVerticalBlanking = RowsPerFrame \quad \text{(EQ 1)}$$

NTSC:

$$4 + 240 + 4) + 14 + (4 + 240 + 4) + 15 = 525 \quad \text{(EQ 2)}$$

PAL:

$$4 + 240 + 4) + 64 + (4 + 240 + 4) + 65 = 625 \quad \text{(EQ 3)}$$

Blanking Calculations

When calculating blanking, minimum values for horizontal blanking and vertical blanking must be taken into account. Table 8 shows minimum values for each register. This is valid for non NTSC or PAL modes only.

Table 8: Blanking Minimum Values (in Sensor Stand-alone Mode)

Parameter	Minimum
Horizontal blanking	132 (sensor pixel clocks)
Vertical blanking	6 + # of dark rows

Minimum Horizontal Blanking (in Sensor Stand-alone Mode)

The minimum horizontal blanking value is constrained by the time used for sampling a row of pixels and the overhead in the row readout. This can be expressed in an equation as:

$$HBLANK(min) = (startup\ overhead + sampling\ time + extra\ cb\ time + dark\ col\ time) \quad \text{(EQ 4)}$$

$$= (31 + done\_sample/2 + 16 + (22 \times read\_dark\_cols)) \quad \text{(EQ 5)}$$

$$= (47 + done\_sample/2 + (22 \times read\_dark\_cols)) \quad \text{(EQ 6)}$$

where:

$$done\_sample = R0x07E\ (rounded\ up\ to\ nearest\ even\ number) \quad \text{(EQ 7)}$$

$$read\_dark\_cols = R0x22:0,\ (bit[8]) \quad \text{(EQ 8)}$$

with default settings:

$$HBLANK(MIN) = (47 + 152/2 + 22) = 145\ PIXCLK\ periods \quad \text{(EQ 9)}$$

To get an aggressive minimum value for the horizontal blanking, the larger of R0x079[15:8] and R0x076[15:8] can be substituted for the R0x07E value in the above equation. With default settings, this gives a minimum HBLANK time of 127.

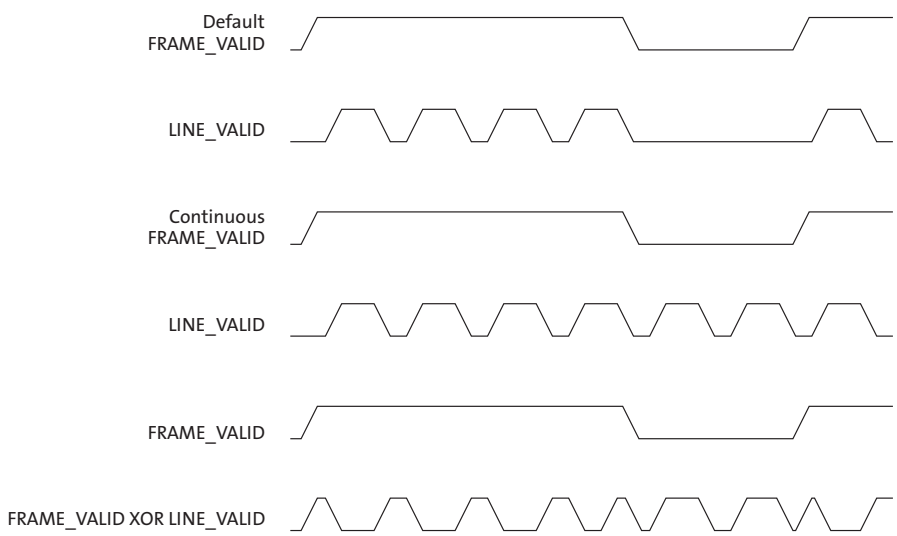
Valid Data Signals Options

LINE_VALID Signal

By setting bits[15:14] of R0x020, the LV signal is programmed for three different output formats. The formats shown below illustrate reading out four rows and two vertical blanking rows (Figure 16 on page 35).

The default line valid format is shown first; continuous LV is shown second. In the last format, the LV signal is exclusive ORed (XOR) between the continuous LV signal and the FV signal.

Figure 16: LINE_VALID Formats



Integration Time

Integration time is controlled by R0x009 (shutter width, in multiples of the row time) and R0x00C (shutter delay, in PIXCLK_PERIOD/2). R0x00C is used to control sub-row integration times and will only have a visible effect for small values of R0x009. The total integration time, ^{t}INT, is shown in the equations below (PIXCLK_PERIOD is in terms of master clock periods):

$$^{t}INT = R0x009 \times Row\ Time - Integration\ Overhead - Shutter\ Delay \quad \text{(EQ 10)}$$

where:

$$Row\ Time = (R0x004 + HBLANK\_REG + 8(when\ border\ is\ set)) \times PIXCLK\_PERIOD \quad \text{(EQ 11)}$$

$$Integration\ Overhead = 182\ master\ clock\ periods \quad \text{(EQ 12)}$$

$$Shutter\ Delay = R0x00C/2 \times PIXCLK\_PERIOD \quad \text{(EQ 13)}$$

with default settings for NTSC:

$$^{t}INT = (470 \times 858 \times 2) - 182 - 0 = 806{,}388\ master\ clock\ periods \quad \text{(EQ 14)}$$

with default settings for PAL:

$$^{t}INT = (470 \times 864 \times 2) - 182 - 0 = 811{,}978 \text{ master clock periods} \quad \text{(EQ 15)}$$

In this equation, the integration overhead corresponds to the delay between the row reset sequence and the row sample (read) sequence.

The integration overhead shown is valid only for the default PIXCLK_PERIOD and default sample (R0x07E) and reset (R0x087) values.

Typically, the value of the shutter width register (R0x009) is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time.

If R0x009 is increased beyond the total number of rows per frame (525 for NTSC, 625 for PAL), the sensor will add additional blanking rows as needed and violate the frame time requirement of NTSC and PAL. However, the effective value of R0x009 is always limited by the settings in R0x013 and R0x014.

A second constraint is that ^{t}INT must be adjusted to avoid banding in the image caused by light flicker. This means that ^{t}INT must be a multiple of 1/120 of a second under 60Hz flicker, and a multiple of 1/100 of a second under 50Hz flicker.

Maximum Shutter Delay

The shutter delay can be used to reduce the integration time. A programmed value of *N* reduces the integration time by *N* master clock periods. The maximum shutter delay is set by the row time and the sample time, as shown in the equations below:

$$\text{max shutter delay} = \text{Row Time} - \text{Shutter Overhead} \quad \text{(EQ 16)}$$

where:

$$\text{Row Time} = (\text{R0x004} + \text{HBLANK\_REG}) \times \text{PIXCLK\_PERIOD} \quad \text{(EQ 17)}$$

$$\text{Shutter Overhead (NTSC)} = 356 \text{ master clock periods} \quad \text{(EQ 18)}$$

$$\text{Shutter Overhead (PAL)} = 368 \text{ master clock periods} \quad \text{(EQ 19)}$$

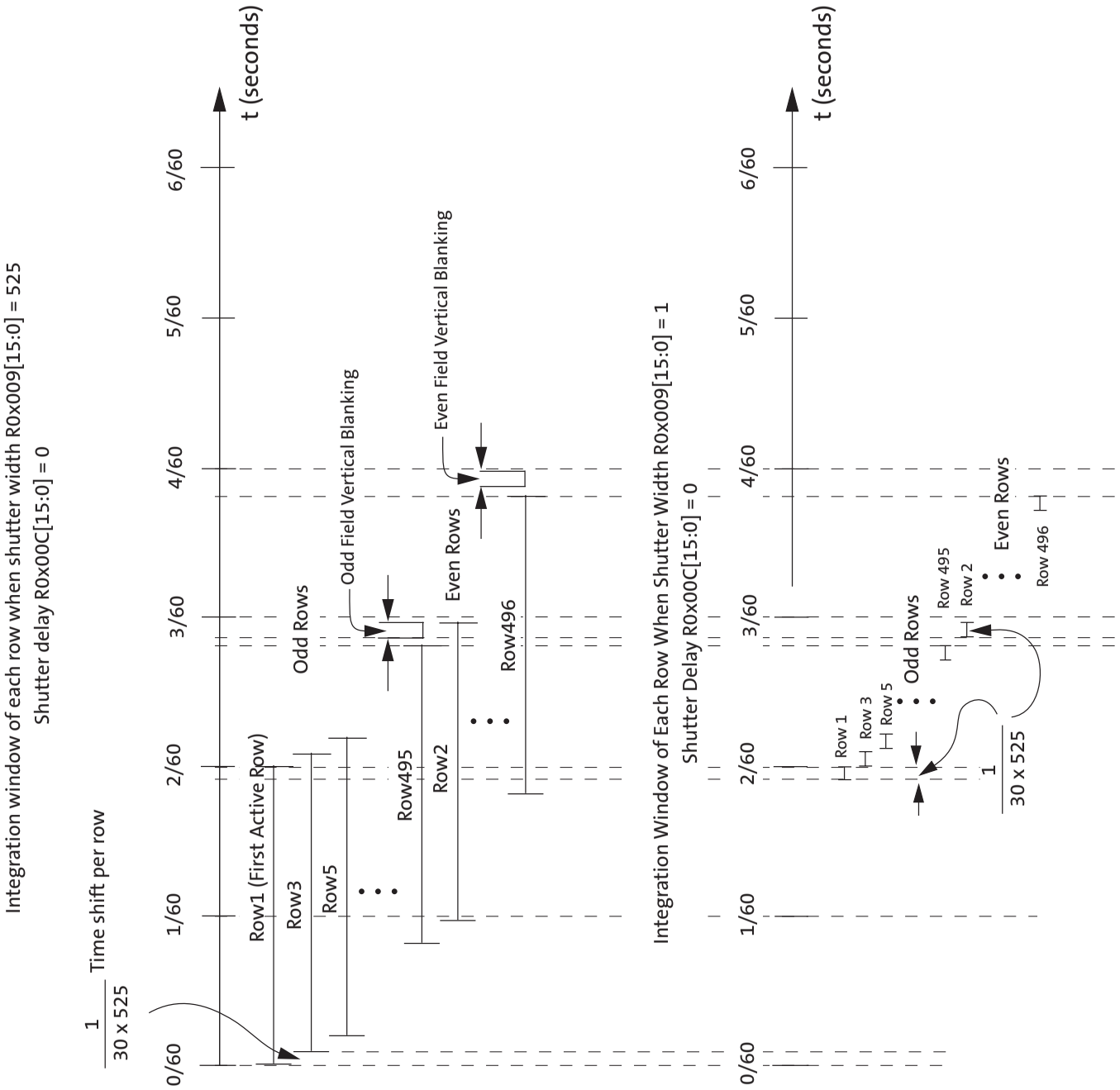
with default settings:

$$\text{NTSC max shutter delay} = (858 \times 2) - 356 = 1360 \text{ master clock periods} \quad \text{(EQ 20)}$$

$$\text{PAL max shutter delay} = (864 \times 2) - 368 = 1360 \text{ master clock periods} \quad \text{(EQ 21)}$$

If the value in this register exceeds the maximum value given by this equation, the sensor may not generate an image. Again, the overhead time shown in this equation is only valid for the default PIXCLK_PERIOD, and the default sample (R0x7E:0) and reset (R0x87:0) valuesFigure 17 on page 38, illustrates the integration time for each sensor row versus the shutter width. Odd rows are integrated first followed by even rows.

Figure 17: Integration Window of Each Sensor Row for NTSC Mode (Interlace Readout)



Note: Drawings are not to scale.

Register Overview

The sensor core, color pipe, and camera control registers are grouped in three separate address spaces, shown in Figure 18.

The register notation is defined in the section below. When accessing the MT9V135 through the two-wire serial interface, the address space (that is the page) must be set prior to accessing the desired register. The page register is sticky once set; it does not change unless overwritten.

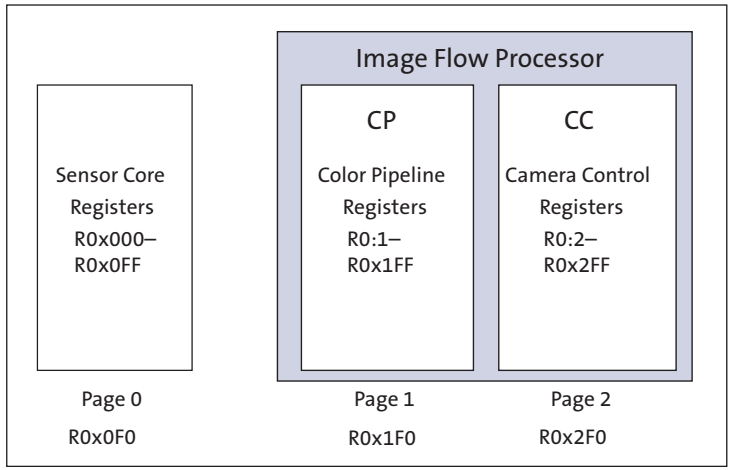
The address page is located at one of the three address spaces (R0x0F0, R0x1F0, and R0x2F0).

Register Notation

The following register address notations are used:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register (register 9) in the sensor page (page 0). Used to uniquely specify a register.
- R0x<3 digit hex address>
  Example: R0x105— Page 1, Aperture Correction register (05). Same as 0x<2 digit hex address> notation; leading digit signifies page number.
- Data Format (Binary) Column Key in the Register Summary tables:
  - 0 = “Don't Care” bit
  - d = RW (read or write) bit
  - ? = RO (read only) bit

Figure 18: Internal Registers Grouping



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Register Default Values

The register definition tables contain the power-on default values for the bit fields and registers of the MT9V135. Modifying these values may affect the performance of the MT9V135 in a positive or negative way. See the individual register descriptions for more detail.

The sensor registers are summarized in Table 9 on page 44. The color pipe registers are summarized in Table 11 on page 51. The camera control registers are summarized in Table 12 on page 56.

Sensor Registers—Short Descriptions

Register addresses that do not appear in the summary tables are not used by the MT9V135.

Table 9: Sensor Core Registers—Address Page 0

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R0:0(R0x000)	Chip Version	dddd dddd dddd dddd	4766 (0x129E)
R1:0(R0x001)	Row Start	0000 0ddd dddd dddd	21 (0x0015)
R2:0(R0x002)	Column Start	0000 0ddd dddd dddd	46 (0x002E)
R3:0(R0x003)	Reserved	–	480 (0x01E0)
R4:0(R0x004)	Reserved	–	640 (0x0280)
R5:0(R0x005)	Horizontal Blanking	00dd dddd dddd dddd	210 (0x00D2)
R6:0(R0x006)	Odd Field Vertical Blanking	0ddd dddd dddd dddd	14 (0x000E)
R7:0(R0x007)	Field Height	0000 0000 dddd dddd	240 (0x00F0)
R9:0(R0x009)	Shutter Width	dddd dddd dddd dddd	262 (0x0106)
R10:0(R0x00A)	Sensor Clock Control	dddd dddd dddd dddd	17 (0x0011)
R11:0(R0x00B)	Extra Delay	00dd dddd dddd dddd	0 (0x0000)
R12:0(R0x00C)	Shutter Delay	00dd dddd dddd dddd	0 (0x0000)
R13:0(R0x00D)	Reset and Standby Control	dddd dddd dddd dddd	264 (0x0108)
R16:0(R0x010)	Reserved	–	0 (0x0000)
R17:0(R0x011)	Even Field Vertical Blanking	0000 0000 0ddd dddd	15 (0x000F)
R18:0(R0x012)	Reserved	–	1260 (0x04EC)
R19:0(R0x013)	Reserved	–	525 (0x020D)
R20:0(R0x014)	Reserved	–	625 (0x0271)
R32:0(R0x020)	Read Mode	dd00 00dd dd00 dd0d	768 (0x0300)
R34:0(R0x022)	Dark Column and Row Control	0ddd dddd dddd dddd	269 (0x010D)
R36:0(R0x024)	Extra Reset	dddd dddd dddd dddd	16384 (0x4000)
R43:0(R0x02B)	Green1 Gain	0000 dddd dddd dddd	40 (0x0028)
R44:0(R0x02C)	Blue Gain	0000 dddd dddd dddd	100 (0x0064)
R45:0(R0x02D)	Red Gain	0000 dddd dddd dddd	30 (0x001E)
R46:0(R0x02E)	Green2 Gain	0000 dddd dddd dddd	40 (0x0028)
R47:0(R0x02F)	Global Gain	d000 dddd dddd dddd	40 (0x0028)
R48:0(R0x030)	Row Noise	dddd dddd dddd dddd	2090 (0x082A)
R49:0(R0x031)	Reserved	–	7168 (0x1C00)
R50:0(R0x032)	Reserved	–	42 (0x002A)
R51:0(R0x033)	Reserved	–	835 (0x0343)
R52:0(R0x034)	Reserved	–	49165 (0xC00D)
R53:0(R0x035)	Reserved	–	8226 (0x2022)

Table 9: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R54:0(R0x036)	Reserved	–	61680 (0xF0F0)
R55:0(R0x037)	Reserved	–	0 (0x0000)
R56:0(R0x038)	Reserved	–	8194 (0x2002)
R59:0(R0x03B)	Reserved	–	22 (0x0016)
R60:0(R0x03C)	Reserved	–	6688 (0x1A20)
R61:0(R0x03D)	Reserved	–	8222 (0x201E)
R62:0(R0x03E)	Reserved	–	8224 (0x2020)
R63:0(R0x03F)	Reserved	–	4128 (0x1020)
R64:0(R0x040)	Reserved	–	8204 (0x200C)
R65:0(R0x041)	Reserved	–	215 (0x00D7)
R66:0(R0x042)	Reserved	–	1943 (0x0797)
R67:0(R0x043)	Reserved	–	1040 (0x0410)
R88:0(R0x058)	Reserved	–	0 (0x0000)
R89:0(R0x059)	Reserved	–	30 (0x001E)
R90:0(R0x05A)	Reserved	–	57354 (0xE00A)
R91:0(R0x05B)	Dark Green1 Frame Average	0000 0000 0??? ????	32 (0x0020)
R92:0(R0x05C)	Dark Blue Frame Average	0000 0000 0??? ????	34 (0x0022)
R93:0(R0x05D)	Dark Red Frame Average	0000 0000 0??? ????	31 (0x001F)
R94:0(R0x05E)	Dark Green2 Frame Average	0000 0000 0??? ????	32 (0x0020)
R95:0(R0x05F)	Black Level Calibration Threshold	dddd dddd dddd dddd	8989 (0x231D)
R96:0(R0x060)	Black Level Calibration Control	000d 000d dddd dddd	128 (0x0080)
R97:0(R0x061)	Green1 Offset Calibration Value	0000 000d dddd dddd	36 (0x0024)
R98:0(R0x062)	Blue Offset Calibration Value	0000 000d dddd dddd	38 (0x0026)
R99:0(R0x063)	Red Offset Calibration Value	0000 000d dddd dddd	36 (0x0024)
R100:0(R0x064)	Green2 Offset Calibration Value	0000 000d dddd dddd	37 (0x0025)
R112:0(R0x070)	Reserved	–	40023 (0x9C57)
R113:0(R0x071)	Reserved	–	40023 (0x9C57)
R114:0(R0x072)	Reserved	–	24921 (0x6159)
R115:0(R0x073)	Reserved	–	39257 (0x9959)
R116:0(R0x074)	Reserved	–	32631 (0x7F77)
R117:0(R0x075)	Reserved	–	32376 (0x7E78)
R118:0(R0x076)	Reserved	–	39033 (0x9879)
R119:0(R0x077)	Reserved	–	30045 (0x755D)
R120:0(R0x078)	Reserved	–	39763 (0x9B53)
R121:0(R0x079)	Reserved	–	39253 (0x9955)

Table 9: Sensor Core Registers—Address Page 0 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R122:0(R0x07A)	Reserved	–	39511 (0x9A57)
R123:0(R0x07B)	Reserved	–	39766 (0x9B56)
R124:0(R0x07C)	Reserved	–	40277 (0x9D55)
R125:0(R0x07D)	Reserved	–	30044 (0x755C)
R126:0(R0x07E)	Reserved	–	157 (0x009D)
R127:0(R0x07F)	Reserved	–	40018 (0x9C52)
R128:0(R0x080)	Reserved	–	22532 (0x5804)
R129:0(R0x081)	Reserved	–	22532 (0x5804)
R130:0(R0x082)	Reserved	–	21520 (0x5410)
R131:0(R0x083)	Reserved	–	21777 (0x5511)
R132:0(R0x084)	Reserved	–	13842 (0x3612)
R133:0(R0x085)	Reserved	–	14100 (0x3714)
R134:0(R0x086)	Reserved	–	23042 (0x5A02)
R135:0(R0x087)	Reserved	–	92 (0x005C)
R200:0(R0x0C8)	Reserved	–	0 (0x0000)
R240:0(R0x0F0)	Page Map	0000 0000 0000 0ddd	0 (0x0000)
R241:0(R0x0F1)	Bytewise Addr	dddd dddd dddd dddd	0 (0x0000)
R245:0(R0x0F5)	Reserved	–	1023 (0x03FF)
R246:0(R0x0F6)	Reserved	–	1023 (0x03FF)
R247:0(R0x0F7)	Reserved	–	0 (0x0000)
R248:0(R0x0F8)	Reserved	–	0 (0x0000)
R249:0(R0x0F9)	Reserved	–	11264 (0x2C00)
R250:0(R0x0FA)	Reserved	–	0 (0x0000)
R251:0(R0x0FB)	Reserved	–	0 (0x0000)
R252:0(R0x0FC)	Reserved	–	0 (0x0000)
R253:0(R0x0FD)	Reserved	–	0 (0x0000)
R255:0(R0x0FF)	Chip Version	???? ???? ???? ????	4766 (0x129E)

Table 10: Color Pipe Registers—Address Space 1

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

RegisterNumber Dec(Hex)	Register Description	Data Forma (Binary)	Default Value Dec(Hex)
R5:1(R0x105)	Aperture Correction	0000 0000 0000 dddd	11 (0x000B)
R6:1(R0x106)	Operating Mode Control	dddd dddd dddd dddd	25614 (0x640E)
R8:1(R0x108)	Output Format Control	dddd dddd dddd dddd	128 (0x0080)

Table 10: Color Pipe Registers—Address Space 1 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

RegisterNumber Dec(Hex)	Register Description	Data Forma (Binary)	Default Value Dec(Hex)
R16:1(R0x110)	Reserved	–	0 (0x0000)
R17:1(R0x111)	Reserved	–	3 (0x0003)
R18:1(R0x112)	Reserved	–	0 (0x0000)
R19:1(R0x113)	Chip level control	0000 0ddd dd0d dddd	1920 (0x0780)
R20:1(R0x114)	Reserved	–	0 (0x0000)
R21:1(R0x115)	Invert Latched Pins	0000 0000 dddd dddd	0 (0x0000)
R22:1(R0x116)	Reserved	–	0 (0x0000)
R23:1(R0x117)	Reserved	–	0 (0x0000)
R24:1(R0x118)	Reserved	–	0 (0x0000)
R25:1(R0x119)	Reserved	–	0 (0x0000)
R26:1(R0x11A)	Reserved	–	0 (0x0000)
R27:1(R0x11B)	Reserved	–	0 (0x0000)
R28:1(R0x11C)	Reserved	–	0 (0x0000)
R29:1(R0x11D)	LVDS Control Register	00dd dddd dddd dddd	8192 (0x2000)
R30:1(R0x11E)	Latched Pin Status	0000 0000 ???? ????	4 (0x0004)
R37:1(R0x125)	Color Saturation Control	0000 0000 00dd dddd	5 (0x0005)
R52:1(R0x134)	Luma Offset [Can be used to Control Brightness]	dddd dddd dddd dddd	16 (0x0010)
R53:1(R0x135)	Luma Clip	dddd dddd dddd dddd	61456 (0xF010)
R58:1(R0x13A)	Reserved	–	512 (0x0200)
R59:1(R0x13B)	Black Subtraction	0000 0ddd dddd dddd	1046 (0x0416)
R60:1(R0x13C)	Black Addition	0000 0ddd dddd dddd	1024 (0x0400)
R71:1(R0x147)	Reserved	–	24 (0x0018)
R72:1(R0x148)	Test Pattern Generator Control	0000 0000 dddd dddd	0 (0x0000)
R83:1(R0x153)	Reserved	–	7700 (0x1E14)
R84:1(R0x154)	Reserved	–	17966 (0x462E)
R85:1(R0x155)	Reserved	–	34666 (0x876A)
R86:1(R0x156)	Reserved	–	47008 (0xB7A0)
R87:1(R0x157)	Reserved	–	57548 (0xE0CC)
R88:1(R0x158)	Reserved	–	0 (0x0000)
R104:1(R0x168)	Reserved	–	17 (0x0011)
R128:1(R0x180)	Lens Correction Control	0000 0000 0ddd dddd	3 (0x0003)
R129:1(R0x181)	Lens Vertical Red Knee 0 and Initial Value	dddd dddd dddd dddd	60677 (0xED05)
R130:1(R0x182)	Lens Vertical Red Knees 2 and 1	dddd dddd dddd dddd	3804 (0x0EDC)
R131:1(R0x183)	Lens Vertical Red Knees 4 and 3	dddd dddd dddd dddd	61193 (0xEF09)
R132:1(R0x184)	Lens Vertical Green Knee 0 and Initial Value	dddd dddd dddd dddd	60677 (0xED05)

Table 10: Color Pipe Registers—Address Space 1 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

RegisterNumber Dec(Hex)	Register Description	Data Forma (Binary)	Default Value Dec(Hex)
R133:1(R0x185)	Lens Vertical Green Knees 2 and 1	dddd dddd dddd dddd	3804 (0x0EDC)
R134:1(R0x186)	Lens Vertical Green Knees 4 and 3	dddd dddd dddd dddd	61193 (0xEF09)
R135:1(R0x187)	Lens Vertical Blue Knee 0 and Initial Value	dddd dddd dddd dddd	60677 (0xED05)
R136:1(R0x188)	Lens Vertical Blue Knees 2 and 1	dddd dddd dddd dddd	3804 (0x0EDC)
R137:1(R0x189)	Lens Vertical Blue Knees 4and 3	dddd dddd dddd dddd	61193 (0xEF09)
R138:1(R0x18A)	Lens Horizontal Red Knee 0 and Initial Value	dddd dddd dddd dddd	59401 (0xE809)
R139:1(R0x18B)	Lens Horizontal Red Knees 2 and 1	dddd dddd dddd dddd	63732 (0xF8F4)
R140:1(R0x18C)	Lens Horizontal Red Knees 4 and 3	dddd dddd dddd dddd	61428 (0xEFF4)
R141:1(R0x18D)	Lens Horizontal Red Knee 5	0000 0000 dddd dddd	2 (0x0002)
R142:1(R0x18E)	Lens Horizontal Green Knee 0 and Initial Value	dddd dddd dddd dddd	59401 (0xE809)
R143:1(R0x18F)	Lens Horizontal Green Knees 2 and 1	dddd dddd dddd dddd	63732 (0xF8F4)
R144:1(R0x190)	Lens Horizontal Green Knees 4 and 3	dddd dddd dddd dddd	61428 (0xEFF4)
R145:1(R0x191)	Lens Horizontal Green Knee 5	0000 0000 dddd dddd	2 (0x0002)
R146:1(R0x192)	Lens Horizontal Blue Knee 0 and Initial Value	dddd dddd dddd dddd	59401 (0xE809)
R147:1(R0x193)	Lens Horizontal Blue Knees 2 and 1	dddd dddd dddd dddd	63732 (0xF8F4)
R148:1(R0x194)	Lens Horizontal Blue Knees 4 and 3	dddd dddd dddd dddd	61428 (0xEFF4)
R149:1(R0x195)	Lens Horizontal Blue Knee 5	0000 0000 dddd dddd	2 (0x0002)
R153:1(R0x199)	Line Counter	000? ???? ???? ????	80 (0x0050)
R154:1(R0x19A)	Frame Counter	???? ???? ???? ????	423 (0x01A7)
R155:1(R0x19B)	Output Format Control 2	0ddd dddd dddd dddd	512 (0x0200)
R157:1(R0x19D)	Defect Correction Control	dddd dddd dddd dddd	9390 (0x24AE)
R159:1(R0x19F)	Reserved	–	0 (0x0000)
R160:1(R0x1A0)	Reserved	–	640 (0x0280)
R161:1(R0x1A1)	Reserved	–	640 (0x0280)
R162:1(R0x1A2)	Reserved	–	0 (0x0000)
R163:1(R0x1A3)	Reserved	–	240 (0x00F0)
R164:1(R0x1A4)	Reserved	–	240 (0x00F0)
R165:1(R0x1A5)	Reserved	–	0 (0x0000)
R166:1(R0x1A6)	Reserved	–	640 (0x0280)
R167:1(R0x1A7)	Reducer Horizontal Output Size Resize	0000 0ddd dddd dddd	640 (0x0280)
R168:1(R0x1A8)	Reserved	–	0 (0x0000)
R169:1(R0x1A9)	Reserved	–	240 (0x00F0)
R170:1(R0x1AA)	Reducer Vertical Output Size Resize	0000 0ddd dddd dddd	240 (0x00F0)
R171:1(R0x1AB)	Reserved	–	640 (0x0280)
R172:1(R0x1AC)	Reserved	–	240 (0x00F0)

Table 10: Color Pipe Registers—Address Space 1 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

RegisterNumber Dec(Hex)	Register Description	Data Forma (Binary)	Default Value Dec(Hex)
R174:1(R0x1AE)	Reserved	–	3081 (0x0C09)
R175:1(R0x1AF)	Reducer Zoom Control	0000 dddd dddd dddd	2048 (0x0800)
R180:1(R0x1B4)	Reserved	–	32 (0x0020)
R182:1(R0x1B6)	Lens Vertical Red Knees 6 and 5	dddd dddd dddd dddd	0 (0x0000)
R183:1(R0x1B7)	Lens Vertical Red Knees 8 and 7	dddd dddd dddd dddd	0 (0x0000)
R184:1(R0x1B8)	Lens Vertical Green Knees 6 and 5	dddd dddd dddd dddd	0 (0x0000)
R185:1(R0x1B9)	Lens Vertical Green Knees 8 and 7	dddd dddd dddd dddd	0 (0x0000)
R186:1(R0x1BA)	Lens Vertical Blue Knees 6 and 5	dddd dddd dddd dddd	0 (0x0000)
R187:1(R0x1BB)	Lens Vertical Blue Knees 8 and 7	dddd dddd dddd dddd	0 (0x0000)
R188:1(R0x1BC)	Lens Horizontal Red Knees 7 and 6	dddd dddd dddd dddd	528 (0x0210)
R189:1(R0x1BD)	Lens Horizontal Red Knees 9 and 8	dddd dddd dddd dddd	526 (0x020E)
R190:1(R0x1BE)	Lens Horizontal Red Knee 10	0000 0000 dddd dddd	23 (0x0017)
R191:1(R0x1BF)	Lens Horizontal Green Knees 7 and 6	dddd dddd dddd dddd	528 (0x0210)
R192:1(R0x1C0)	Lens Horizontal Green Knees 9 and 8	dddd dddd dddd dddd	526 (0x020E)
R193:1(R0x1C1)	Lens Horizontal Green Knee 10	0000 0000 dddd dddd	23 (0x0017)
R194:1(R0x1C2)	Lens Horizontal Blue Knees 7 and 6	dddd dddd dddd dddd	528 (0x0210)
R195:1(R0x1C3)	Lens Horizontal Blue Knees 9 and 8	dddd dddd dddd dddd	526 (0x020E)
R196:1(R0x1C4)	Lens Horizontal Blue Knee 10	0000 0000 dddd dddd	23 (0x0017)
R200:1(R0x1C8)	Reserved	–	7947 (0x1F0B)
R201:1(R0x1C9)	Reserved	–	0 (0x0000)
R202:1(R0x1CA)	Reserved	–	0 (0x0000)
R203:1(R0x1CB)	Reserved	–	0 (0x0000)
R204:1(R0x1CC)	Reserved	–	0 (0x0000)
R205:1(R0x1CD)	Reserved	–	0 (0x0000)
R206:1(R0x1CE)	Reserved	–	0 (0x0000)
R207:1(R0x1CF)	Reserved	–	0 (0x0000)
R208:1(R0x1D0)	Reserved	–	0 (0x0000)
R220:1(R0x1DC)	Gamma Knee Y2 and Y1	dddd dddd dddd dddd	4101 (0x1005)
R221:1(R0x1DD)	Gamma Knee Y3 and Y4	dddd dddd dddd dddd	22575 (0x582F)
R222:1(R0x1DE)	Gamma Knee Y5 and Y6	dddd dddd dddd dddd	39808 (0x9B80)
R223:1(R0x1DF)	Gamma Knee Y7 and Y8	dddd dddd dddd dddd	49840 (0xC2B0)
R224:1(R0x1E0)	Gamma Knee Y9 and Y10	dddd dddd dddd dddd	57554 (0xE0D2)
R225:1(R0x1E1)	Gamma Knee Y0	0000 0000 dddd dddd	0 (0x0000)
R226:1(R0x1E2)	Reserved	–	28672 (0x7000)
R227:1(R0x1E3)	Reserved	–	45091 (0xB023)

Table 10: Color Pipe Registers—Address Space 1 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

RegisterNumber Dec(Hex)	Register Description	Data Forma (Binary)	Default Value Dec(Hex)
R240:1(R0x1F0)	Page Map	0000 0000 0000 0ddd	1 (0x0001)
R241:1(R0x1F1)	Bytewise Addr	dddd dddd dddd dddd	0 (0x0000)

Table 11: Camera Control Registers—Address Page 2

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R2:2(R0x202)	Base Matrix Signs	0000 000d dddd dddd	238 (0x00EE)
R3:2(R0x203)	Color Correction Matrices Scale Codes K1-K5	0ddd dddd dddd dddd	14627 (0x3923)
R4:2(R0x204)	Color Correction Matrices Scale Codes K6-K9	0000 dddd dddd dddd	1828 (0x0724)
R9:2(R0x209)	Base Matrix Color Correction Coefficient K1	0000 0000 dddd dddd	177 (0x00B1)
R10:2(R0x20A)	Base Matrix Color Correction Coefficient K2	0000 0000 dddd dddd	51 (0x0033)
R11:2(R0x20B)	Base Matrix Color Correction Coefficient K3	0000 0000 dddd dddd	47 (0x002F)
R12:2(R0x20C)	Base Matrix Color Correction Coefficient K4	0000 0000 dddd dddd	128 (0x0080)
R13:2(R0x20D)	Base Matrix Color Correction Coefficient K5	0000 0000 dddd dddd	240 (0x00F0)
R14:2(R0x20E)	Base Matrix Color Correction Coefficient K6	0000 0000 dddd dddd	96 (0x0060)
R15:2(R0x20F)	Base Matrix Color Correction Coefficient K7	0000 0000 dddd dddd	20 (0x0014)
R16:2(R0x210)	Base Matrix Color Correction Coefficient K8	0000 0000 dddd dddd	164 (0x00A4)
R17:2(R0x211)	Base Matrix Color Correction Coefficient K9	0000 0000 dddd dddd	220 (0x00DC)
R18:2(R0x212)	Current Color Correction Matrix Position	0000 0000 0??? ????	0 (0x0000)
R19:2(R0x213)	Current AWB Red Channel	0000 0000 ???? ????	140 (0x008C)
R20:2(R0x214)	Current AWB Blue Channel	0000 0000 ???? ????	157 (0x009D)
R21:2(R0x215)	Delta Matrix Signs	0000 000d dddd dddd	0 (0x0000)
R22:2(R0x216)	Delta Matrix Color Correction Coefficient D1	0000 0000 dddd dddd	0 (0x0000)
R23:2(R0x217)	Delta Matrix Color Correction Coefficient D2	0000 0000 dddd dddd	0 (0x0000)
R24:2(R0x218)	Delta Matrix Color Correction Coefficient D3	0000 0000 dddd dddd	0 (0x0000)
R25:2(R0x219)	Delta Matrix Color Correction Coefficient D4	0000 0000 dddd dddd	0 (0x0000)
R26:2(R0x21A)	Delta Matrix Color Correction Coefficient D5	0000 0000 dddd dddd	0 (0x0000)
R27:2(R0x21B)	Delta Matrix Color Correction Coefficient D6	0000 0000 dddd dddd	0 (0x0000)
R28:2(R0x21C)	Delta Matrix Color Correction Coefficient D7	0000 0000 dddd dddd	0 (0x0000)
R29:2(R0x21D)	Delta Matrix Color Correction Coefficient D8	0000 0000 dddd dddd	0 (0x0000)
R30:2(R0x21E)	Delta Matrix Color Correction Coefficient D9	0000 0000 dddd dddd	0 (0x0000)
R31:2(R0x21F)	Chroma Limits	0000 0000 dddd dddd	160 (0x00A0)
R32:2(R0x220)	AWB Luma Limits	dddd dddd dddd dddd	51220 (0xC814)
R33:2(R0x221)	Manual WB Red and Blue Gains	dddd dddd dddd dddd	32896 (0x8080)
R34:2(R0x222)	Red Gain AWB Limits	dddd dddd dddd dddd	55648 (0xD960)
R35:2(R0x223)	Blue Gain AWB Limits	dddd dddd dddd dddd	55648 (0xD960)
R36:2(R0x224)	AWB CCM Adjustment Limits	0ddd dddd 0ddd dddd	32512 (0x7F00)
R38:2(R0x226)	Auto Exposure Horizontal Window Boundaries	dddd dddd dddd dddd	32768 (0x8000)
R39:2(R0x227)	Auto Exposure Vertical Window Boundaries	dddd dddd dddd dddd	32776 (0x8008)
R40:2(R0x228)	AWB Advanced Control	dddd dddd dddd dddd	61186 (0xEF02)

Table 11: Camera Control Registers—Address Page 2 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R41:2(R0x229)	White Balance Gain Wide Stability Gates	dddd dddd dddd dddd	36211 (0x8D73)
R42:2(R0x22A)	WB Zone Validity Limits	dddd dddd dddd dddd	208 (0x00D0)
R43:2(R0x22B)	Auto Exposure Horizontal Center Window Boundaries	dddd dddd dddd dddd	24608 (0x6020)
R44:2(R0x22C)	Auto Exposure Vertical Center Window Boundaries	dddd dddd dddd dddd	24608 (0x6020)
R45:2(R0x22D)	AWB Window Boundaries	dddd dddd dddd dddd	24977 (0x6191)
R46:2(R0x22E)	Auto Exposure Target and Precision Control	dddd dddd dddd dddd	2106 (0x083A)
R47:2(R0x22F)	Reserved	–	56932 (0xDE64)
R48:2(R0x230)	AWB Red Measurement	0000 0000 ???? ????	123 (0x007B)
R49:2(R0x231)	AWB Luminance Measurement	0000 0000 ???? ????	135 (0x0087)
R50:2(R0x232)	AWB Blue Measurement	0000 0000 ???? ????	109 (0x006D)
R51:2(R0x233)	Reserved	–	8209 (0x2011)
R52:2(R0x234)	Auto Exposure Decision Frequency	0000 0000 dddd dddd	0 (0x0000)
R54:2(R0x236)	Auto Exposure Gain Limits	dddd dddd dddd dddd	40976 (0xA010)
R55:2(R0x237)	Reserved	–	128 (0x0080)
R56:2(R0x238)	Reserved	–	1088 (0x0440)
R57:2(R0x239)	Reserved	–	1716 (0x06B4)
R58:2(R0x23A)	Reserved	–	1716 (0x06B4)
R59:2(R0x23B)	Reserved	–	1260 (0x04EC)
R60:2(R0x23C)	Reserved	–	1278 (0x04FE)
R61:2(R0x23D)	Reserved	–	6108 (0x17DC)
R62:2(R0x23E)	CCM Adjustment Gain Threshold	000d dddd dddd dddd	8191 (0x1FFF)
R63:2(R0x23F)	Auto Exposure Current Gain Zone	???? ???? ???? ????	2 (0x0002)
R70:2(R0x246)	Reserved	–	55552 (0xD900)
R75:2(R0x24B)	Reserved	–	4 (0x0004)
R76:2(R0x24C)	Auto Exposure Current Luma Monitor	???? ???? ???? ????	15488 (0x3C80)
R77:2(R0x24D)	Auto Exposure Time Averaged Luma Monitor	0000 0000 ???? ????	59 (0x003B)
R79:2(R0x24F)	Reserved	–	169 (0x00A9)
R87:2(R0x257)	Reserved	–	525 (0x020D)
R88:2(R0x258)	Reserved	–	625 (0x0271)
R89:2(R0x259)	Reserved	–	500 (0x01F4)
R90:2(R0x25A)	Reserved	–	500 (0x01F4)
R91:2(R0x25B)	Flicker Control	?000 0000 0000 0ddd	32770 (0x8002)
R92:2(R0x25C)	Reserved	–	4108 (0x100C)
R93:2(R0x25D)	Reserved	–	5392 (0x1510)
R94:2(R0x25E)	Base Sensor Core Gain Ratios	dddd dddd dddd dddd	30789 (0x7845)

Table 11: Camera Control Registers—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R95:2(R0x25F)	Delta Sensor Core Gain Ratios	dddd dddd dddd dddd	20007 (0x4E27)
R96:2(R0x260)	Delta Sensor Core Gain Ratio Signs	0000 0000 0000 00dd	2 (0x0002)
R97:2(R0x261)	AWB Analog Gain Ratios Monitor	???? ???? ???? ????	40753 (0x9F31)
R98:2(R0x262)	Auto Exposure Digital Gain Monitor	???? ???? ???? ????	4112 (0x1010)
R99:2(R0x263)	Reserved	–	12330 (0x302A)
R100:2(R0x264)	Reserved	–	23036 (0x59FC)
R101:2(R0x265)	Auto Exposure Luma Offset	0000 00dd dddd dddd	0 (0x0000)
R103:2(R0x267)	Auto Exposure Digital Gain Limits	dddd dddd dddd dddd	8208 (0x2010)
R104:2(R0x268)	Reserved	–	17 (0x0011)
R106:2(R0x26A)	Reserved	–	0 (0x0000)
R107:2(R0x26B)	Reserved	–	0 (0x0000)
R108:2(R0x26C)	Reserved	–	126 (0x007E)
R109:2(R0x26D)	Reserved	–	126 (0x007E)
R110:2(R0x26E)	Reserved	–	62 (0x003E)
R111:2(R0x26F)	Reserved	–	126 (0x007E)
R112:2(R0x270)	Reserved	–	110 (0x006E)
R113:2(R0x271)	Reserved	–	66 (0x0042)
R114:2(R0x272)	Reserved	–	66 (0x0042)
R115:2(R0x273)	Reserved	–	2 (0x0002)
R116:2(R0x274)	Reserved	–	122 (0x007A)
R117:2(R0x275)	Reserved	–	114 (0x0072)
R118:2(R0x276)	Reserved	–	78 (0x004E)
R119:2(R0x277)	Reserved	–	118 (0x0076)
R120:2(R0x278)	Reserved	–	94 (0x005E)
R121:2(R0x279)	Reserved	–	126 (0x007E)
R122:2(R0x27A)	Reserved	–	68 (0x0044)
R123:2(R0x27B)	Reserved	–	64 (0x0040)
R124:2(R0x27C)	Reserved	–	64 (0x0040)
R125:2(R0x27D)	Reserved	–	0 (0x0000)
R130:2(R0x282)	Reserved	–	1023 (0x03FF)
R131:2(R0x283)	Reserved	–	769 (0x0301)
R132:2(R0x284)	Reserved	–	193 (0x00C1)
R133:2(R0x285)	Reserved	–	929 (0x03A1)
R134:2(R0x286)	Reserved	–	980 (0x03D4)
R135:2(R0x287)	Reserved	–	983 (0x03D7)

Table 11: Camera Control Registers—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R136:2(R0x288)	Reserved	–	921 (0x0399)
R137:2(R0x289)	Reserved	–	1016 (0x03F8)
R138:2(R0x28A)	Reserved	–	28 (0x001C)
R139:2(R0x28B)	Reserved	–	957 (0x03BD)
R140:2(R0x28C)	Reserved	–	987 (0x03DB)
R141:2(R0x28D)	Reserved	–	957 (0x03BD)
R142:2(R0x28E)	Reserved	–	1020 (0x03FC)
R143:2(R0x28F)	Reserved	–	990 (0x03DE)
R144:2(R0x290)	Reserved	–	990 (0x03DE)
R145:2(R0x291)	Reserved	–	990 (0x03DE)
R146:2(R0x292)	Reserved	–	990 (0x03DE)
R147:2(R0x293)	Reserved	–	31 (0x001F)
R148:2(R0x294)	Reserved	–	65 (0x0041)
R149:2(R0x295)	Reserved	–	867 (0x0363)
R150:2(R0x296)	Reserved	–	0 (0x0000)
R151:2(R0x297)	Reserved	–	384 (0x0180)
R152:2(R0x298)	Reserved	–	255 (0x00FF)
R153:2(R0x299)	Reserved	–	1 (0x0001)
R156:2(R0x29C)	Reserved	–	57120 (0xDF20)
R180:2(R0x2B4)	Reserved	–	32 (0x0020)
R181:2(R0x2B5)	Reserved	–	257 (0x0101)
R198:2(R0x2C6)	Reserved	–	0 (0x0000)
R199:2(R0x2C7)	Reserved	–	0 (0x0000)
R200:2(R0x2C8)	Reserved	–	7947 (0x1F0B)
R201:2(R0x2C9)	Reserved	–	0 (0x0000)
R202:2(R0x2CA)	Reserved	–	43264 (0xA900)
R203:2(R0x2CB)	Reserved	–	0 (0x0000)
R204:2(R0x2CC)	Reserved	–	0 (0x0000)
R205:2(R0x2CD)	Reserved	–	8608 (0x21A0)
R206:2(R0x2CE)	Reserved	–	7835 (0x1E9B)
R207:2(R0x2CF)	Reserved	–	19018 (0x4A4A)
R208:2(R0x2D0)	Reserved	–	5773 (0x168D)
R209:2(R0x2D1)	Reserved	–	77 (0x004D)
R210:2(R0x2D2)	Reserved	–	0 (0x0000)
R211:2(R0x2D3)	Reserved	–	0 (0x0000)

Table 11: Camera Control Registers—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number Dec(Hex)	Register Description	Data Format (Binary)	Default Value Dec(Hex)
R212:2(R0x2D4)	Reserved	–	520 (0x0208)
R213:2(R0x2D5)	Reserved	–	0 (0x0000)
R239:2(R0x2EF)	Reserved	–	8 (0x0008)
R240:2(R0x2F0)	Page Map	0000 0000 0000 0ddd	2 (0x0002)
R241:2(R0x2F1)	Bytewise Addr	dddd dddd dddd dddd	0 (0x0000)
R242:2(R0x2F2)	AWB Red and Blue Gains Offsets	dddd dddd dddd dddd	0 (0x0000)
R243:2(R0x2F3)	Reserved	–	685 (0x02AD)
R245:2(R0x2F5)	Reserved	–	64 (0x0040)
R246:2(R0x2F6)	Reserved	–	127 (0x007F)
R247:2(R0x2F7)	Reserved	–	1728 (0x06C0)
R248:2(R0x2F8)	Reserved	–	1728 (0x06C0)
R249:2(R0x2F9)	Reserved	–	1360 (0x0550)
R250:2(R0x2FA)	Reserved	–	1280 (0x0500)
R251:2(R0x2FB)	Reserved	–	525 (0x020D)
R252:2(R0x2FC)	Reserved	–	625 (0x0271)
R253:2(R0x2FD)	Reserved	–	502 (0x01F6)
R254:2(R0x2FE)	Reserved	–	502 (0x01F6)
R255:2(R0x2FF)	Reserved	–	43136 (0xA880)

Sensor Core Register Descriptions—Address Page 0

Table 12: Sensor Core Registers—Address Page 0

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R0:0 R0x000	15:0	0x129E	Chip Version (RO)		
	15:8	0x0012	Reserved		
	7:4	0x0009	Reserved		
	3	0x0001	Reserved		
	2:0	0x0006	Reserved		
	Chip version. Read only				
R1:0 R0x001	15:0	0x0015	Row Start (R/W)	Y	N
	The first row of the output frame. A value of 21 (default value) starts the output frame at the first active row. Changing this register is not advised since the image would be moved out of the visible area.				
R2:0 R0x002	15:0	0x002E	Column Start (R/W)	N	N
	The first column of the output frame. A value of 46 (default value) starts the output frame at the first active column; use only the default value for correct NTSC or PAL operation.				
R5:0 R0x005	15:0	0x00D2	Horizontal Blanking (R/W)	Y	N
	Number of blank columns in a row. Use only the default values for correct NTSC or PAL operation. Default for NTSC: 0xD2; PAL: 0xD8.				
R6:0 R0x006	15:0	0x000E	Odd Field Vertical Blanking (R/W)	N	N
	Number of rows in the odd vertical blanking period. Use only the default values for correct NTSC or PAL operation. Default for NTSC: 0x0E; PAL: 0x40.				
R7:0 R0x007	15:0	0x00F0	Field Height (R/W)	N	Y
	Field height in rows. One half the pixel array image rows, output in each field for NTSC or PAL operation modes. Default value set to 240. Use only the default value for correct NTSC or PAL operation.				
R9:0 R0x009	15:0	0x0106	Shutter Width (R/W)	Y	N
	Integration time in number of rows. The total integration time is also influenced by the shutter delay (R12:0) and the integration-overhead time.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R10:0 R0x00A	15:0	0x0011	Sensor Clock Control (R/W)		
	15:14	0x0000	Reserved		
	13	0x0000	Reserved		
	12:9	X	Reserved		
	8	0x0000	Invert pixel clock For SOC bypass mode only. 0: FRAME_VALID, LINE_VALID, and Dout are set up relative to the delayed rising edge of PIXCLK. 1: FRAME_VALID, LINE_VALID, and Dout are set up relative to the delayed falling edge of PIXCLK.	N	N
	7:4	0x0001	Reserved		
	3:0	0x0001	Reserved		
R11:0 R0x00B	15:0	0x0000	Extra Delay (R/W)	N	N
	Extra vertical blanking inserted between frames. A programmed value of N increases the vertical blanking time by N pixel clock periods. Can be used to get a more exact frame rate. It may affect the integration times of parts of the image when the integration time is less than one frame. Use only the default value for correct NTSC and PAL operation.				
R12:0 R0x00C	15:0	0x0000	Shutter Delay (R/W)	N	N
	The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. If the value in this register exceeds the row time, the reset of the row does not complete before the associated row is sampled, and the sensor does not generate an image. A programmed value of N reduces the integration time by N pixel clock periods.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R13:0 R0x00D	15:0	0x0108	Reset and Standby Control (R/W)		
	15	0x0000	Synchronize changes 0: Default operation, updates changes to registers that affect image brightness at the next frame boundary (integration time, integration delay, gain, horizontal blanking and vertical blanking, or row mirror). 1: Inhibits this update; register changes remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register updates are made on the next frame start.	N	N
	14	X	Reserved		
	13	0x0000	Stop SOC 0: SOC clocks are enabled. 1: SOC clocks are disabled.	N	N
	12	0x0000	Reserved		
	11	X	Reserved		
	10	0x0000	Toggle two-wire serial interface address 0: By default, the sensor serial bus responds to addresses 0xBA and 0xBB. 1: The sensor serial bus responds to addresses 0x90 and 0x91. Writes to this bit are ignored when STANDBY is asserted. See "Slave Address" on page 117.	N	N
	9	0x0000	Restart bad frames 0: No restart is forced for bad frames. 1: A restart is forced to take place whenever a bad frame is detected. This can shorten the delay when waiting for a good frame since the delay, when masking out a bad frame and performing a restart, is the integration time rather than the full frame time.	N	N
	8	0x0001	Show bad frames 0: Only output good frames (default). 1: Output all frames (including bad frames). A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, mirroring, or use of border.	N	N
	7	0x0000	Inhibit standby from pin By default, asserting the STANDBY pin places the sensor in a low-power state. 0: Normal operation. 1: Stops the STANDBY pin from affecting entry to or exit from the low-power state. See "Power-Saving Modes" on page 108.	N	N
	6	0x0000	Standby output enable 0: Asserting STANDBY causes the pin interface to enter a High-Z (default). 1: Stops STANDBY from contributing to output-enable control.	N	N
	5	0x0000	Reset SOC registers 0: Resume the SOC. 1: Reset to SOC (only).	N	N

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
	4	0x0000	Output disable 0: Normal operation. 1: Output signals are tri-stated.	N	N
	3	0x0001	Chip enable 0: Stop sensor readout. When this is returned to 1, sensor readout restarts and begins resetting the starting row in a new frame. To reduce the digital power, the master clock to the sensor can be disabled or the standby pin can be used. 1: Normal operation.	N	N
	2	0x0000	Analog standby 0: Normal operation 1: Place the sensor in a low-power state. See "Power-Saving Modes" on page 108. Note: setting this bit will effect NTSC and PAL operation.	N	N
	1	0x0000	Restart sensor 0: Normal operation. 1: Causes the sensor to truncate the current frame and start resetting the first row. The delay before the first valid frame is read out is equal to the integration time. This bit always reads back as 0.	N	N
	0	0x0000	Reset registers 0: Resume normal operation 1: Puts the sensor in reset; the frame being generated is truncated and the pin interface goes to an idle state. All internal registers (except for this bit) go to the default power-up state.	N	N
R17:0	15:0	0x000F	Even Field Vertical Blanking (R/W)	Y	N
R0x011	Vertical blanking in rows, between two fields in interlaced modes (NTSC or PAL). To keep correct NTSC or PAL timing, this register must be programmed with the default values. Default for NTSC: 0x0F; PAL: 0x41.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R32:0 R0x020	15:0	0x0300	Read Mode (R/W)		
	15	0x0000	XOR LINE_VALID with FRAME_VALID 0: LINE_VALID = LINE_VALID 1: XOR LINE_VALID with FRAME_VALID	N	N
	14	0x0000	LINE_VALID during vertical blanking 0: Normal LINE_VALID (default, no LINE_VALID during vertical blank). 1: "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking).	N	N
	13:10	X	Reserved		
	9	0x0001	Show border 0: Do not show the border. 1: This bit indicates whether to show the border enabled by bit 8. When bit 8 is 0, this bit has no meaning. When bit 8 is 1, this bit decides whether the border pixels should be treated as extra active pixels (1) or extra blanking pixels (0). Must be set for correct NTSC and PAL operation.	N	N
	8	0x0001	Readout border pixels 0: Do not read out border pixels. 1: A 4-pixel border is output around the active image array independent of readout mode (mirror and so forth). Setting this bit therefore adds 4 to the numbers of rows and columns in the frame. Must be set for correct NTSC and PAL operation.	N	N
	7	0x0000	Reserved		
	6	0x0000	Reserved		
	5:4	X	Reserved		
	3	0x0000	First field even in PAL mode 0: The first PAL field output consists of odd-numbered rows of the pixel array, and the second field consists of even-numbered rows. 1: The first PAL field output consists of even-numbered rows of pixel the array, and the second field consists of odd-numbered rows.	N	N
	2	0x0000	First field even in NTSC mode 0: The first NTSC field output consists of odd-numbered rows of the pixel array. The second field consists of even-numbered rows. 1: The first NTSC field output consists of even-numbered rows of pixel array. The second field consists of odd-numbered rows.	N	N
	1	X	Reserved		
	0	0x0000	Mirror rows 0: Rows not mirrored (sensor reads top to bottom). 1: Rows mirrored (image flipped vertically, sensor reads bottom to top). To mirror columns (horizontal flip), see R21:1 bit 1.	N	N

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R34:0 R0x022	15:0	0x010D	Dark Column and Row Control (R/W)		
	15:10	X	Reserved		
	9	0x0000	Show dark columns in output frame 0: Do not show dark columns. 1: The programmed dark columns are output before the active pixels in a line. The dark columns are usually read out during horizontal blank. The horizontal blanking time is therefore decreased by the same amount that is added to the active line when this bit is enabled. This feature does not work in the NTSC and PAL output modes.	N	N
	8	0x0001	Read dark columns 0: An arbitrary number of dark columns can be read out by including them in the active image. 1: Enables the readout of dark columns 23:4 for use in the row-wise noise correction algorithm. Enabling the dark columns increases the minimum value for horizontal blanking but does not affect the row time.	N	N
	7	0x0000	Show dark rows in output frame 0: Do not show dark rows. 1: The programmed dark rows are output before the active window along with the extra rows between the dark and active rows. FRAME_VALID is thus asserted earlier than normal. This has no effect on integration time or frame rate. This feature does not work in the NTSC and PAL output modes.	N	N
	6:4	0x0000	Reserved		
	3	0x0001	Reserved		
	2:0	0x0005	Reserved		
	When bit 7 is set, dark and extra rows (always 2) are shown. Bit 8 and 9 decide if the dark columns are to be read and shown, respectively.				
R36:0 R0x024	15:0	0x4000	Extra Reset (R/W)		
	15	X	Reserved		
	14	0x0001	Reset next row	N	N
	13:0	X	Reserved		
	Setting bit 14 enables the next row reset logic. When enabled, the sensor logic resets also the next row to the row being reset by the shutter operation, when it is applicable. Note that in interlaced modes, the next row belongs to the next field. The condition is that the shutter width is less than one field time.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R43:0 R0x02B	15:0	0x0028	Green1 Gain (R/W)		
	15:12	X	Reserved		
	11:9	0x0000	Digital gain Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*Analog gain	N	N
	8:7	0x0000	Analog gain Analog gain = [Bit8 +1]*[Bit7 +1]*Initial gain	N	N
	6:0	0x0028	Initial gain Initial gain = bits[6:0] * 0.03125. A value of 32 corresponds to a gain of 1.0.	N	N
	The initial analog gain is equal to the value in bits [6:0] multiplied by 0.03125 (1/32). For each 1 in the bits 7 and 8, the total gain is doubled. Bits [11:9] are used in the sensor logic; for each "1" in these bits, the data from the ADC is doubled (that is, the total gain is doubled). Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*[Bit8 +1]*[Bit7 +1]*Initial Gain.				
R44:0 R0x02C	15:0	0x0064	Blue Gain (R/W)		
	15:12	X	Reserved		
	11:9	0x0000	Digital gain Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*Analog gain	N	N
	8:7	0x0000	Analog gain Analog gain = [Bit8 +1]*[Bit7 +1]*Initial gain	N	N
	6:0	0x0064	Initial gain Initial gain = bits[6:0] * 0.03125. A value of 32 corresponds to a gain of 1.0.	N	N
	The initial analog gain is equal to the value in bits [6:0] multiplied by 0.03125 (1/32). For each 1 in the bits 7 and 8, the total gain is doubled. Bits [11:9] are used in the sensor logic; for each "1" in these bits, the data from the ADC is doubled (that is, the total gain is doubled). Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*[Bit8 +1]*[Bit7 +1]*Initial gain.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R45:0 R0x02D	15:0	0x001E	Red Gain (R/W)		
	15:12	X	Reserved		
	11:9	0x0000	Digital gain Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*Analog gain	N	N
	8:7	0x0000	Analog gain Analog gain = [Bit8 +1]*[Bit7 +1]*Initial Gain	N	N
	6:0	0x001E	Initial gain Initial gain = bits[6:0] * 0.03125. A value of 32 corresponds to a gain of 1.0.	N	N
	The initial analog gain is equal to the value in bits [6:0] multiplied by 0.03125 (1/32). For each 1 in the bits 7 and 8, the total gain is doubled. Bits [11:9] are used in the sensor logic; for each "1" in these bits, the data from the ADC is doubled (that is, the total gain is doubled). Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*[Bit8 +1]*[Bit7 +1]*Initial gain.				
R46:0 R0x02E	15:0	0x0028	Green2 Gain (R/W)		
	15:12	X	Reserved		
	11:9	0x0000	Digital gain Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*Analog gain	N	N
	8:7	0x0000	Analog gain Analog gain = [Bit8 +1]*[Bit7 +1]*Initial gain	N	N
	6:0	0x0028	Initial gain Initial gain = bits[6:0] * 0.03125. A value of 32 corresponds to a gain of 1.0.	N	N
	The initial analog gain is equal to the value in bits [6:0] multiplied by 0.03125 (1/32). For each 1 in the bits 7 and 8, the total gain is doubled. Bits [11:9] are used in the sensor logic; for each "1" in these bits, the data from the ADC is doubled (that is, the total gain is doubled). Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*[Bit8 +1]*[Bit7 +1]*Initial gain.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R47:0 R0x02F	15:0	0x0028	Global Gain (R/W)		
	15	0x0000	Reserved		
	14:12	X	Reserved		
	11:9	0x0000	Digital gain Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*Analog gain	N	N
	8:7	0x0000	Analog gain Analog gain = [Bit8 +1]*[Bit7 +1]*Initial gain	N	N
	6:0	0x0028	Initial gain Initial gain = bits[6:0] * 0.03125. A value of 32 corresponds to a gain of 1.0.	N	N
	Writing a value to this register is equal to writing that value to the 4 gain registers: 0x2B:0, 0x2C:0, 0x2D:0 and 0x2E:0. When read, it returns the value stored in Reg0x2B:0. The initial analog gain is equal to the value in bits [6:0] multiplied by 0.03125 (1/32). For each 1 in the bits 7 and 8, the total gain is doubled. Bits [11:9] are used in the sensor logic; for each "1" in these bits, the data from the ADC is doubled (that is, the total gain is doubled). Total gain = [Bit11 +1]*[Bit10 +1]*[Bit9 +1]*[Bit8 +1]*[Bit7 +1]*Initial gain.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R48:0 R0x030	15:0	0x082A	Row Noise (R/W)		
	15	0x0000	Enable digital frame-wise correction When this bit is set, the black level is calculated and applied for each color of each of the four black rows and the same values are applied to each subsequent row so that new values are applied once per frame.	N	N
	14:12	0x0000	Gain threshold When the upper analog gain bits are equal to or larger than this threshold, the dark column average is used in the row noise correction algorithm. Otherwise, the subtracted value is determined by R48:0[11]. This check is performed independently for each color, and is a means to turn off the row noise correction algorithm for lower gains without affecting the black level out of the sensor. Typical threshold values are 0, 1, 3 and 7. (0 - x1/32 - x1/16; 1 - x2 - x16; 3 - x4 - x16; 7 - x8 - x16).	N	N
	11	0x0001	Use black level average 0: Use the mean of the black level programmed threshold in the row noise correction algorithm for low gains. 1: Use the black level frame average from the dark rows in the row noise correction algorithm for low gains. Note: this frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off.	N	N
	10	0x0000	Enable correction 0: Normal operation. 1: Enable row noise cancellation algorithm. The average value of the dark columns read out is used as a correction for the whole row. The dark average is subtracted from each pixel on the row, and then a constant is added (R48:0[9:0]).	N	N
	9:0	0x002A	Row noise constant Constant used in the row noise cancellation algorithm. It should be set to the dark level targeted by the black level algorithm plus the noise expected between the averaged values of the dark columns. The default constant is set to 42 LSB.	N	N
R91:0 R0x05B	15:0	0x0020	Dark Green1 Frame Average (RO)	N	N
	The frame-averaged green1 black level that is used in the black level calibration algorithm.				
R92:0 R0x05C	15:0	0x0022	Dark Blue Frame Average (RO)	N	N
	The frame-averaged blue black level that is used in the black level calibration algorithm.				
R93:0 R0x05D	15:0	0x001F	Dark Red Frame Average (RO)	N	N
	The frame-averaged red black level that is used in the black level calibration algorithm.				
R94:0 R0x05E	15:0	0x0020	Dark Green2 Frame Average (RO)	N	N
	The frame-averaged green2 black level that is used in the black level calibration algorithm.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R95:0 R0x05F	15:0	0x231D	Black Level Calibration Threshold (R/W)		
	15	X	Reserved		
	14:8	0x0023	Thres_hi Upper threshold for targeted black level in ADC LSBs.	N	N
	7	X	Reserved		
	6:0	0x001D	Thres_lo Lower threshold for targeted black level in ADC LSBs.	N	N
R96:0 R0x060	15:0	0x0080	Black Level Calibration Control (R/W)		
	15:9	X	Reserved		
	8	0x0000	Enable calibration sweep mode 0: Disable calibration sweep mode 1: The calibration value is increased by one every frame, and all channels are the same. This can be used to get a ramp input to the ADC from the calibration DACs.	N	N
	7:5	0x0004	Frames to average over 2 to the power of this value determines how many frames to average when the black level algorithm is in the averaging mode. In this mode, the running frame average is calculated from the following formula: Running frame ave = old running frame ave - (old running frame ave)/2n + (new frame ave)/ 2n.	N	N
	4	0x0000	Keep step size at 1 0: Start at a higher step size when in rapid sweep mode, to converge faster to the correct value. (Default) 1: The step size is forced to "1" for the rapid sweep algorithm.	N	N
	3	0x0000	Reserved		
	2	0x0000	Use red calib value for blue 1: The same calibration value is used for red and blue pixels: Calib blue = calib red.	N	N
	1	0x0000	Use green1 calib value for green2 1: The same calibration value is used for all green pixels: Calib green2 = calib green1.	N	N
	0	0x0000	Manual override auto black level Manual override of black level correction. 0: Normal operation (default). 1: Override automatic black level correction with programmed values. (R0x61:0 to R0x64:0).	N	N
R97:0 R0x061	15:0	0x0024	Green1 Offset Calibration Value (R/W)	N	N
	Analog calibration offset for green1 pixels, represented as a two's complement 8-bit value (range: -256 to 255). If R0x60:0[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x60:0[0] = 1, this register is R/W and can be used to set the calibration offset manually. Green1 pixels share rows with red pixels.				

Table 12: Sensor Core Registers—Address Page 0 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name	Frame Sync'd	Bad Frame
R98:0 R0x062	15:0	0x0026	Blue Offset Calibration Value (R/W)	N	N
	Analog calibration offset for blue pixels, represented as a two's complement 8-bit value (range: -256 to 255). If R0x60:0[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x60:0[0] = 1, this register is R/W and can be used to set the calibration offset manually.				
R99:0 R0x063	15:0	0x0024	Red Offset Calibration Value (R/W)	N	N
	Analog calibration offset for red pixels, represented as a two's complement 8-bit value (range: -256 to 255). If R0x60:0[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x60:0[0] = 1, this register is R/W and can be used to manually set the calibration offset.				
R100:0 R0x064	15:0	0x0025	Green2 Offset Calibration Value (R/W)	N	N
	Analog calibration offset for green2 pixels, represented as a two's complement 8-bit value (range: -256 to 255). If R0x60:0[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x60:0[0] = 1, this register is R/W and can be used to manually set the calibration offset. Green2 pixels share rows with blue pixels.				
R240:0 R0x0F0	15:0	0x0000	Page Map (R/W)	N	N
	Set camera chip register page. 0: Sensor core 1: ColorPipe 2: Camera control.				
R241:0 R0x0F1	15:0	0x0000	Bytewise Addr (R/W)	N	N
	Special address to perform 8-bit (instead of 16-bit) READs and WRITEs to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 118 and "Appendix A: Serial Bus Description" on page 116.				
R255:0 R0x0FF	15:0	0x129E	Chip Version (RO)	N	N
	Chip version. Read only.				

Color Pipe Register Descriptions—Address Page 1

Table 13: Color Pipe Register—Address Page 1
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R5:1 R0x105	15:0	0x000B	Aperture Correction (R/W)
	15:4	X	Reserved
	3	0x0001	Enable Auto sharpening Enables automatic sharpness reduction control.
	2:0	0x0003	Sharpening factor Sharpening factor: 000: No Sharpening. 001: 25% Sharpening. 010: 50% Sharpening. 011: 75% Sharpening. 100: 100% Sharpening. 101: 125% Sharpening. 110: 150% Sharpening. 111: 200% Sharpening.
	Aperture correction scale factor used for sharpening.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R6:1 R0x106	15:0	0x640E	Operating Mode Control (R/W)
	15	0x0000	Manual white balance Enables manual white balance. User can set the base matrix and color channel gains. This bit must be asserted and de-asserted with a frame in between to force new color-correction settings to take effect.
	14	0x0001	Auto exposure Enables auto exposure.
	13	0x0001	Defect correction Enables on-the-fly defect correction.
	12	0x0000	Clip aperture correction Clips aperture corrections. Small aperture corrections (<8) are attenuated to reduce noise amplification.
	11	0x0000	Not used Not used.
	10	0x0001	Lens shading correction Enables lens shading correction.
	9:8	0x0000	Reserved
	7	0x0000	AE flicker control enable Enables flicker control.
	6	0x0000	Enable the interpolator in 2D defect correction This bit should be set to a "1" when operating in the interlace mode.
	5	0x0000	Reserved
	4	0x0000	Bypass color correction matrix Bypasses color-correction matrix. 0: Normal color processing. 1: Outputs "raw" color bypassing color correction.
	3:2	0x0003	AE back light control Auto exposure back light compensation control. 00: Auto exposure sampling window is specified by R38:2 and R39:2 ("large window"). 01: Auto exposure sampling window is specified by R43:2 and R44:2 ("small window"). 1x: Auto exposure sampling window is specified by the weighted sum of the large window and the small window, with the small window weighted four times more heavily. (Where x = "0" or "1").
	1	0x0001	Enables auto white balance Enables auto white balance. 0: Freezes white balance at current values. 1: Enables auto white balance.
	0	0x0000	Reserved Reserved for future expansion.
	This register specifies the operating mode of the IFP.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R8:1 R0x108	15:0	0x0080	Output Format Control (R/W)
	15:11	0x0000	Reserved Reserved for future expansion.
	10	0x0000	Gate PIXCLK 0: PIXCLK not gated 1: PIXCLK gated with LINE_VALID
	9	0x0000	Flip Bayer column Flip Bayer columns in processed Bayer output mode. 0: Column order is green, red and blue, green. 1: Column order is red, green and green, blue.
	8	0x0000	Flip Bayer row Flip Bayer row in processed Bayer output mode. 0: First row contains green and red; the second row contains blue and green. 1: First row contains blue and green; the second row contains green and red.
	7	0x0001	Ctls CCIR656 protection bits Controls the values used for the protection bits in Rec. ITU-R BT.656 codes. 0: Use zeros for the protection bits. 1: Use the correct values.
	6	X	Reserved
	5	0x0000	Multiplex Y[YCbCr] or G[RGB] Multiplexes Y (in YCbCr mode) or green (in RGB mode) channel on all channels (monochrome). 0: Normal operation 1: Forces Y or G onto all channels.
	4	0x0000	Disable Cb Disables Cb color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode. 0: Normal operation. 1: Forces Cb to 128 or B to 0.
	3	0x0000	Disable Y Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode. 0: Normal operation. 1: Forces Y to 128 or G to 0.
	2	0x0000	Disable Cr Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode. 0: Normal operation. 1: Forces Cr to 128 or R to 0.
	1	0x0000	Bayer CFA [vert shift] Toggles the assumptions about Bayer vertical shift. 0: Row containing red comes first. 1: Row containing blue comes first.

Table 13: Color Pipe Register—Address Page 1 (continued)

0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R19:1 R0x113	15:0	0x0780	Chip level control (R/W)
	15:11	X	Reserved
	10	0x0001	Din[7:0] and DIN_CLK input enable Setting this bit enables Din[7:0] and DIN_CLK input pads. This bit can be cleared for floating Din[7:0] and DIN_CLK inputs
	9	0x0001	Din_CLK hysteresis enable Enable the hysteresis of the Din_CLK pad in a noisy environment.
	8	0x0001	EXT_CLK hysteresis enable Enable the hysteresis of the EXT_CLK pad in a noisy environment.
	7	0x0001	FRAME_VALID odd field to even field level 0: FRAME_VALID drops between even and odd frames. 1: FRAME_VALID remains HIGH between even and odd fields. Also LINE_VALID drops when FRAME_VALID is HIGH. This ensures that the 243 active lines of each field (even and odd) can be identified by LINE_VALID = FRAME_VALID = 1.
	6	0x0000	INV_F Invert the F bit in the 656 generated bit stream.
	5	X	Reserved
	4	0x0000	Select Din_CLK 0: Select the internal 2X pixel clock as the clock for latching the Din[7:0] data. 1: Select the external Din_CLK as the clock for latching the Din[7:0] data.
	3	0x0000	DIN sample edge 0: Use the positive edge of the muxed (DIN_CLK/internal 2X pixel clock) to latch the Din[7:0] data. 1: Use the negative edge.
	2	0x0000	TV encoder select ext DSP 0: TV encoder selects the internal SOC output as its input data. 1: TV encoder selects the data from external Din[7:0] port as its input data.
	1:0	0x0000	Dout[7:0] select 00: CCIR656 data stream (interlaced) is selected. Dout[7:0] = CCIR656 data. Dout_LSB[1:0] = 0x0. 01: Reserved 10: SOC colorpipe output is selected. 11: Reserved
	Controls several chip level input/output parameters		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R21:1 R0x115	15:0	0x0000	Invert Latched Pins (R/W)
	15:3	X	Reserved
	2	0x0000	XORed with the latched PEDESTAL The PEDESTAL pin status latched in R30:1 is XORed with this bit before it is used. Software uses this bit to enable or disable the pedestal.
	1	0x0000	XORed with the latched HORIZ_FLIP The HORIZ_FLIP pin status latched in R30:1 is XORed with this bit before it is used. Software uses this bit to flip the image on the horizontal axis.
	0	0x0000	XORed with the latched NTSC_PAL_SEL The NTSC_PAL_SEL pin status latched in R30:1 is XORed with this bit before it is used. Software uses this pin to switch between NTSC and PAL.
	The status of pins (PEDESTAL, HORIZ_FLIP, NTSC_PAL_SEL) are latched at reset into R30:1. Bits in R30:1 are XORed with this register (R21:1) before they are used.		
R29:1 R0x11D	15:0	0x2000	LVDS Control Register (R/W)
	15:14	X	Reserved
	13	0x0001	LVDS power down When this bit is set or the pad LVDS_ENABLE is low or if the pad STANDBY is set, the LVDS output is disabled.
	12	0x0000	PLL test enable 0: Normal operation. 1: Enable testing the PLL in the LVDS module.
	11	0x0000	LVDS test enable 0: Normal operation. 1: LVDS start and stop bits are replaced with R29:1[10] (LVDS_TESTDATA), LVDS data is replaced with R29:1[9:0] (LVDS_DATA).
	10	0x0000	LVDS_TESTDATA When R29:1[11] (LVDS_TEST) is 1, LVDS start and stop bits are replaced with this bit.
	9:0	0x0000	LVDS test data When R29:1[11] (LVDS_TEST) is 0, normal data is sent to the LVDS. When R29:1[11] is 1, the value of this field is sent to the LVDS.
	This is used for debugging/testing the LVDS module.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R30:1 R0x11E	15:0	0x0004	Latched Pin Status (RO)
	15:3	X	Reserved
	2	RO	PEDESTAL PEDESTAL pin latched during reset.
	1	RO	HORIZ_FLIP HORIZ_FLIP pin latched at reset.
	0	RO	NTSC_PAL_SEL NTSC_PAL_SEL pin latched at reset.
	This register is used to latch the PEDESTAL, HORIZ_FLIP, NTSC_PAL_SEL pin status during reset and is accessible (RO) through the two-wire serial interface.		
R37:1 R0x125	15:0	0x0005	Color Saturation Control (R/W)
	15:6	X	Reserved
	5:3	0x0000	Overall attenuation of saturation Specify overall attenuation of the color saturation. 000: Full color saturation 001: 75% of full saturation 010: 50% of full saturation 011: 37.5% of full saturation 100: 25% of full saturation 101: 150% of full saturation 110: Black and white
	2:0	0x0005	Reserved
	This register specifies the color saturation control settings.		
R52:1 R0x134	15:0	0x0010	Luma Offset [Can be used to Control Brightness] (R/W)
	15:8	0x0000	Offset in RGB mode Offset in RGB mode
	7:0	0x0010	Y offset in YCbCr mode Y offset in YCbCr mode
	Offset added to the luma prior to output.		
R53:1 R0x135	15:0	0xF010	Luma Clip (R/W)
	15:8	0x00F0	Upper limit Highest value of output luma.
	7:0	0x0010	Lower limit Lowest value of output luminance.
	Clipping limits for output luma.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R59:1 R0x13B	15:0	0x0416	Black Subtraction (R/W)
	15:11	X	Reserved
	10	0x0001	Enables subtraction of BL- Enables subtraction of black level negative offset from the signal, before lens shading correction. 0: No black level subtraction performed. 1: Subtraction enabled.
	9:0	0x0016	Black level minus offset [BL-] Black level negative offset. Set this value to Row Noise Constant, R48:0 [9:0], the black level in the signal from the sensor core. The first block of the IFP subtracts black level negative offset from the sensor core signal. The objective is to remove any pedestal before lens shading correction and auto exposure digital gains.
	Defines and enables black level negative offset. Controls reduction of the black level in the signal from the sensor core before lens shading correction auto exposure digital gains.		
R60:1 R0x13C	15:0	0x0400	Black Addition (R/W)
	15:11	X	Reserved
	10	0x0001	Enables addition of black level plus offset (BL+) Enables addition of black level positive offset to the lens shading corrected signal. 0: No addition performed. 1: Addition enabled.
	9:0	0x0000	Black level positive offset [BL+] This value is added to each pixel value, after lens shading correction and auto exposure digital gains. Black level positive can be used to raise the black level subsequent IFP processing.
	Defines and enables black level positive offset. Controls raising the black level in the signal after lens shading correction and auto exposure digital gains.		
R72:1 R0x148	15:0	0x0000	Test Pattern Generator Control (R/W)
	15:8	X	Reserved
	7	0x0000	1: Force white balance digital gains to 1.0 0: Normal operation. 1: Forces white balance digital gains to 1.0 (disable digital gains).
	6:3	X	Reserved
	2:0	0x0000	Test pattern at the beginning of IFP Test pattern at the beginning of IFP.
	This register enables test pattern generation at the input of the image processor. Values greater than 0 turn on the test pattern generator. 0: Select the sensor image. 1 to 6: The brightness of the flat color areas depends on the value programmed (from 1 to 6) in this register. 7: Produces the color bar pattern.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R128:1 R0x180	15:0	0x0003	Lens Correction Control (R/W)
	15:7	X	Reserved
	6	0x0000	Reserved This bit is unused. This bit is reserved for future use.
	5	0x0000	Reserved This bit is unused. This bit is reserved for future use.
	4:2	0x0000	Kxy scaling The coefficient, "kp" or "Kxy," of the cross-term. A 3-bit code determines the value of kp. 000: 0 001: 1 010: 2 011: 4 100: 8 Others: 8
	1:0	0x0003	Kx; Ky The scaling factor, "kd" or "Kx," for derivative or knee values. A two-bit code determines the value of kd: 00: 1 01: 0.5 10: 0.25 11: 0.125
	Defines the scaling factor and the cross-term coefficient for lens shading correction.		
R129:1 R0x181	15:0	0xED05	Lens Vertical Red Knee 0 and Initial Value (R/W)
	15:8	0x00ED	Red vertical knee pt 0 Value of red vertical derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the vertical term of the red compensation function.
	7:0	0x0005	Red vertical initial value Initial value of red vertical function. Initial value of the vertical term of the red compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1, toggling all bits, then adding 1.		
R130:1 R0x182	15:0	0x0EDC	Lens Vertical Red Knees 2 and 1 (R/W)
	15:8	0x000E	Red vertical knee pt 2 Value of red vertical derivative at vertex (knee) 2. Value at vertex 2 value of the piecewise linear derivative of the vertical term of the red compensation function.
	7:0	0x00DC	Red vertical knee pt 1 Value of red vertical derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the vertical term of the red compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R131:1 R0x183	15:0	0xEF09	Lens Vertical Red Knees 4 and 3 (R/W)
	15:8	0x00EF	Red vertical knee pt 4 Value of red vertical derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the vertical term of the red-compensation function.
	7:0	0x0009	Red vertical knee pt 3 Value of red vertical derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the vertical term of the red compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R132:1 R0x184	15:0	0xED05	Lens Vertical Green Knee 0 and Initial Value (R/W)
	15:8	0x00ED	Green vertical knee pt 0 Value of green vertical derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the vertical term of the green compensation function.
	7:0	0x0005	Green vertical initial value Initial value of green vertical function. Initial value of the vertical term of the green compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R133:1 R0x185	15:0	0x0EDC	Lens Vertical Green Knees 2 and 1 (R/W)
	15:8	0x000E	Green vertical knee pt 2 Value of green vertical derivative at vertex (knee) 2. Value, at vertex 2, of the piecewise linear derivative of the vertical term of the green compensation function.
	7:0	0x00DC	Green vertical knee pt 1 Value of green vertical derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the vertical term of the green compensation function.
	Knee (vertex) values are in two's compliment representation, for example, 0xFF is equivalent to -1.		
R134:1 R0x186	15:0	0xEF09	Lens Vertical Green Knees 4 and 3 (R/W)
	15:8	0x00EF	Green vertical knee pt 4 Value of green vertical derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the vertical term of the green compensation function.
	7:0	0x0009	Green vertical knee pt 3 Value of green vertical derivative of vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the vertical term of the green compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R135:1 R0x187	15:0	0xED05	Lens Vertical Blue Knee 0 and Initial Value (R/W)
	15:8	0x00ED	Blue vertical knee pt 0 Value of blue vertical derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the vertical term of the blue compensation function.
	7:0	0x0005	Blue vertical initial value Initial value of blue vertical function. Initial value of the vertical term of the blue compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R136:1 R0x188	15:0	0x0EDC	Lens Vertical Blue Knees 2 and 1 (R/W)
	15:8	0x000E	Blue vertical knee pt 2 Value of blue vertical derivative at vertex (knee) 2. Value, at vertex 2, of the piecewise linear derivative of the vertical term of the blue compensation function.
	7:0	0x00DC	Blue vertical knee pt 1 Value of blue vertical derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the vertical term of the blue compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R137:1 R0x189	15:0	0xEF09	Lens Vertical Blue Knees 4and 3 (R/W)
	15:8	0x00EF	Blue vertical knee pt 4 Value of blue vertical derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the vertical term of the blue compensation function.
	7:0	0x0009	Blue vertical knee pt 3 Value of blue vertical derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the vertical term of the blue compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R138:1 R0x18A	15:0	0xE809	Lens Horizontal Red Knee 0 and Initial Value (R/W)
	15:8	0x00E8	Red horizontal knee pt 0 Value of red horizontal derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the horizontal term of the red compensation function.
	7:0	0x0009	Red horizontal initial value Initial value of red horizontal function. Initial value of the horizontal term of the red compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R139:1 R0x18B	15:0	0xF8F4	Lens Horizontal Red Knees 2 and 1 (R/W)
	15:8	0x00F8	Red horizontal knee pt 2 Value of red horizontal derivative at vertex (knee) 2. Value, at vertex 2, of the piecewise linear derivative of the horizontal term of the red compensation function.
	7:0	0x00F4	Red horizontal knee pt 1 Value of red horizontal derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the horizontal term of the red compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R140:1 R0x18C	15:0	0xEFF4	Lens Horizontal Red Knees 4 and 3 (R/W)
	15:8	0x00EF	Red horizontal knee pt 4 Value of red horizontal derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the horizontal term of the red compensation function.
	7:0	0x00F4	Red horizontal knee pt 3 Value of red horizontal derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the horizontal term of the red compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R141:1 R0x18D	15:0	0x0002	Lens Horizontal Red Knee 5 (R/W)
	15:8	X	Reserved
	7:0	0x0002	Red horizontal knee pt 5 Value of red horizontal derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the horizontal term of the red compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R142:1 R0x18E	15:0	0xE809	Lens Horizontal Green Knee 0 and Initial Value (R/W)
	15:8	0x00E8	Green horizontal knee pt 0 Value of green horizontal derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the horizontal term of the green compensation function.
	7:0	0x0009	Green horizontal initial value Initial value of green horizontal function. Initial value of the horizontal term of the green compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R143:1 R0x18F	15:0	0xF8F4	Lens Horizontal Green Knees 2 and 1 (R/W)
	15:8	0x00F8	Green horizontal knee pt 2 Value of green horizontal derivative at vertex (knee) 2. Value, at vertex 2, of the piecewise linear derivative of the horizontal term of the green compensation function.
	7:0	0x00F4	Green horizontal knee pt 1 Value of green horizontal derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the horizontal term of the green compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R144:1 R0x190	15:0	0xEFF4	Lens Horizontal Green Knees 4 and 3 (R/W)
	15:8	0x00EF	Green horizontal knee pt 4 Value of green horizontal derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the horizontal term of the green compensation function.
	7:0	0x00F4	Green horizontal knee pt 3 Value of green horizontal derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the horizontal term of the green compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R145:1 R0x191	15:0	0x0002	Lens Horizontal Green Knee 5 (R/W)
	15:8	X	Reserved
	7:0	0x0002	Green horizontal knee pt 5 Value of green horizontal derivative at vertex (knee) 5. Value, at vertex 5, of the piecewise linear derivative of the horizontal term of the green compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R146:1 R0x192	15:0	0xE809	Lens Horizontal Blue Knee 0 and Initial Value (R/W)
	15:8	0x00E8	Blue horizontal knee pt 0 Value of blue horizontal derivative at vertex (knee) 0. Value, at vertex 0, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	7:0	0x0009	Blue horizontal initial value Initial value of blue horizontal function. Initial value of the horizontal term of the blue compensation function.
	Initial values are unsigned, positive. Knee values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R147:1 R0x193	15:0	0xF8F4	Lens Horizontal Blue Knees 2 and 1 (R/W)
	15:8	0x00F8	Blue horizontal knee pt 2 Value of blue horizontal derivative at vertex (knee) 2. Value, at vertex 2, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	7:0	0x00F4	Blue horizontal knee pt 1 Value of blue horizontal derivative at vertex (knee) 1. Value, at vertex 1, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R148:1 R0x194	15:0	0xEFF4	Lens Horizontal Blue Knees 4 and 3 (R/W)
	15:8	0x00EF	Blue horizontal knee pt 4 Value of blue horizontal derivative at vertex (knee) 4. Value, at vertex 4, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	7:0	0x00F4	Blue horizontal knee pt 3 Value of blue horizontal derivative at vertex (knee) 3. Value, at vertex 3, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R149:1 R0x195	15:0	0x0002	Lens Horizontal Blue Knee 5 (R/W)
	15:8	X	Reserved
	7:0	0x0002	Blue horizontal knee pt 5 Value of blue horizontal derivative at vertex (knee) 5. Value, at vertex 5, of the piecewise linear derivative of the horizontal term of the blue compensation function.
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R153:1 R0x199	15:0	0x0050	Line Counter (RO)
	Use line counter to determine the number of the line currently being output.		
R154:1 R0x19A	15:0	0x01A7	Frame Counter (RO)
	Use frame counter to determine the index of the frame currently being output.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R155:1 R0x19B	15:0	0x0200	Output Format Control 2 (R/W)
	15	X	Reserved
	14	0x0000	Output processed Bayer Output processed Bayer data.
	13	0x0000	Debug flicker luma Reserved.
	12	0x0000	SOC as sensor stand-alone mode Sensor output coupled directly to SOC camera port, including two extra LSB pins to provide access to the full 10-bit sensor output. Bits [9:2] of the sensor output are mapped to Dout[7:0]. Bits [1:0] of the sensor output are mapped to Dout_LSB1 and Dout_LSB0, respectively.
	11	0x0000	CCIR656 codes Enables embedding Rec. ITU-R BT.656 synchronization codes to the output data.
	10	0x0000	Bypass IP Entire image processing is bypassed and raw Bayer is output directly. In YCbCr or RGB mode: 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; that is, 8+2. Data rate is effectively the same as default 16-bits /per pixel modes. Auto exposure, AWB, and other features still function and control the sensor, though they are assuming some gain or correction through the colorpipe.
	9	0x0001	Invert output pixel clock By default, this bit is asserted and data is launched off the falling edge of PIXCLK for capture by the receiver on the rising edge.
	8	0x0000	Enable RGB output 0: Output YCbCr data. 1: Output RGB format data as defined by R155:1[7:6].
	7:6	0x0000	RGB output format 00: 16-bit RGB565. 01: 15-bit RGB555 10: 12-bit RGB444x. 11: 12-bit RGBx444.
	5:4	0x0000	Test pattern at the end of IFP (ramp) 00: Off. 01: By column. 10: By row. 11: By frame.
	3	0x0000	Reserved
	2	0x0000	Reserved
	1	0x0000	Swap bytes In YCbCr mode, swaps C and Y bytes. In RGB mode, swaps odd and even bytes.

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R157:1 R0x19D	15:0	0x24AE	Defect Correction Control (R/W)
	15	X	Reserved
	14:8	0x0024	Reserved Reserved.
	7:5	0x0005	Relative threshold Relative threshold for defect detection.
	4:0	0x000E	Absolute threshold Absolute threshold for defect detection.
	Defect correction control.		
R167:1 R0x1A7	15:0	0x0280	Reducer Horizontal Output Size Resize (R/W)
	15:11	X	Reserved
	10:0	0x0280	Horiz size of output image X Size.
	Controls reducer horizontal output size.		
R170:1 R0x1AA	15:0	0x00F0	Reducer Vertical Output Size Resize (R/W)
	15:11	X	Reserved
	10:0	0x00F0	Vert size of output image Y Size.
	Controls reducer vertical output size.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R175:1 R0x1AF	15:0	0x0800	Reducer Zoom Control (R/W)
	15:12	X	Reserved
	11	0x0001	EN_EXPAND 0: Display 640 pixels per line 1: Enable the line expander to interpolate the input image lines from 642 pixels per line to 720 pixels per line for the NTSC and PAL modes of operation.
	10	X	Reserved
	9	0x0000	Reserved
	8	0x0000	Reserved
	7	X	Reserved
	6	0x0000	Reserved
	5	0x0000	Reserved
	4	0x0000	Reserved
	3	0x0000	Reserved
	2	X	Reserved
	1	0x0000	Reserved
	0	0x0000	Reserved
	R175:1[11] controls horizontal expansion for NTSC and PAL.		
R182:1 R0x1B6	15:0	0x0000	Lens Vertical Red Knees 6 and 5 (R/W)
	15:8	0x0000	Red vertical knee pt 6
	7:0	0x0000	Red vertical knee pt 5
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R183:1 R0x1B7	15:0	0x0000	Lens Vertical Red Knees 8 and 7 (R/W)
	15:8	0x0000	Red vertical knee pt 8
	7:0	0x0000	Red vertical knee pt 7
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R184:1 R0x1B8	15:0	0x0000	Lens Vertical Green Knees 6 and 5 (R/W)
	15:8	0x0000	Green vertical knee pt 6
	7:0	0x0000	Green vertical knee pt 5
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R185:1 R0x1B9	15:0	0x0000	Lens Vertical Green Knees 8 and 7 (R/W)
	15:8	0x0000	Green vertical knee pt 8
	7:0	0x0000	Green vertical knee pt 7
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R186:1 R0x1BA	15:0	0x0000	Lens Vertical Blue Knees 6 and 5 (R/W)
	15:8	0x0000	Blue vertical knee pt 6
	7:0	0x0000	Blue vertical knee pt 5
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R187:1 R0x1BB	15:0	0x0000	Lens Vertical Blue Knees 8 and 7 (R/W)
	15:8	0x0000	Blue vertical knee pt 8
	7:0	0x0000	Blue vertical knee pt 7
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R188:1 R0x1BC	15:0	0x0210	Lens Horizontal Red Knees 7 and 6 (R/W)
	15:8	0x0002	Red horizontal knee pt 7
	7:0	0x0010	Red horizontal knee pt 6
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R189:1 R0x1BD	15:0	0x020E	Lens Horizontal Red Knees 9 and 8 (R/W)
	15:8	0x0002	Red horizontal knee pt 9
	7:0	0x000E	Red horizontal knee pt 8
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R190:1 R0x1BE	15:0	0x0017	Lens Horizontal Red Knee 10 (R/W)
	15:8	X	Reserved
	7:0	0x0017	Red horizontal knee pt 10
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R191:1 R0x1BF	15:0	0x0210	Lens Horizontal Green Knees 7 and 6 (R/W)
	15:8	0x0002	Green horizontal knee pt 7
	7:0	0x0010	Green horizontal knee pt 6
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R192:1 R0x1C0	15:0	0x020E	Lens Horizontal Green Knees 9 and 8 (R/W)
	15:8	0x0002	Green horizontal knee pt 9
	7:0	0x000E	Green horizontal knee pt 8
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R193:1 R0x1C1	15:0	0x0017	Lens Horizontal Green Knee 10 (R/W)
	15:8	X	Reserved
	7:0	0x0017	Green horizontal knee pt 10
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R194:1 R0x1C2	15:0	0x0210	Lens Horizontal Blue Knees 7 and 6 (R/W)
	15:8	0x0002	Blue horizontal knee pt 7
	7:0	0x0010	Blue horizontal knee pt 6
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R195:1 R0x1C3	15:0	0x020E	Lens Horizontal Blue Knees 9 and 8 (R/W)
	15:8	0x0002	Blue horizontal knee pt 9
	7:0	0x000E	Blue horizontal knee pt 8
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R196:1 R0x1C4	15:0	0x0017	Lens Horizontal Blue Knee 10 (R/W)
	15:8	X	Reserved
	7:0	0x0017	Blue horizontal knee pt 10
	Knee (vertex) values are in two's complement representation, for example, 0xFF is equivalent to -1.		
R220:1 R0x1DC	15:0	0x1005	Gamma Knee Y2 and Y1 (R/W)
	15:8	0x0010	Y2
	7:0	0x0005	Y1
	This register specifies output values Y1 and Y2 for the piecewise linear gamma correction. Piecewise linear gamma correction transforms 10-bit luminance from color processing to nonlinear 8-bit luminance to be output from the chip. Pre-gamma image processing generates 10-bit luminance values ranging from 0 through 896. Piecewise linear gamma correction has 10 linear intervals with knee points corresponding to the following input values: Xi = 0 ... 10 = {0, 16, 32, 64, 128, 256, 384, 512, 640, 768, 896}. For each input value Xi, the user can program the corresponding output value Yi as illustrated in the accompanying text in this table. The valid range for Yi is from 0 through 255. A further offset is added to the gamma corrected values as specified in R52:1. Default values for gamma table knee points implemented a gamma of 0.6.		
R221:1 R0x1DD	15:0	0x582F	Gamma Knee Y3 and Y4 (R/W)
	15:8	0x0058	Y4
	7:0	0x002F	Y3
	This register specifies output values Y3 and Y4 for the piecewise linear gamma correction. For a description of the gamma correction table, see R220:1.		
R222:1 R0x1DE	15:0	0x9B80	Gamma Knee Y5 and Y6 (R/W)
	15:8	0x009B	Y6
	7:0	0x0080	Y5
	This register specifies output values Y5 and Y6 for the piecewise linear gamma correction. For a description of the gamma correction table, see R220:1.		

Table 13: Color Pipe Register—Address Page 1 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R223:1 R0x1DF	15:0	0xC2B0	Gamma Knee Y7 and Y8 (R/W)
	15:8	0x00C2	Y8
	7:0	0x00B0	Y7
	This register specifies output values Y7 and Y8 for the piecewise linear gamma correction. For a description of the gamma correction table, see R220:1.		
R224:1 R0x1E0	15:0	0xE0D2	Gamma Knee Y9 and Y10 (R/W)
	15:8	0x00E0	Y10
	7:0	0x00D2	Y9
	This register specifies output values Y9 and Y10 for the piecewise linear gamma correction. For a description of the gamma correction table, see R220:1. The final output luminance is clamped to Y10.		
R225:1 R0x1E1	15:0	0x0000	Gamma Knee Y0 (R/W)
	15:8	X	Reserved
	7:0	0x0000	Y0
	This register specifies output value Y0 corresponding to 0 input of the piecewise linear gamma correction. For a description of the gamma correction table, see R220:1.		
R240:1 R0x1F0	15:0	0x0001	Page Map (R/W)
	Set camera chip register page. 0: Sensor core 1: Colorpipe 2: Camera control.		
R241:1 R0x1F1	15:0	0x0000	Bytewise Addr (R/W)
	Special address to perform 8-bit (instead of 16-bit) READs and WRITEs to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 118 and "Appendix A: Serial Bus Description" on page 116.		

Camera Control Register Descriptions—Address Page 2

Table 14: Camera Control Register—Address Page 2
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R2:2 R0x202	15:0	0x00EE	Base Matrix Signs (R/W)
	15:9	X	Reserved
	8	0x0000	K1 (Always positive) The sign of K1 is always positive; this bit is always 0.
	7	0x0001	Sign of K2
	6	0x0001	Sign of K3
	5	0x0001	Sign of K4
	4	0x0000	K5 (Always positive) The sign of K5 is always positive; this bit is always 0.
	3	0x0001	Sign of K6
	2	0x0001	Sign of K7
	1	0x0001	Sign of K8
	0	0x0000	K9 (Always positive) The sign of K9 is always positive; this bit is always 0.
	This register specifies the signs of the 9 coefficients in the base color correction matrix. ("0" = positive; "1" = negative)		
R3:2 R0x203	15:0	0x3923	Color Correction Matrices Scale Codes K1-K5 (R/W)
	15	X	Reserved
	14:12	0x0003	Scaling of K5
	11:9	0x0004	Scaling of K4
	8:6	0x0004	Scaling of K3
	5:3	0x0004	Scaling of K2
	2:0	0x0003	Scaling of K1
	This register specifies the scaling of coefficients K1 through K5 of the color correction matrices. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC. The magnitudes of all coefficients are stored as 8-bit unsigned integers. The scaling scheme accommodates fractional coefficient magnitudes in the range from 0.004 through 15.93. Prior to loading, fractional coefficients are multiplied by 16, 32, 64, 128, or 256 and rounded to the nearest integer. For maximum accuracy, the scale factor should be selected so that the scaled coefficient is as close as possible to, but not exceeding, 255. The power of 2 used for scaling in excess of 4 is specified as a 3-bit value in R3:2 and R4:2. The encoding is: 000: Scale by 16. 001: Scale by 32. 010: Scale by 64. 011: Scale by 128. 100: Scale by 256. A single scale factor is used for the corresponding coefficients in the base and delta matrices.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R4:2 R0x204	15:0	0x0724	Color Correction Matrices Scale Codes K6-K9 (R/W)
	15:12	X	Reserved
	11:9	0x0003	Scaling of K9
	8:6	0x0004	Scaling of K8
	5:3	0x0004	Scaling of K7
	2:0	0x0004	Scaling of K6
	This register specifies the scaling of color correction coefficients K6 through K9 of the color correction matrices. Refer to R3:2 for more details.		
R9:2 R0x209	15:0	0x00B1	Base Matrix Color Correction Coefficient K1 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K1.		
R10:2 R0x20A	15:0	0x0033	Base Matrix Color Correction Coefficient K2 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K2.		
R11:2 R0x20B	15:0	0x002F	Base Matrix Color Correction Coefficient K3 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K3.		
R12:2 R0x20C	15:0	0x0080	Base Matrix Color Correction Coefficient K4 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K4.		
R13:2 R0x20D	15:0	0x00F0	Base Matrix Color Correction Coefficient K5 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K5.		
R14:2 R0x20E	15:0	0x0060	Base Matrix Color Correction Coefficient K6 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K6.		
R15:2 R0x20F	15:0	0x0014	Base Matrix Color Correction Coefficient K7 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K7.		
R16:2 R0x210	15:0	0x00A4	Base Matrix Color Correction Coefficient K8 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K8.		
R17:2 R0x211	15:0	0x00DC	Base Matrix Color Correction Coefficient K9 (R/W)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K9.		
R18:2 R0x212	15:0	0x0000	Current Color Correction Matrix Position (RO)
	This register specifies the current position of the color correction matrix relative to the original calibration matrices. The matrix position is expressed as a 7-bit number represented in 0.bbbbbbb fixed point format. Positions range from 0/128 for red-rich illumination to 127/128 for blue-rich illumination.		
R19:2 R0x213	15:0	0x008C	Current AWB Red Channel (RO)
	This register reports the current value of the red digital gain as an 8-bit number in b.bbbbbbb fixed point format, which ranges from 0/128 to 255/128.		
R20:2 R0x214	15:0	0x009D	Current AWB Blue Channel (RO)
	This register reports the current value of the blue digital gain as an 8-bit number in b.bbbbbbb fixed point format, which ranges from 0/128 to 255/128.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R21:2 R0x215	15:0	0x0000	Delta Matrix Signs (R/W)
	15:9	X	Reserved
	8	0x0000	Sign of D1
	7	0x0000	Sign of D2
	6	0x0000	Sign of D3
	5	0x0000	Sign of D4
	4	0x0000	Sign of D5
	3	0x0000	Sign of D6
	2	0x0000	Sign of D7
	1	0x0000	Sign of D8
	0	0x0000	Sign of D9
	This register specifies the signs of the 9 coefficients of the delta color correction matrix. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R22:2 R0x216	15:0	0x0000	Delta Matrix Color Correction Coefficient D1 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D1. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R23:2 R0x217	15:0	0x0000	Delta Matrix Color Correction Coefficient D2 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D2. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R24:2 R0x218	15:0	0x0000	Delta Matrix Color Correction Coefficient D3 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D3. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R25:2 R0x219	15:0	0x0000	Delta Matrix Color Correction Coefficient D4 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D4. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R26:2 R0x21A	15:0	0x0000	Delta Matrix Color Correction Coefficient D5 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D5. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R27:2 R0x21B	15:0	0x0000	Delta Matrix Color Correction Coefficient D6 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D6. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R28:2 R0x21C	15:0	0x0000	Delta Matrix Color Correction Coefficient D7 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D7. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R29:2 R0x21D	15:0	0x0000	Delta Matrix Color Correction Coefficient D8 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D8. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R30:2 R0x21E	15:0	0x0000	Delta Matrix Color Correction Coefficient D9 (R/W)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D9. Refer to the description of R9:2 for a detailed description of the color correction matrices used in the SOC.		
R31:2 R0x21F	15:0	0x00A0	Chroma Limits (R/W)
	15:8	X	Reserved
	7:6	0x0002	Relative limit Relative test, which compares the magnitudes of the 7-bit chroma to the largest 8-bit RGB component for the pixel: 00: Test always passes. 01: chroma < 1/4 max_color. 10: chroma < 1/2 max_color. 11: chroma < max_color.
	5:0	0x0020	Absolute limit Absolute test: both chroma must lie below this value
	This register controls chroma tests that prevent deeply saturated colors from skewing the white balance statistics. Pixels that do not pass these tests are not counted.		
R32:2 R0x220	15:0	0xC814	AWB Luma Limits (R/W)
	15:8	0x00C8	Upper limit Upper limit of luminance for white balance statistics.
	7:0	0x0014	Lower limit Lower limit of luminance for white balance statistics.
	To avoid skewing white balance statistics by very dark or very bright values, this register represents the luminance range of pixels to be used for white balance statistics. These limits are 8-bit values represented as 0.bbbbbbbb fixed point format in the range of 0/256 through 224/256.		
R33:2 R0x221	15:0	0x8080	Manual WB Red and Blue Gains (R/W)
	15:8	0x0080	Red gain Red channel gain.
	7:0	0x0080	Blue gain Blue channel gain.
	This register stores the red and blue color channel gains for use when manual white balance is enabled (R6:1[15] is "1"). The programmed values represent the desired gains as 8-bit numbers in b.bbbbbbb fixed point format, which range from 0/128 through 255/128. As an example, unity gain has the value 128 (0x80).		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R34:2 R0x222	15:0	0xD960	Red Gain AWB Limits (R/W)
	15:8	0x00D9	Upper limit Upper limit of red channel gain.
	7:0	0x0060	Lower limit Lower limit of red channel gain.
	This register sets the range of red gain adjustment by the AWB algorithm. These limits depend on the normalization of the color correction matrices programmed in R9:2-R17:2 and R22:2-R30:2. To preserve full-range red, a lower limit below 0.75 is not recommended when using default matrices. The 8-bit gain limits are represented in b.bbbbbbb fixed point format. Values range from 0/128 through 255/128.		
R35:2 R0x223	15:0	0xD960	Blue Gain AWB Limits (R/W)
	15:8	0x00D9	Upper limit Upper limit of blue channel gain.
	7:0	0x0060	Lower limit Lower limit of blue channel gain.
	This register sets the range of blue gain adjustment by the AWB algorithm. These limits depend on the normalization of the color correction matrices programmed in R9:2-R17:2 and R22:2-R30:2. To preserve full-range blue, a lower limit below 0.75 is not recommended when using default matrices. The 8-bit gain limits are represented in b.bbbbbbb fixed point format. Values range from 0/128 through 255/128.		
R36:2 R0x224	15:0	0x7F00	AWB CCM Adjustment Limits (R/W)
	15	X	Reserved
	14:8	0x007F	Upper limit Upper limit of the matrix position.
	7	X	Reserved
	6:0	0x0000	Lower limit Lower limit of the matrix position.
	As described in R18:2, AWB determines the best position of the color correction matrix by interpolating between 2 edge matrices: one for red-rich illumination and one for blue-rich illumination. The limits of the matrix position are expressed as 7-bit numbers represented in 0.bbbbbbb fixed point format. Positions range from 0/128 for red-rich illumination through 127/128 for blue-rich illumination.		
R38:2 R0x226	15:0	0x8000	Auto Exposure Horizontal Window Boundaries (R/W)
	15:8	0x0080	Right boundary
	7:0	0x0000	Left boundary
	This register specifies the left and right boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R39:2 R0x227	15:0	0x8008	Auto Exposure Vertical Window Boundaries (R/W)
	15:8	0x0080	Bottom boundary
	7:0	0x0008	Top boundary
	This register specifies the top and bottom boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the topmost edge of the frame.		
R40:2 R0x228	15:0	0xEF02	AWB Advanced Control (R/W)
	15	0x0001	Enable matrix normalization Reserved
	14	0x0001	Reserved
	13	0x0001	Reserved
	12	0x0000	Reserved
	11	0x0001	Reserved
	10	0x0001	Reserved
	9:8	0x0003	Reserved
	7	X	Reserved
	6:3	0x0000	Reserved
	2:0	0x0002	Reserved
	This register controls the rate of adaptation for the AWB algorithm.		
R41:2 R0x229	15:0	0x8D73	White Balance Gain Wide Stability Gates (R/W)
	15:8	0x008D	Upper gate
	7:0	0x0073	Lower gate
	This register describes the hysteresis window for AWB matrix motion. The 8-bit fields contain values in b.bbbbbbb fixed point format, which represent numbers from 0/128 through 255/128. Whenever the blue digital gain lies outside this window, it triggers AWB to move the color correction matrix toward a position with the blue digital gain near unity.		
R42:2 R0x22A	15:0	0x00D0	WB Zone Validity Limits (R/W)
	15:8	0x0000	Min number of open zones required for WB to operate Minimum number of zones that must be valid for the set of zones to be considered valid.
	7:4	0x000D	Upper limit Upper bound on the hue variation threshold.
	3:0	0x0000	Low limit Lower bound on the hue variation threshold.
	This register contains three parameters used in the white balance calculation to select regions of interest. The hue variation threshold parameters bound the range within which the hue variation threshold can wander as it attempts to keep the number of valid zones close to, but above, the minimum number of zones specified in the third parameter. This behavior attempts to keep the white balance algorithm focused on the most useful regions of the image while ignoring those that might imbalance the statistics.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R43:2 R0x22B	15:0	0x6020	Auto Exposure Horizontal Center Window Boundaries (R/W)
	15:8	0x0060	Right boundary Right window boundary.
	7:0	0x0020	Left boundary Left window boundary.
	This register specifies the left and right boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the leftmost edge of the frame.		
R44:2 R0x22C	15:0	0x6020	Auto Exposure Vertical Center Window Boundaries (R/W)
	15:8	0x0060	Top boundary Top window boundary.
	7:0	0x0020	Bottom boundary Bottom window boundary.
	This register specifies the top and bottom boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottommost edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the topmost edge of the frame.		
R45:2 R0x22D	15:0	0x6191	AWB Window Boundaries (R/W)
	15:12	0x0006	Bottom boundary Bottom window boundary (in units of blocks).
	11:8	0x0001	Top boundary Top window boundary (in units of blocks).
	7:4	0x0009	Right boundary Right window boundary (in units of 2 blocks).
	3:0	0x0001	Left boundary Left window boundary (in units of 2 blocks).
	This register specifies the boundaries of the window used by the WB measurement engine. It describes the window in terms relative to the size of the image: horizontally, in units of 1/10 of the width of the image; vertically, in units of 1/16 of the height of the image. Although the positioning is highly quantized, the window remains roughly in place as the resolution changes. More precisely, the values in the registers are the desired boundaries, in units of square blocks of pixels vertically, and in units of two such blocks horizontally. The size of the blocks is determined by the resolution of the image seen by the White Balance measurement engine and is 8x8, 16x16, 32x32, or 64x64 pixels. The block size is the smallest size that can cover the image with no more than 20 blocks horizontally and 16 blocks vertically. Using this concept of blocks, the window scales as the image size changes, albeit coarsely. Care must be taken when the aspect ratio of the image deviates substantially from that of a full-resolution image, as the horizontal and vertical dimensions suggest very different choices of block size. When this happens, the larger block size is selected, leading to greater quantization along one dimension.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R46:2 R0x22E	15:0	0x083A	Auto Exposure Target and Precision Control (R/W)
	15:8	0x0008	AE stability window and range Half-size of the AE target luma stability window.
	7:0	0x003A	Luminance value Luma value of the AE static target.
	This register specifies the luma target of the AE algorithm and the size of the window or range around the target in which no AE adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size. Bits R46:2[7:0] have a range of [0-224]. This is target luma that AE is attempting to achieve. Bits R46:2[15:8] is the half-width of the window around the target luma that provides hysteresis, that is, AE is considered adapted if the time averaged luma (R77:2) is equal to the value in R46:2[7:0] + or - R46:2[15:8]. Warning: Make sure that R46:2[7:0] - R46:2[15:8] remains nonnegative.		
R48:2 R0x230	15:0	0x007B	AWB Red Measurement (RO)
	This register outputs the WB measurement of red in the image. This value is normalized to an arbitrary value that is the same for R48:2, R49:2, and R50:2. Only the ratios between these registers are meaningful.		
R49:2 R0x231	15:0	0x0087	AWB Luminance Measurement (RO)
	This register outputs the WB measurement of luminance in the image. This value is normalized to an arbitrary value that is the same for R48:2, R49:2, and R50:2. Only the ratios between these registers are meaningful.		
R50:2 R0x232	15:0	0x006D	AWB Blue Measurement (RO)
	This register outputs the WB measurement of blue in the image. This value is normalized to an arbitrary value that is the same for R48:2, R49:2, and R50:2. Only the ratios between these registers are meaningful.		
R52:2 R0x234	15:0	0x0000	Auto Exposure Decision Frequency (R/W)
	Auto exposure luma is updated every N frames, where N is given by this register.		
R54:2 R0x236	15:0	0xA010	Auto Exposure Gain Limits (R/W)
	15:8	0x00A0	Upper limit Upper gain limit. The 8-bit value is in bbbb.bbbb fixed point format. The nominal value is about 1/2 the maximum possible analog gain.
	7:0	0x0010	Lower limit Lower gain limit. The 8-bit value is in bbbb.bbbb fixed point format. The nominal value is 1.0 (0x10).
	This register specifies upper and lower imager gain limits for the auto exposure algorithm. The values refers to virtual gains rather than the gains that can be programmed in the gains registers of the sensor core (R43:0 to R46:0, R53:0). Virtual gains range from 1 to 255, with 16 corresponding to a gain of 1.0, and 128 corresponding to a gain of 8. Virtual gains are mapped into sensor-specific analog gain settings; however the actual feasible gain limits are affected by the range of values that the red to green and blue to green ratios of AWB can assume. While the virtual gain setting developed by auto exposure directly controls the green analog gain, the red and blue virtual gains are derived from the gain ratios, and ultimately place a maximum bound on the green gain to avoid out-of-range analog gain values for the red and blue components. The minimum bound on virtual gain can be greater than 1.0 if the sensor needs a minimum signal gain in order to cover the full value range of the sensor's ADC.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R62:2 R0x23E	15:0	0x1FFF	CCM Adjustment Gain Threshold (R/W)
	15:13	X	Reserved
	12	0x0001	Automatic saturation control enable 0: Disable automatic color saturation control. 1: Enable automatic color saturation control.
	11:10	0x0003	Reserved
	9:8	0x0003	Reserved
	7:0	0x00FF	Reserved
R63:2 R0x23F	15:0	0x0002	Auto Exposure Current Gain Zone (RO)
	This register monitors the current value of the index to the exposure gains table. Zone of 0 indicates a bright image, with shutter widths set without regard to flicker abatement. Zones 1 through 3 reflect shutter widths that permit full frame rate. Zone 4 reflect increasing integration times, with a corresponding decrease in frame rate governed by the inclusive limits set in R54:2. Zone 4 is very low illumination.		
R76:2 R0x24C	15:0	0x3C80	Auto Exposure Current Luma Monitor (RO)
	The value of this register is the normalized sum of pre-gamma corrected luma samples, as determined by the AE backlight compensation field of the mode control register (R6:1, bits [3:2]). The format of this register is fixed point bbbbbbbb.bbbbbbbb, with a range of [0.0, 224.0].		
R77:2 R0x24D	15:0	0x003B	Auto Exposure Time Averaged Luma Monitor (RO)
	The value of this register is the time-averaged normalized sum of all the pre-gamma corrected luma samples (time-averaged luma), as determined by the AE backlight compensation field of the mode control register (R6:1, bits[3:2]). However, when the time-averaged luma moves outside the luma target range, the time averaging is disabled and this registers value becomes identical to that of R76:2[15:9].		
R91:2 R0x25B	15:0	0x8002	Flicker Control (R/W)
	15	RO	Reserved
	14:3	X	Reserved
	2	0x0000	Reserved
	1	0x0001	Manual 50/60 When in manual flicker mode (R91:2[0] = 1), defines which flicker frequency to avoid. 0: 50Hz 1: 60Hz
	0	0x0000	Auto/Manual
	Primary flicker control register.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R94:2 R0x25E	15:0	0x7845	Base Sensor Core Gain Ratios (R/W)
	15:8	0x0078	B ratio Base Blue/Green ratio = (BlueGain/GreenGain (right) + BlueGain/GreenGain (left)) / 2.
	7:0	0x0045	R ratio Base Red/Green ratio = (RedGain/GreenGain (right) + RedGain/GreenGain (left)) / 2.
	This register specifies the magnitudes of the base imager core analog gain ratios used during the calibration of the edge color correction matrices. As with the color correction matrix coefficients, the base ratios are the average of the ratios at the extreme calibration points. They are 8-bit numbers represented in bb.bbbbbb fixed point format. They are always positive.		
R95:2 R0x25F	15:0	0x4E27	Delta Sensor Core Gain Ratios (R/W)
	15:8	0x004E	B ratio Delta Blue/Green ratio = BlueGain/GreenGain (right) - BlueGain/GreenGain (left).
	7:0	0x0027	R ratio Delta Red/Green ratio = RedGain/GreenGain (right) - RedGain/GreenGain (left).
	This register specifies the magnitudes of the imager core analog gain ratio deltas derived from the calibration of the edge color correction matrices. As with the color correction matrix coefficients, the gain ratio deltas are the differences between the sensor gain ratios at the blue-rich and red-rich extreme calibration points. They are 8-bit numbers represented in bb.bbbbbb fixed point format. Their signs are stored in R96:2.		
R96:2 R0x260	15:0	0x0002	Delta Sensor Core Gain Ratio Signs (R/W)
	15:2	X	Reserved
	1	0x0001	Sign delta B Sign of the delta of the blue to green imager core analog gain ratios.
	0	0x0000	Sign delta R Sign of the delta of the red to green imager core analog gain ratios.
	This register specifies the signs of the deltas of the imager core analog gain ratios.		
R97:2 R0x261	15:0	0x9F31	AWB Analog Gain Ratios Monitor (RO)
	15:8	RO	Blue gain ratio Sensor analog gain ratio for blue and green.
	7:0	RO	Red gain ratio Sensor analog gain ratio for red and green.
	This register reflects the current values of the sensor analog gain ratios computed by the AWB unit.		
R98:2 R0x262	15:0	0x1010	Auto Exposure Digital Gain Monitor (RO)
	15:8	RO	Post lens correction digital gain Writable if AE is disabled, otherwise RO.
	7:0	RO	Pre lens correction digital gain Writable if AE is disabled, otherwise RO.
	These digital gains are applied within the IFP. They are independent of the imager gains and writable only when AE is disabled R6:1[14]=0.		

Table 14: Camera Control Register—Address Page 2 (continued)
0 = "Don't Care" bit, d = R/W (Read or Write) bit, ? = RO (Read Only) bit

Register Number	Bits	Default	Name
R101:2 R0x265	15:0	0x0000	Auto Exposure Luma Offset (R/W)
	This value is subtracted from all the pixel values that contribute to current luma (and time averaged luma). The resultant value is clamped at 0. The default value of this register should be at least the default value of colorpipe register, R60:1[9-0], if R60:1[10] is set.)		
R103:2 R0x267	15:0	0x2010	Auto Exposure Digital Gain Limits (R/W)
	15:8	0x0020	Post-Lens correction digital gain upper limit Maximum limit on post-lens correction digital gain.
	7:0	0x0010	Pre-Lens correction digital gain upper limit Maximum limit on pre-lens correction digital gain.
	This register specifies the upper limits of the digital gains used by the AE algorithm. The values programmed into this register are in bbbb.bbbb fixed point format. A gain of 1.0 is represented by the value of 16.		
R240:2 R0x2F0	15:0	0x0002	Page Map (R/W)
	Set camera chip register page. 0: Sensor core. 1: Colorpipe. 2: Camera control.		
R241:2 R0x2F1	15:0	0x0000	Bytewise Addr (R/W)
	Special address to perform 8-bit (instead of 16-bit) READs and WRITEs to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 118 and "Appendix A: Serial Bus Description" on page 116.		
R242:2 R0x2F2	15:0	0x0000	AWB Red and Blue Gains Offsets (R/W)
	15:8	0x0000	Red gain Red channel gain offset.
	7:0	0x0000	Blue gain offset Blue channel gain offset.
	This register stores the red and blue color channel gain offsets for use when AWB is enabled (R6:2[1] = "0"). The programmed values should represent the desired gain offsets in 1.7 fixed point format (b.bbbbbbb) (or multiplied by 128).		

Modes and Timing

This section provides an overview of the typical usage modes and related timing information for the MT9V135.

Composite Video Output

The analog composite video output is enabled by default and is the main usage mode for the MT9V135.

The external pin NTSC_PAL_SELECT can be used to configure the device for default NTSC or PAL operation. This and other video configuration settings are available as register settings accessible through the serial interface. For proper NTSC and PAL operation, use only default register values.

NTSC

Both differential and single connections of the full NTSC format are supported. The differential connection that uses two output lines is used for low noise or long distance applications. The single connection is used for PCB tracks and screened cable where noise is not a concern. The NTSC format has three black lines at the bottom of each image for padding (which most LCDs do not display).

PAL

The PAL format is supported with 480 active image rows only. Black bars are padded on top and bottom of the image for PAL format support. The PAL format has 24 black lines at the top and bottom of each image for padding.

NTSC or PAL with External Image Processing

The on-chip video encoder and DAC can be used with external data stream input (DIN[7:0] port). Correct NTSC or PAL formatted CCIR656 data is required for correct composite video output.

This mode can typically be used together with data output on the parallel DOUT[7:0] port—for example, for external overlay solutions.

Single-Ended and Differential Composite Output

The composite output can be operated in a single-ended or differential mode by simply changing the external resistor configuration. For single-ended termination, two schematics are presented. The first is SMPTE-compliant; the second is an alternative.

For differential mode termination, the first differential schematic; Figure 21 on page 100, is SMPTE-compliant.

See Figure 19 on page 99 through Figure 23 on page 101 for termination schematics.

Note: The differential schematics have not been tested.

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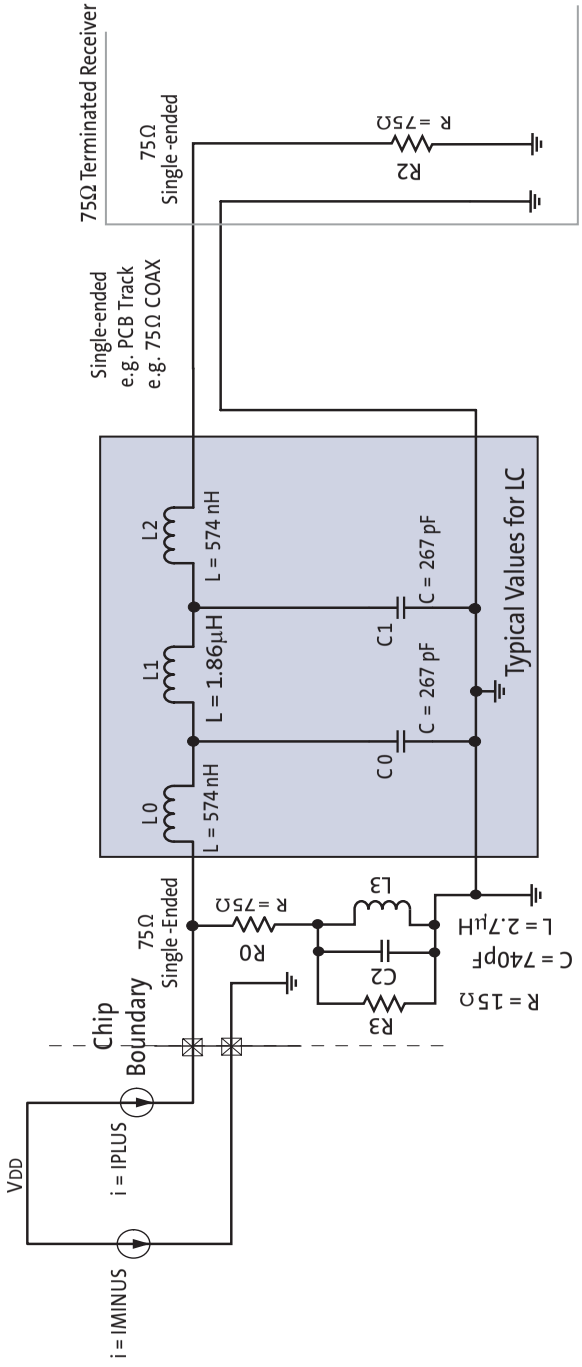


Figure 19: Single-Ended Termination—SMPTE Compliant

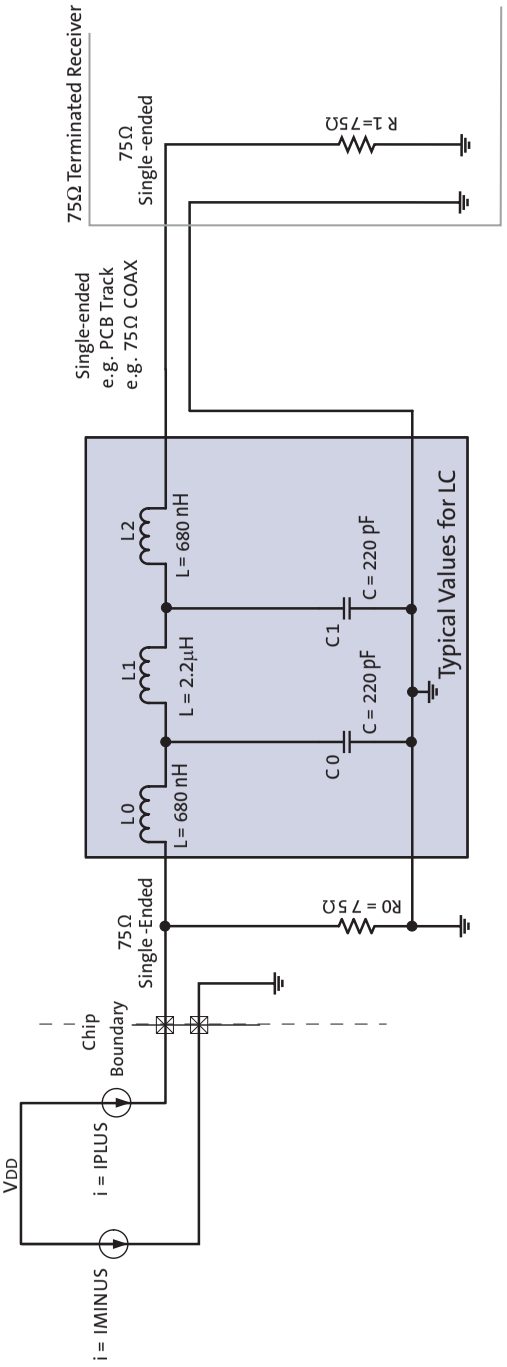


Figure 20: Single-Ended Termination

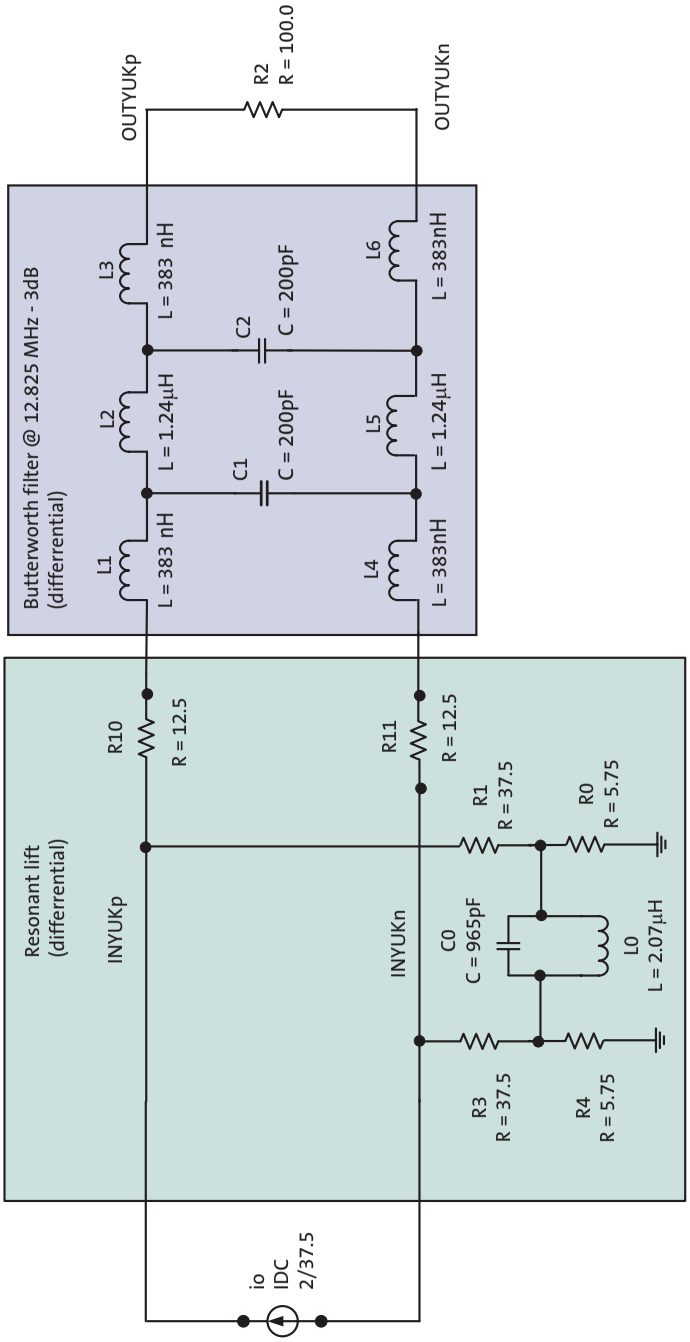


Figure 21: Differential Connection—SMPTE-Compliant

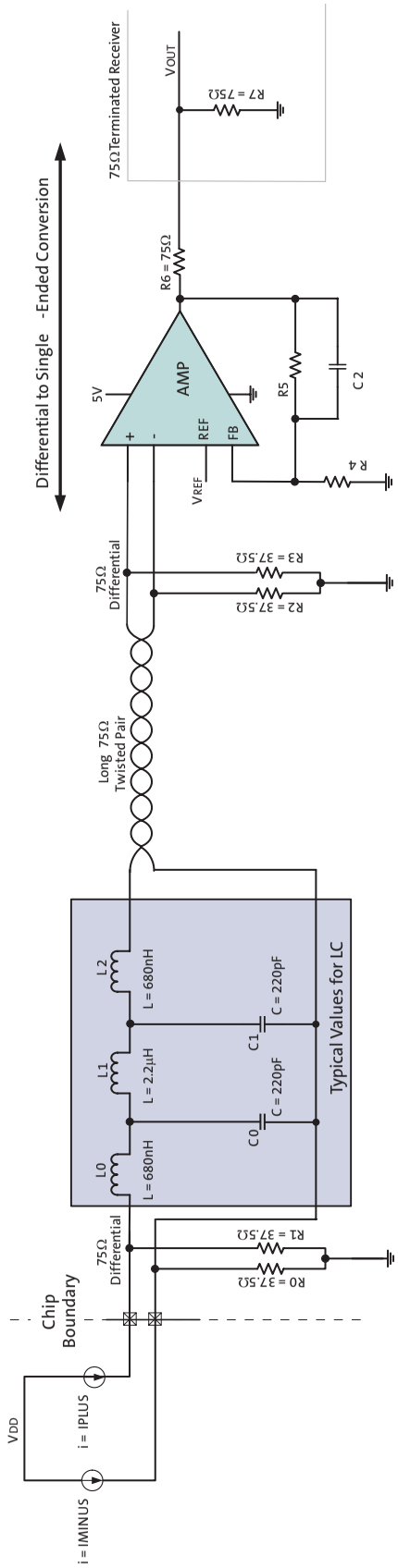


Figure 22: Differential Connection—Grounded Terminations

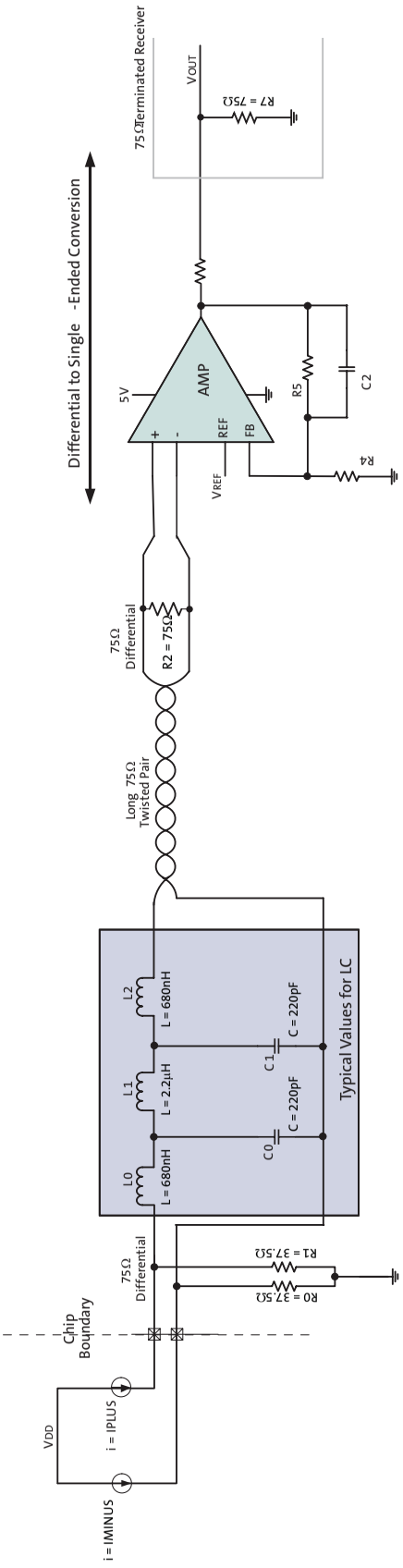


Figure 23: Differential Connection—Floating Termination

Serial (LVDS) Output

The serial high-speed output port supports the interlaced CCIR-656 data format.

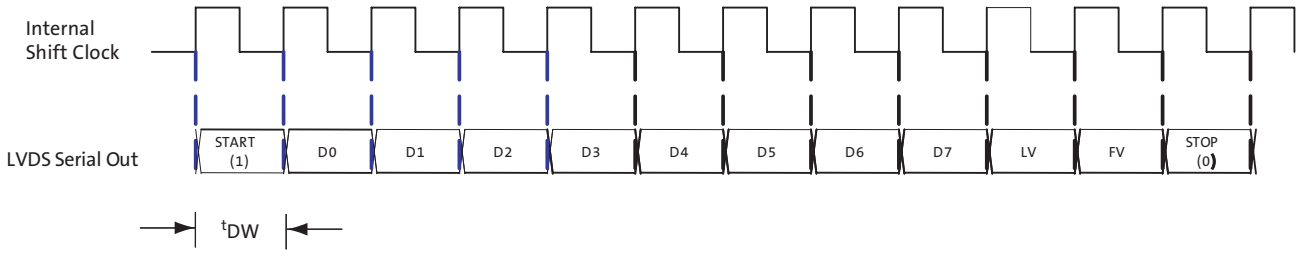
The LVDS port is disabled by default, but can be enabled by the external pin LVDS_ENABLE. This pin must be asserted for LVDS to function. LVDS can be disabled through R0x11D[13]. LVDS is also disabled when STANDBY is asserted.

The output LVDS format is the standard 12-bit package with 10-bit payload format supported by off-the-shelf deserializers, including National (DS92LV1212A), Maxim (MAX9205), and TI (SN65LV1212). An on-chip x12 PLL is included for high-speed LVDS clock generation. LVDS output clock speed is 324 MHz for CCIR support. Table 15 describes the LVDS packet format; Figure 24 on page 102 shows the LVDS data format.

Table 15: LVDS Packet Format

12-Bit Packet	CCIR-656
Bit[0]	1 (START bit)
Bit[1]	PixelData[0]
Bit[2]	PixelData[1]
Bit[3]	PixelData[2]
Bit[4]	PixelData[3]
Bit[5]	PixelData[4]
Bit[6]	PixelData[5]
Bit[7]	PixelData[6]
Bit[8]	PixelData[7]
Bit[9]	LV
Bit[10]	FV
Bit[11]	0 (STOP bit)

Figure 24: LVDS Serial Output Data Format



Notes:
1. Each LVDS packet contains 12 bits. It starts with a "1" (START bit) and ends with a "0" (STOP bit).
2. The 8-bit CCIR656-compliant video data byte is shifted out with the LSB bit out first, following the START bit.
3. The LV and the FV bits are sent out following the video data byte.
4. A 12x PLL generates the internal shift clock from EXTCLK input. The 8-bit DOUT[7:0] is concatenated with LV and FV outputs and shifted out through the differential LVDS_POS/LVDS_NEG outputs.
5. Refer to Table 16 for LVDS data timing.

Table 16: Serial Output Data Timing Values (for EXTCLK = 27 MHz)

Name	Minimum	Typical	Maximum	Units
^{t}DW	2.5	2.7	3.08	ns

Parallel Output (DOUT)

Interlaced

The DOUT[7:0] port supports outputting the interlaced data stream in a variety of formats, as described in more detail in "ITU-R BT.656 and RGB Output" on page 27.

Figure 25 shows the data that is output on the parallel port for CCIR656. Both NTSC and PAL formats are displayed. The blue values in Figure 25 represent NTSC (525/60). The red values represent PAL (625/50).

Figure 25: CCIR656 8-Bit Parallel Interface Format for 525/60 (625/50) Video Systems

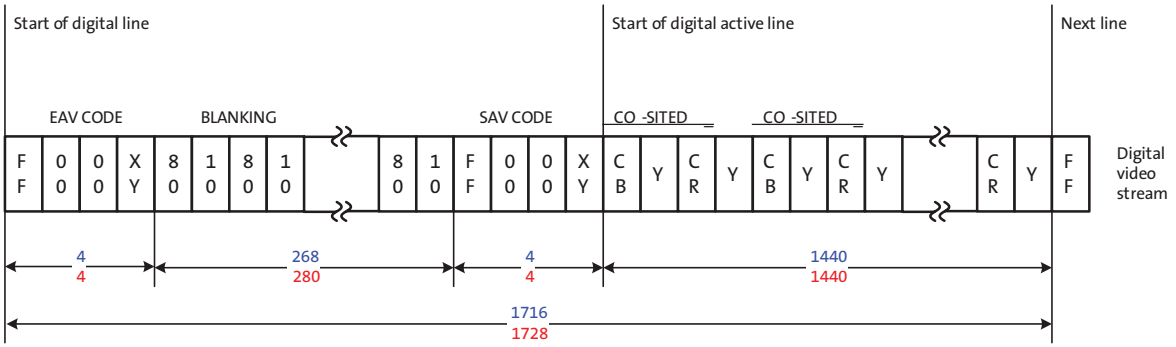


Figure 26 shows detailed vertical blanking information for NTSC timing. See Table 17 on page 104 for data on field, vertical blanking, EAV, and SAV states.

Figure 26: Typical CCIR656 Vertical Blanking Intervals for 525/60 Video System

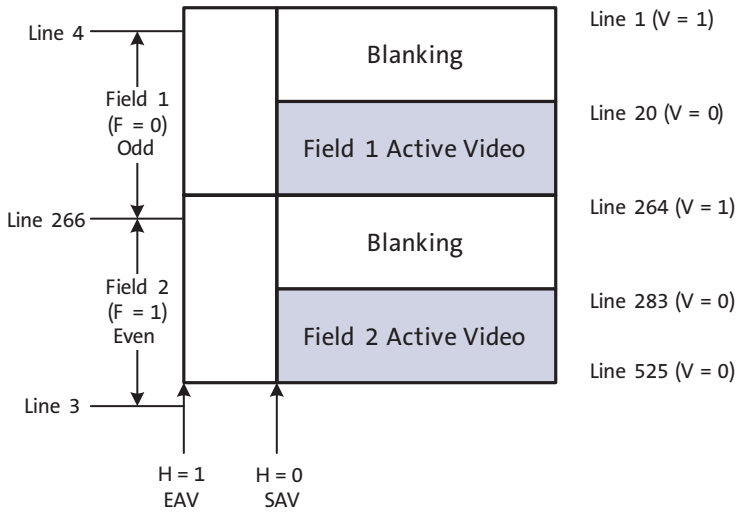


Table 17: Field, Vertical Blanking, EAV, and SAV States

Line Number	F	V	H (EAV)	H (SAV)
1–3	1	1	1	0
4–9	0	1	1	0
20–263	0	0	1	0
264–265	0	1	1	0
266–282	1	1	1	0
283–525	1	0	1	0

Figure 27 shows detailed vertical blanking information for PAL timing. See Table 18 for data on field, vertical blanking, EAV, and SAV states.

Figure 27: Typical CCIR656 Vertical Blanking Intervals for 625/50 Video System

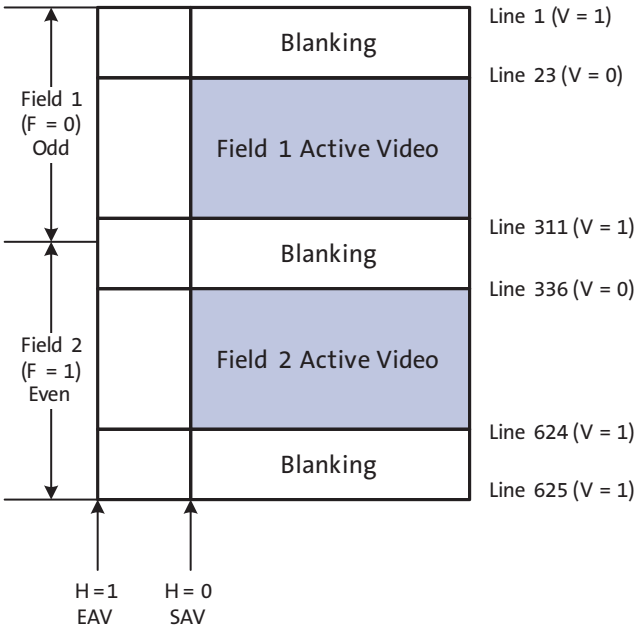


Table 18: Field, Vertical Blanking, EAV, and SAV States

Line Number	F	V	H (EAV)	H (SAV)
1–22	0	1	1	0
23–310	0	0	1	0
311–312	0	1	1	0
313–335	1	1	1	0
336–623	1	0	1	0
624–625	1	1	1	0

Progressive

The DOUT[7:0] port also supports progressive, raw data output. The on-chip color processor does not support reading out the pixel array progressively, but the raw pixel data can be made available in sensor stand-alone mode.

Parallel Input (DIN)

The data-in port allows external CCIR656 data to be multiplexed into the NTSC or PAL output data. Figure 28 shows the timing of the data-in (DIN[7:0]) signals. Table 19 describes timing values for the parallel input waveform. Both mode 0 and mode 1 waveforms are supported by the MT9V135.

Figure 28: Parallel Input Data Timing Waveform

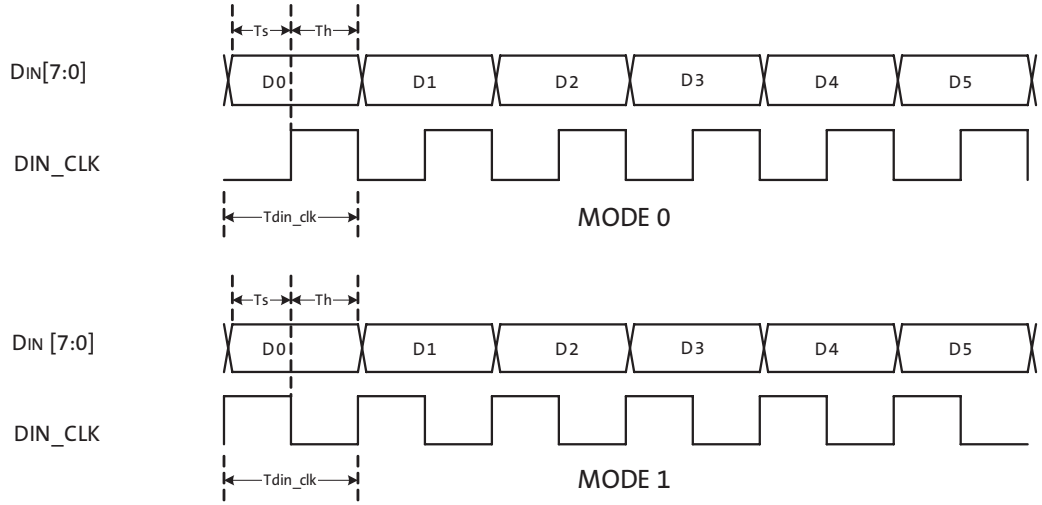


Table 19: Parallel Input Data Timing Values

Name	Min	Typical	Max	Function
Tdin_clk	36.975	37.0	37.025	DIN_CLK Period
Ts	–	18.5	–	DIN Setup Time
Th	–	18.5	–	DIN Hold Time

Notes: 1. The DIN_CLK clock frequency must match the EXTCLK clock frequency. There can be a phase difference between EXTCLK and DIN_CLK, but the frequency must be the same.

Interlaced Modes

True Interlaced

By default, the MT9V135 reads out the image array in a true interlaced fashion where each field maps to the odd and even rows respectively. The color pipe is supplied by a regular Bayer pattern data stream due to the "paired Bayer" CFA filters used with the pixel array, as described in "Pixel Array Structure" on page 14.

Mirroring

The MT9V135 supports both horizontal and vertical flips, regardless of the output format. Horizontal flip, column sequencing reversed, can be enabled by an external pin (HORIZ_FLIP) or a register setting (R0x115[1]). Vertical flip can be controlled through a register setting (R0x020[0]).

Reset, Clocks, and Standby

Reset

Power-up reset is asserted/de-asserted with the RESET_BAR pin, which is active LOW. In the reset state, all control registers are set to default values.

Soft reset is asserted/de-asserted by the two-wire serial interface program. In soft-reset mode, the two-wire serial interface and the register bus are still running. All control registers are reset using default values. See R0x00D.

Clocks

The MT9V135 has three primary clocks:

1. A master clock coming from the EXTCLK signal.
2. A pixel clock using a clock-gated operation running at half frequency of the master clock in sensor stand-alone mode and the same frequency as EXTCLK in SOC mode.
3. DIN_CLK that is associated with the parallel DIN port.

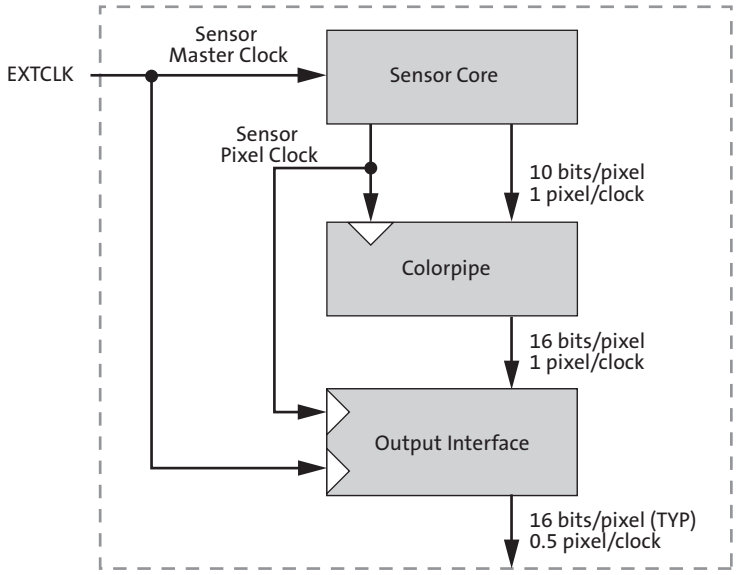
All device clocks are turned off in power-down mode. When the MT9V135 operates in sensor stand-alone mode, the image flow pipeline clocks can be shut off to conserve power. See R0x00D.

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions. The relationship of the primary clocks is depicted in Figure 29 on page 107.

The image flow pipeline typically generates up to 16 bits per pixel—for example, YCbCr or RGB565—but has only an 8-bit port through which to communicate this pixel data.

To generate NTSC or PAL format images, the sensor core requires a 27 MHz clock.

Figure 29: Primary Clock Relationships



Standby Pin

STANDBY is a multipurpose signal that controls three functions: low-power standby, the two-wire serial interface device address, and output signal state functions. Table 20 shows how STANDBY affects the output signal state.

Two-wire serial interface address is based on the SADDR pin XORed with the R0x00D[10]; the R0x00D[10] default is 0. (See Table 31 on page 116 for details). The R0x00D[10] is not writable when STANDBY is asserted "1."

Hard standby is asserted or de-asserted on STANDBY, as described in "Power-Saving Modes" on page 108.

Table 20: STANDBY Effect on the Output State

STANDBY Output Enable R0x00D[6]	Output Disable R0x00D[4]	STANDBY	Output State
0	0	0	Driven
0	0	1	High-Z
1	0	x	Driven
x	1	x	High-Z

Power-Saving Modes

The sensor can be put into the low-power standby state by either of the following mechanisms:

- Asserting STANDBY (provided that R0x00D[7] = 0)
- Setting R0x00D[3:2] = 01 by performing a register write through the serial register interface (R0x00D[2]: analog standby = 1, R0x00D[3]: chip enable = 0)

The two methods are equivalent and have the same effect:

- The source of standby is synchronized and latched. Once latched, the full standby sequence is completed even if the source of standby is removed.
- The readout of the current row is completed.
- Internal clocks are gated off.
- The analog signal chain and associated current and voltage sources are placed in a low-power state.

The standby state is maintained for as long as the standby source remains asserted. The state of the signal interface while in standby state is shown in Table 21.

Table 21: Signal State During Standby

Signal	State
FV	0
LV	0
PIXCLK	1
DOUT[7:0], DOUT_LSB[1:0]	0

While in standby, the state of the internal registers is maintained. The sensor continues to respond to accesses through its serial register interface when STANDBY is asserted through a register write, as described above. The serial register interface does not respond when standby mode is entered by asserting the external STANDBY pin.

An even lower-power standby state can be achieved by stopping the input clock (EXTCLK) while in standby. If the input clock is stopped, the sensor will not respond to accesses through its two-wire serial register interface.

Exit from standby must be through the same mechanism as entry to standby. When the standby source is negated:

1. The internal clocks are restarted.
2. The analog circuitry is restored to its normal operating state.
3. The timing and control circuitry performs a restart, equivalent to writing R0x00D[1] = 1.

After this sequence has completed, normal operation is resumed. If the input clock has been stopped during standby it must be restarted before leaving standby.

Floating Inputs

The following MT9V135 pins cannot be floated:

- DIN[7:0] (tie to GND if not used)
- DIN_CLK (tie to GND if not used)
- PEDESTAL—Valid for NTSC only, this pin should be pulled LOW for PAL
- LVDS ENABLE—This pin must always be pulled HIGH if LVDS is used
- SDATA—This pin is bidirectional and should not be floated

Output Data Ordering

Table 22: Output Data Ordering in DOUT RGB Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
RGB444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGBx444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Note: PIXCLK is 27 MHz when EXTCLK is 27 MHz.

Table 23: Output Data Ordering in Sensor Stand-Alone Mode

Mode	D7	D6	D5	D4	D3	D2	D1	D0	DOUT_LSB1	DOUT_LSB0
10-bit Output	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Note: PIXCLK is 13.5 MHz when EXTCLK is 27 MHz.

Table 24: Data Ordering in LVDS Serial Mode

Mode	Package[0]	Package[8:1]	Package[9]	Package[10]	Package[11]
Default	Start bit 1'b1	DOUT[7:0]	LINE_VALID	FRAME_VALID	Stop bit 1'b0

Note: Data output rate is 324 Mb/s when EXTCLK is 27 MHz.

I/O Timing

Digital Output

By default, the MT9V135 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in Figure 30.

As an option, the polarity of the PIXCLK can be inverted from the default. This is achieved by programming R0x19B[9] to "0."

Figure 30: Digital Output I/O Timing

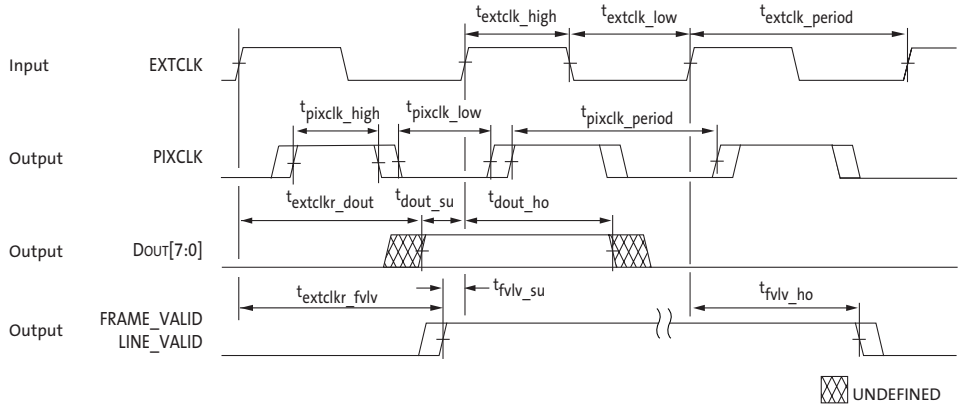
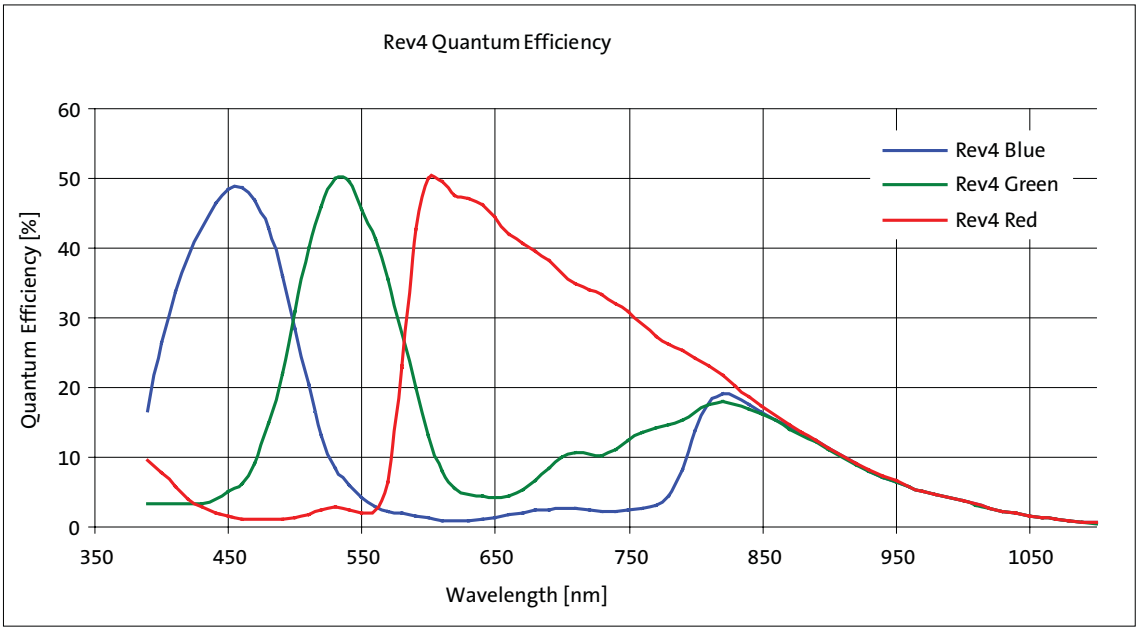


Table 25: Digital Output I/O Timing
T_A = Ambient = 25°C; VDD = 2.5–3.1V

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	t_{extclk_high}		17	–	20	ns
	t_{extclk_low}		17	–	20	ns
	t_{extclk_period}		–	37.0	–	ns
	f_{extclk}	max +/- 100 ppm		27		MHz
PIXCLK[1]	t_{pixclk_low}		14	–	22	ns
	t_{pixclk_high}		14	–	22	ns
	t_{pixclk_period}		36.7	37	37.4	ns
DATA[7:0]	$t_{extclkr\_dout}$		8	14	18	ns
	t_{dout_su}		14	18.5	23	ns
	t_{dout_ho}		14	18.5	23	ns
FV/LV	$t_{extclkr\_fvlv}$		8	14	18	ns
	t_{fvlv_su}		14	18.5	23	ns
	t_{fvlv_ho}		14	18.5	23	ns

Note: PIXCLK may be inverted by programming register R0x19B[9] = 0.

Figure 31: Spectral Characteristics



Electrical Specifications

Table 26: Electrical Characteristics and Operating Conditions
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter[1]	Condition	Min	Typ	Max	Unit
I/O and core digital voltage (V_{DD})	–	2.5	2.8	3.1	V
LVDS PLL voltage	–	2.5	2.8	3.1	V
Video DAC voltage	–	2.5	2.8	3.1	V
Analog voltage (V_{AA})	–	2.5	2.8	3.1	V
Pixel supply voltage (V_{AAPIX})	–	2.5	2.8	3.1	V
Leakage current	STANDBY, EXTCLK: HIGH or LOW			10	µA
Imager operating temperature	–	–40		+85	°C
Storage temperature	–	–40		+125	°C

Notes:
1. V_{DD}, V_{AA}, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.
2. Customers requiring a similar part with greater temperature range should consider using the MT9V125.

Table 27: Video DAC Electrical Characteristics
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter	Condition	Min	Typ	Max	Unit
Resolution		–	10	–	bits
DNL	Single-ended mode	–	0.8	1.1	bits
INL	Single-ended mode	–	5.7	8.1	bits
Output local load	Single-ended mode, output pad (DAC_POS)	–	75	–	Ω
	Single-ended mode, unused output (DAC_NEG)	–	0	–	Ω
Output voltage	Single-ended mode, code 000h	–	0.02	–	V
	Single-ended mode, code 3FFh	–	1.42	–	V
Output current	Single-ended mode, code 000h	–	0.6	–	mA
	Single-ended mode, code 3FFh	–	37.9	–	mA
DNL	Differential mode	–	0.7	1	bits
INL	Differential mode	–	1.4	3	bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω
Output voltage	Differential mode, code 000h, pad dacp	–	0.37	–	V
	Differential mode, code 000h, pad dacn	–	1.07	–	V
	Differential mode, code 3FFh, pad dacp	–	1.07	–	V
	Differential mode, code 3FFH, pad dacn	–	0.37	–	V
Output voltage	Differential mode, code 000h, pad dacp	–	0.6	–	mA
	Differential mode, code 000h, pad dacn	–	37.9	–	mA
	Differential mode, code 3FFh, pad dacp	–	37.9	–	mA
	Differential mode, code 3FFH, pad dacn	–	0.6	–	mA
Differential output, mid level	Differential mode	–	0.72	–	V
Supply current	Estimate	–	–	55	mA

Table 28: Digital I/O Parameters
T_A = Ambient = 25°C; All supplies at 2.8V

Signal	Parameter	Definitions	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		1	–	30	pF
		Output signal slew	2.8V, 30pF load	–	0.72	–	V/ns
			2.8V, 5pF load	–	1.25	–	V/ns
	V_{OH}	Output high voltage		2.5	2.8	3.1	V
	V_{OL}	Output low voltage		–0.3	–	0.3	V
	I_{OH}	Output high current	V_{DD} = 2.8V, V_{OH} = 2.4V	16	–	26.5	mA
	I_{OL}	Output low current	V_{DD} = 2.8V, V_{OL} = 0.4V	15.9	–	21.3	mA
All Inputs	V_{IH}	Input high voltage	V_{DD} = 2.8V	1.48	–	–	V
	V_{IL}	Input low voltage	V_{DD} = 2.8V	–	–	1.43	V
	I_{IN}	Input leakage current		–2	–	2	µA
	Signal CAP	Input signal capacitance		–	3.5	–	pF

Power Consumption

Table 29: Power Consumption
T_A = Ambient = 25°C; All supplies at 2.8V

Mode	Sensor (mW)	Image-Flow Proc (mW)	I/Os (mW)[1]	DAC (mW)	LVDS (mW)	Total (mW)
Active mode [2]	60	100	10	150	80	400
Standby						0.56

Notes: 1. 10pF nominal.
2. (NTSC or PAL) and LVDS should not be operated at the same time.

NTSC Signal Parameters

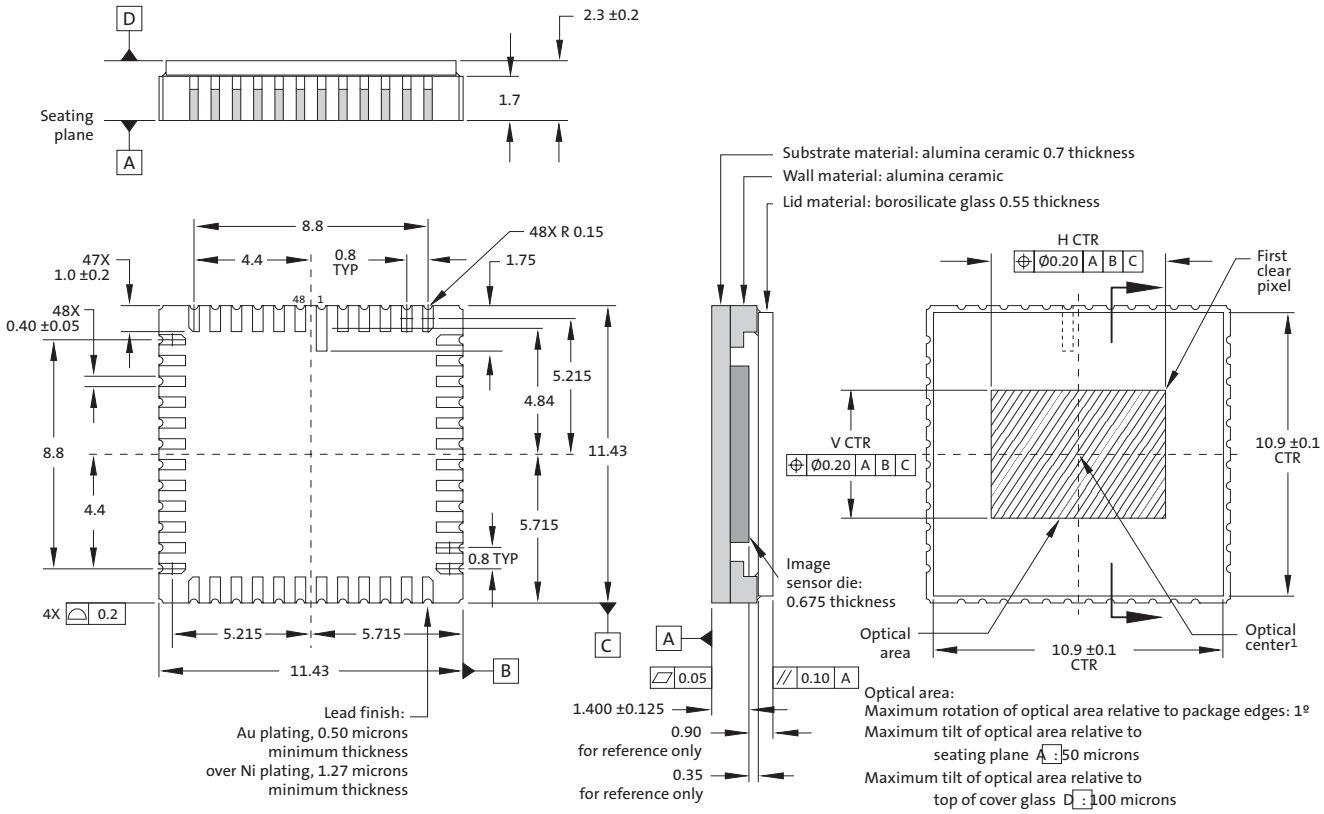
Table 30: NTSC Signal Parameters
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Line Frequency		15730	15735	15740	Hz	
Field Frequency		59.00	59.94	60.00	Hz	
Sync Rise Time		120	164	170	ns	
Sync Fall Time		120	167	170	ns	
Sync Width		4.60	4.74	4.80	?S	
Sync Level		37	39.9	43	IRE	2, 4
Burst Level		37	39.7	43	IRE	2, 4
Sync to Setup (with pedestal off)		9.10	9.40	9.40	µS	
Sync to Burst Start		5.00	5.31	5.60	µS	
Front Porch		1.40	1.40	1.60	µS	
Burst Width		8.0	8.5	10.0	cycles	
Black Level		6.5	7.5	8.5	IRE	1, 2, 4
White Level		90	100	110	IRE	1, 2, 3, 4

Notes:
1. Black and white levels are referenced to the blanking level.
2. NTSC convention standardized by the IRE (1 IRE = 7.14mV).
3. Encoder contrast setting R0x011 = R0x001 = 0.
4. DAC ref = 2.8kΩ, load = 37.5Ω

Package and Die Dimensions

Figure 32: 48-Pin CLCC Package Drawing



Notes:
1. Optical center = package center.
2. All dimensions in millimeters.

Appendix A: Serial Bus Description

Registers are written to and read from the MT9V135 through the two-wire serial interface bus. The sensor is a serial interface slave controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred in and out of the MT9V135 through the serial data (SDATA) line. The SDATA and SCLK lines are pulled up to VDD off-chip by a 1.5KΩ resistor. Either the slave or the master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- an acknowledge bit
- a no-acknowledge bit
- an 8-bit message
- a stop bit
- the slave device 8-bit address

The SADDR pin and R0x00D[10] are used to select between two different addresses in case of conflict with another device. If SADDR XOR R0x00D[10] is LOW, the slave address is 0x90; if SADDR XOR R0x00D[10] is HIGH, the slave address is 0xBA. See Table 31 below.

Table 31: Two-Wire Interface ID Address Switching

SADDR	R0x00D[10]	Two-Wire Interface Address ID
0	0	0x90
0	1	0xBA
1	0	0xBA
1	1	0x90

Sequence

A typical read or write sequence begins with the master sending a start bit. After the start bit, the master sends the 8-bit slave device address. The last bit of the address determines if the request is a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master transfers the 8-bit register address for where a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data, 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits.

The MT9V135 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. The master sends the write mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master clocks out the register data, 8 bits

at a time and sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and one bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xBA; the read address is 0xBB. This applies only when the SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing or the slave when reading) releases the data line, and the receiver signals an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

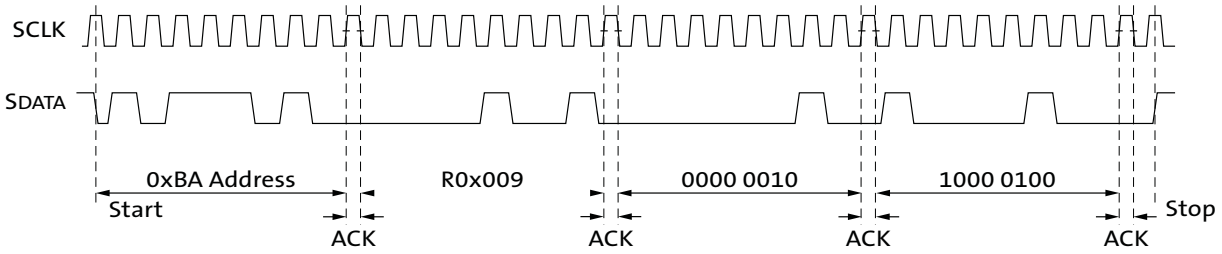
Two-Wire Serial Interface Sample

Write and read sequences (SADDR = 1).

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 33. A start bit sent by the master starts the sequence, followed by the write address. The image sensor sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

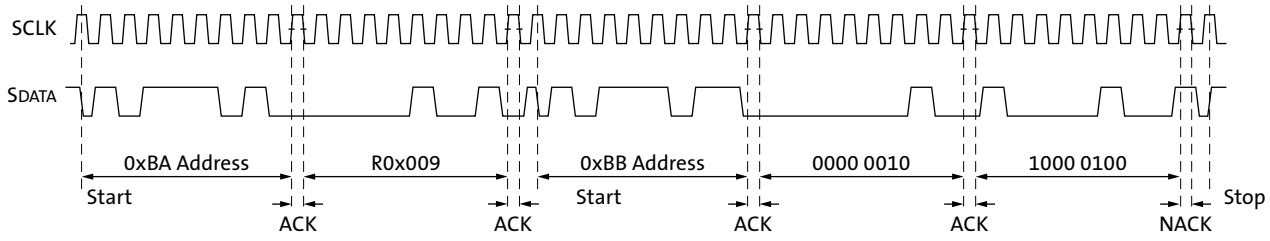
Figure 33: WRITE Timing to R0x009—Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 34. The master writes the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to occur from the register. The master then clocks out the register data, 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

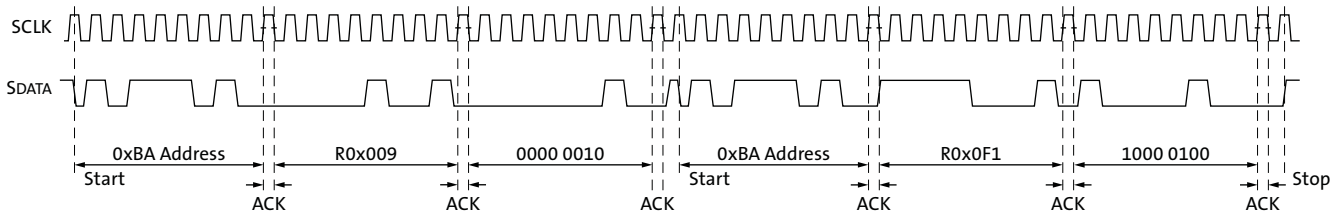
Figure 34: READ Timing From R0x009; Returned Value 0x0284



8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is started by writing the upper 8 bits to the desired register, then writing the lower eight bits to the special register address (R0x0F1). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. In Figure 35 on page 119, a typical sequence for an 8-bit WRITE is shown. The second byte is written to the special register (R0x0F1).

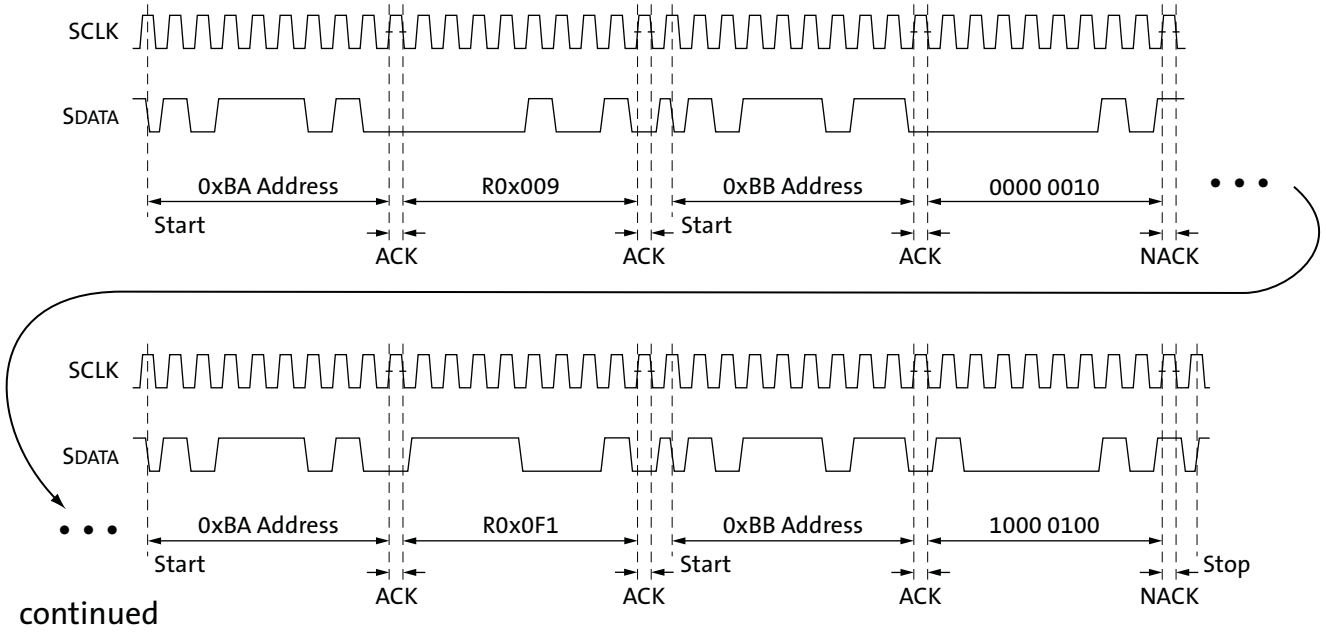
Figure 35: WRITE Timing to R0x009—Value 0x0284



8-Bit READ Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0x0F1), the lower 8 bits are accessed (Figure 36). The master sets the no-acknowledge bits.

Figure 36: READ Timing From R0x009; Returned Value 0x0284



Two-Wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified below in master clock cycles.

Figure 37: Serial Host Clock Period and Duty Cycle

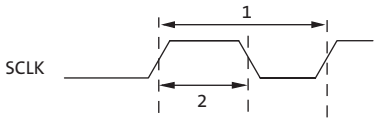


Figure 38: Serial Host Interface Start Condition Timing

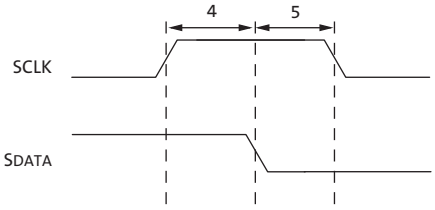
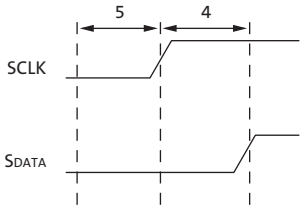
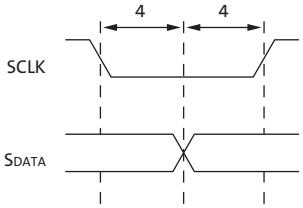


Figure 39: Serial Host Interface Stop Condition Timing



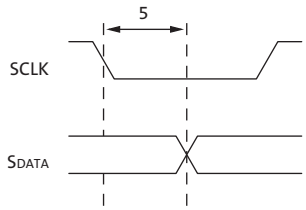
Note: All timing are in units of master clock cycle.

Figure 40: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 41: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 42: Acknowledge Signal Timing After an 8-bit Write to the Sensor

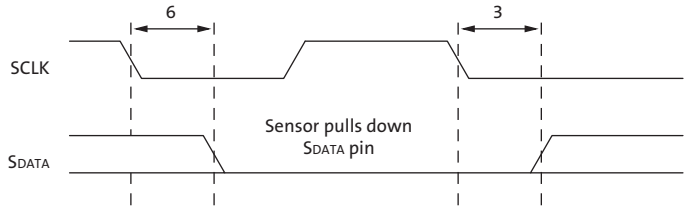
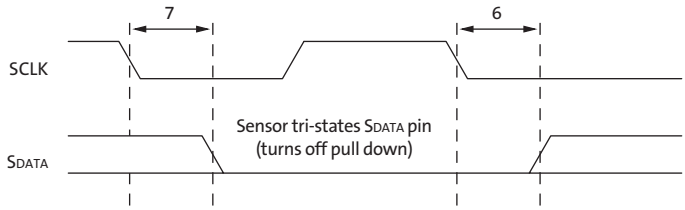


Figure 43: Acknowledge Signal Timing After an 8-bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Revision History

Rev. E 11/12/10

- Applied updated Aptina template

Rev. D 6/21/10

- Updated to non-confidential

Rev. C 5/6/10

- Updated to Aptina template
- Updated to Production status
- Updated Table 1, “Ordering Information,” on page 1
- Updated titles for Figure 4 on page 11 and Figure 32 on page 115 to say 48-pin instead of 44-pin

Rev. B 3/1/07

- Updated Figure 32: 48-Pin CLCC Package Drawing on page 115
- Converted decimal register numbers to hexadecimal

Rev. A 9/06

- Initial release