

# Technical Note

## Signal Integrity Considerations for Module Design

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### Introduction

To assist our customers with the module layout process, this technical note describes layout best practices for mobile imaging module design. A list of recommendations is also provided to assist with design decisions in the layout process.

A few fundamental signal integrity (SI) concepts are presented in order to understand the background for the design recommendations that are offered. This is by no means an exhaustive description of a complex subject, but offered to help the module designers in understanding the reasoning for the design guidelines.

### Signal Integrity and EMI

Electromagnetic interference (EMI) is defined as unwanted, conducted, or radiated signals of electronic origin that can cause degradation of system performance, while signal integrity refers to methods that ensure electrical signals are of sufficient quality for proper operation. Examples that affect signal integrity include crosstalk, ringing, ground bounce, and power supply noise. Failure to plan for induced noise can cause the final design to work incorrectly, affect image quality, force redesigns, and lower yield.

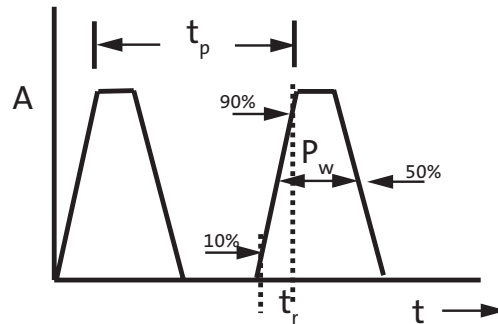
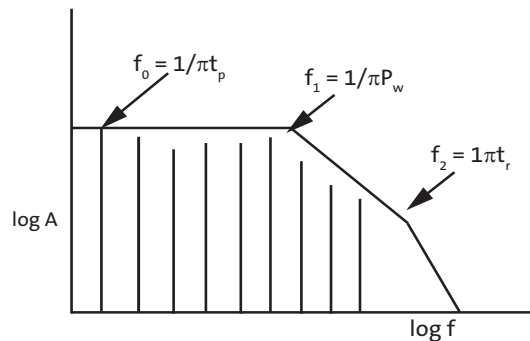
Although we are not specifically discussing EMI in this technical note, techniques to reduce SI will often result in lowering overall system EMI.

The next sections provide details about signal integrity and EMI:

- “Frequency and Time Domain Relationship” on page 1
- “Inductance, Mutual Inductance, and Mutual Capacitance” on page 2
- “Thermal Considerations” on page 4

### Frequency and Time Domain Relationship

The first concept is that a digital waveform observed in the time domain is a combination of a sum of multiple harmonics in the frequency domain (see Figures 1 and 2 on page 2). Nonsinusoidal signals can be described as a combination of multiple sinusoidal frequencies of various amplitudes. One must think of each frequency traveling down the signal path individually and how that signal might be affected by the RLC effects of the signal path and then the sum of all of the frequencies are combined at the endpoint. The result of combining all of the individual frequencies is that if every frequency of concern is unaffected by the signal path, then one would have the same waveform at the endpoint as in the beginning. If any particular frequency is affected by the signal path, then the overall signal becomes distorted. If the resulting waveform is highly distorted, this could affect the proper operation of your system.

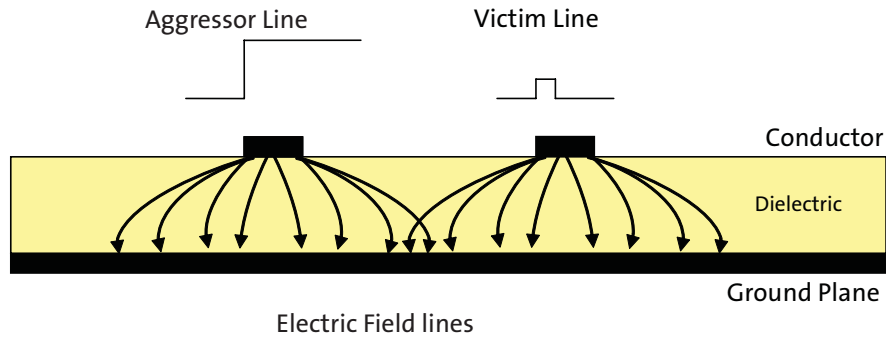
**Figure 1: Time Domain of a Trapezoidal Pulse**

**Figure 2: Frequency Domain of a Trapezoidal Pulse**


In trying to determine the bandwidth of interest of a particular signal, one must typically focus on the fast rise and fall times of the signals involved. If one observes a clock square wave, with a rise time of  $t_r$ , one could use a basic rule of thumb that the bandwidth involved in the frequency domain would be in Figure 2. For example, a digital waveform with a 500ps rise time would generate frequencies of interest to 636 MHz. A slower rise time will generate less high frequency signals and overall magnitudes will decrease. This is the reason to utilize slew rate control where possible. Slew rate control also reduces EMI.

## Inductance, Mutual Inductance, and Mutual Capacitance

Capacitive coupling of two electric fields occurs when current is injected in the victim line proportionally to the  $dV/dT$  of the aggressor line. This is one form of crosstalk. Figure 3 shows how the electric field would interact such that the signal appearing on the aggressor line appears on the victim line.

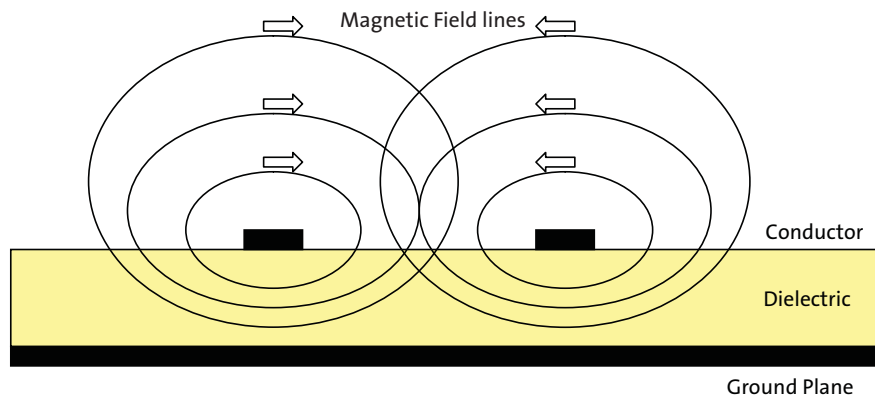
Figure 3: Self and Mutual Capacitance



Self-inductance can be described as the ratio of the magnetic flux produced from a current through a conductive path. The current produces a magnetic field that stores energy. However, magnetic fields in other nearby wires or structures will couple energy and interact with each other. This is another form of crosstalk.

Figure 4 provides a visual example of how the magnetic fields would interact. If the two traces are brought physically closer together, then the magnetic field lines begin to interact with each other.

Figure 4: Self and Mutual Inductance



The effect of the adjacent inductive coupling depends upon the direction the adjacent current is flowing. If we imagine a high frequency signal traveling in a wire loop, we can describe the effective inductance that the signal will 'see' as

$$L_{eff} = L1 + L2 \pm 2M$$

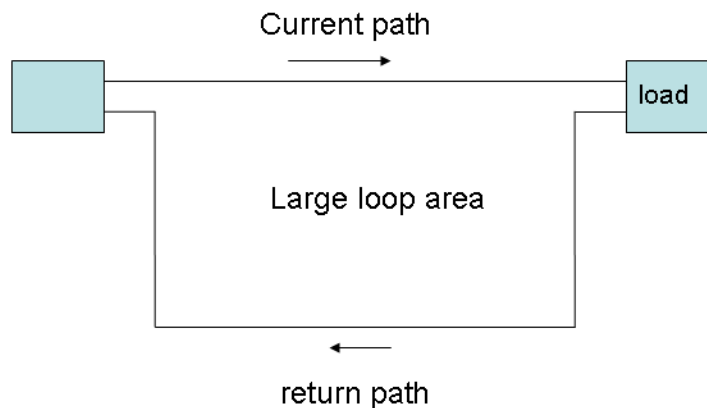
where M describes the mutual inductance, which is a coupling factor between the conductors.

The +/-M will be '+' for currents going in the same direction and '-' for currents going in the opposite direction. Figure 4 shows the direction of the fields when current is flowing such that the current is flowing into the left conductor and returning on the right conductor in a loop. In this case, the mutual inductance would be subtractive to give an overall lower effective inductance of the current path.

We can use mutual inductance to our benefit to reduce the overall effective inductance of the current path. We do this by bringing the return path of the current as close as possible to the source current. Conversely, if currents are going in the same direction, this would increase the effective inductance. In this case, one would want to utilize techniques to minimize the interaction between signals.

We now have a description for a “current loop.” A current loop describes the path the current takes from the source and back to its origin (see Figure 5). The goal is to make the current loop as small as possible.

Figure 5: Current Loop



If one gets a lower effective inductance when the current return path is as close to the signal wire as possible, then using a power/ground plane under the signal wire can reduce the loop area. Also, for signals going in the same direction, the effective inductance would be higher, so one would want to separate them by a distance, if possible. Therefore, one must think about the current loop area and keeping that as small as possible in the layout. Designs with small loop areas have lower EMI.

Currents will follow the path of least impedance. Resistive effects dominate at low frequencies. L and C effects dominate at high frequencies.

## Thermal Considerations

Module layout can have a major impact on the noise levels of the final product because of the elevation of the module temperature. It is imperative to integrate proper thermal management strategies in the system design to prevent degradation of image quality.

## Module Layout Best Practices

The following sections provide design guidelines and considerations regarding various areas of the layout.

- “General Guidelines” on page 5
- “Clocks and High-Speed Traces” on page 5
- “Power Supply” on page 6
- “Power Supply Decoupling and Bypassing” on page 6
- “General Capacitor Guidelines” on page 7
- “Decoupling Capacitor Recommendations” on page 9

## General Guidelines

The following list provides design guidelines and considerations regarding various areas of the layout. We realize that most designs cannot conform to all of these rules because of size and other constraints. The information in the list is presented such that the layout designer can think about the tradeoffs during the design process.

- Follow Aptina data sheet and developer guide for information to correctly terminate unused pins.
- To lower inductance and minimize crosstalk, use multilayer boards with a solid power and ground plane.
- If a solid plane is not possible, consider minimizing the overall inductance of the current return path.
- All high-frequency signals should flow over a solid ground plane related to the signal to minimize the current return loop.
- When using flex cables, use a return path under the signal traces where possible.
- For external connections, place all the connectors that will go to the same destination board close to each other to avoid large current return loop.
- Use ground plane under traces to minimize crosstalk (for example, on flex between sensor and connector, a thin lamination under traces is better than a thick one).
- Route signal traces over their respective power/ground return paths. This means digital areas over digital ground, and analog portions over analog ground.
- Differential traces should be adjacent and matched physically.
- Use VIAs carefully. VIAs represent discontinuity in the signal path.
- Use additional ground pads to isolate signals and to allow for short return paths.
- Separate digital and analog grounds.

One must also keep in mind the design trade-off between electrical and thermal requirements. Design rules to optimize signal integrity can often negatively affect thermal performance of the system. Verify that there is a sufficient thermal path to reduce the die operating temperature that would otherwise affect image quality.

## Clocks and High-Speed Traces

- Widen spacing between HS signal lines as routing restrictions allow extra space, especially on the clock inputs.
- Keep high speed (that is, fast  $t_p$ ,  $t_f$ ) signals away from the clock lines.
- Shield the clock with grounded adjacent traces.
- Keep clock traces as straight and short as possible.
- Discontinuities on a transmission path will degrade a signal. Do not use sharp 90-degree bends. Mitered 45-degree bends are preferred.
- Keep clock signals on a single layer.

- Turn on slew rate control, if available, to slow down fast edges when speed is not critical to minimize simultaneous pad switching currents and ground bounce and minimize over- and undershoot due to pulse reflections from the load.
- If necessary, use proper terminations to reduce potential reflections and ringing on fast signals.
- Limit high frequency signals as much as possible.
- Avoid VIAs, which can cause impedance changes and reflections.

## Power Supply

- Use solid plane layers to distribute power.
- Shared power distributions can increase crosstalk between physical areas. For more information about crosstalk, see “Inductance, Mutual Inductance, and Mutual Capacitance” on page 2.
- Make traces related to power and ground as short and wide as possible to reduce the potential for supply sag and ground bounce effects.
- Consider trace inductance and mutual coupling when designing power distribution.
- Pair respective power supply lines and areas.
- Position for a low inductance power and ground trace.
- Space power and ground pads to allow for required bypass capacitors.
- Maintain as much plane structure and connectivity as possible. Try not to tear up the ground planes with too many holes and cuts.
- Minimize the spacing between planes to increase coupling and create built in capacitance.
- Do not share VIAs.
- Provide sufficient power and ground connections.
- Connect each ground pad or VIA to the ground and power planes individually. Avoid daisy-chaining connections.
- Bond wires typically add 1nH/mil for 1mil gold wire. Bond wires can be responsible for a significant amount of parasitic effects. For example, a 1mil diameter gold wire can typically add 1nH/mil of self inductance.

## Power Supply Decoupling and Bypassing

Bypassing is used for reducing the high frequency current flow by shunting and reducing the noise current to ground. Proper bypassing is required for decoupling. The bypassing path must provide significantly lower impedance at the frequency of interest than the power supply leads.

The goal of decoupling is to prevent the transmission of noise from one part of the circuit to another by providing isolation between the two circuits to ensure proper operation.

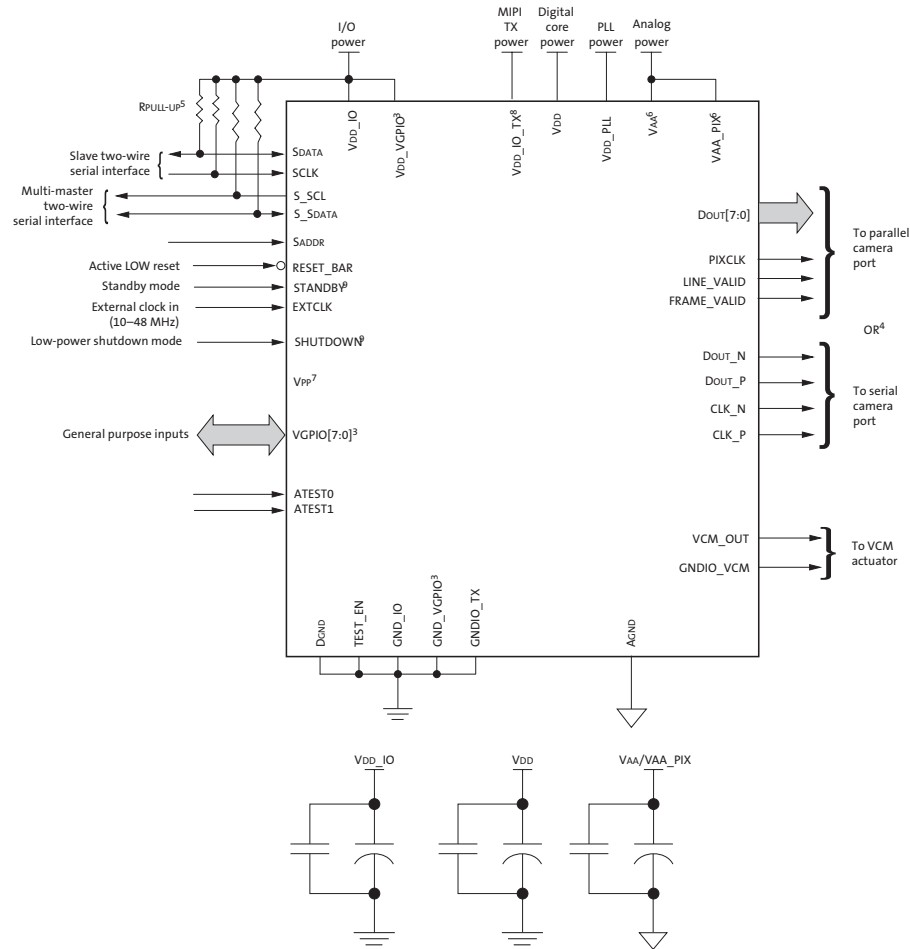
Decoupling and bypassing typically involve using capacitors tied to ground, or other trace signals to reduce noise levels.

## General Capacitor Guidelines

- The minimum decoupling capacitor must be able to supply the current required during worst-case switching conditions. Use  $C(dV) = di/dt$  to calculate the required capacitor sizes.
- In a real system with parasitic effects, the circuit will consist of multiple RLC components.
- Use surface mount low effective series resistance (ESR) capacitors to minimize lead inductance over a high range of frequencies.
- Multiple capacitors on a supply makes it easier for physical distribution by lowering effective inductance and ESR. However, if one uses multiple capacitors, be aware that a frequency resonant pole can be created between the values used.
- Mount the capacitor as close as possible to the sensor power and ground pads.
- Place the smaller, high frequency capacitors nearer to the sensor pads to provide a shorter path for fast transient currents.
- Use large, multiple VIAs from the capacitors to the power planes to minimize R and L while allowing for maximum current flow.
- Use wide, short traces between VIAs and capacitor pads, or adjacent to the pad.
- A real world capacitor is not just a bulk capacitor, but can be modeled as a RLC in series. Be aware of the frequency characteristics of the components used.
- Verify that the temperature characteristics of the capacitors used will be suitable for the system operating environment. The characteristics of the capacitors can be significantly degraded at higher temperatures.

## Current Aptina Recommendations

Figure 6: Typical Connection for the MT9P111



- Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor. The minimum recommended decoupling configuration is 0.1μF per supply on module and 10μF off module.
  2. If a MIPI interface is not required, the following pads must be left floating: DOUT\_P, DOUT\_N, CLK\_P, and CLK\_N.
  3. The VGPIO pads can serve multiple features that can be reconfigured. The function and direction will vary by applications. If VGPIO pads are not required, the VDD\_VGPIO, GND\_VGPIO, and VGPIO[7:0] pads can be left floating.
  4. Only one of the output modes (serial or parallel) can be used at any time.
  5. Aptina recommends a resistor value of 1.5KΩ to VDD\_IO for the two-wire serial interface Rpull-up; however, greater values may be used for slower transmission speeds.
  6. VAA and VAA\_PIX must be tied together.
  7. VPP is the one-time programmable (OTP) memory programming voltage and should be left floating during normal operation.
  8. VDDIO\_TX can be connected to VDD\_IO if VDD\_IO = 2.8V. Otherwise, VDDIO\_TX can be tied to the VAA supply if an Aptina recommended decoupling capacitor is used. VDDIO\_TX must be connected to a 2.8V supply.
  9. If STANDBY and SHUTDOWN pins are not used, they must be connected to DGND.



## Decoupling Capacitor Recommendations

It is important to provide clean, well-regulated power to each power supply. The customer is ultimately responsible for ensuring that clean power is provided for their own designs because hardware design is influenced by many factors, including layout, operating conditions, and component selection.

The recommendations for capacitor placement and values listed below are based on the Aptina internal demo camera design and verified in hardware.

Aptina recommends the following, in order of preference:

1. Mount 0.1 $\mu$ F and 1 $\mu$ F decoupling capacitors for each power supply as close as possible to the pad and place a 10 $\mu$ F capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design (VDD\_PLL tied to VAA), use a 0.1 $\mu$ F and 1 $\mu$ F capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 $\mu$ F capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, use a 1 $\mu$ F capacitor (preferred) or a 0.1 $\mu$ F capacitor for each of the three regulated supplies. Aptina also recommends placing a 10 $\mu$ F capacitor for each supply off-module but close to each supply.
4. Give priority to the VAA supply for additional decoupling capacitors.

Aptina does not recommend inductive filtering components.

## Summary

We have presented some general module layout guidelines for our customers to consider and have touched upon a few of the concepts of signal integrity to help familiarize our customers with the basis of those rules.

Schematic and layout reviews are available for Aptina customers. Contact your Aptina representative for information regarding customer schematic and layout reviews.

## Additional Resources

See TN-09-49 Connecting Bypass Capacitors to MT9M112 for more information.

## Revision History

<b>Rev. C</b> .....		<b>8/10</b>
	<ul style="list-style-type: none"> <li>• Updated to Aptina template</li> <li>• Updated to non-confidential</li> </ul>	
<b>Rev. B</b> .....		<b>12/08</b>
	<ul style="list-style-type: none"> <li>• Demoted the following sections to show subordinate relationship to “Signal Integrity and EMI” on page 1               <ul style="list-style-type: none"> <li>– “Frequency and Time Domain Relationship” on page 1</li> <li>– “Inductance, Mutual Inductance, and Mutual Capacitance” on page 2</li> <li>– “Thermal Considerations” on page 4</li> </ul> </li> <li>• Added bullet list to provide cross-references to subordinate headings in “Signal Integrity and EMI” on page 1</li> <li>• Promoted “Module Layout Best Practices” on page 5 to a major heading</li> <li>• Demoted the following sections to show subordinate relationship to “Module Layout Best Practices” on page 5               <ul style="list-style-type: none"> <li>– “General Guidelines” on page 5</li> <li>– “Clocks and High-Speed Traces” on page 5</li> <li>– “Power Supply” on page 6</li> <li>– “Power Supply Decoupling and Bypassing” on page 6</li> <li>– “General Capacitor Guidelines” on page 7</li> </ul> </li> <li>• Added “Decoupling Capacitor Recommendations” on page 9.</li> <li>• Removed TN-00-06 Bypass Capacitor doc from “Additional Resources” on page 9.</li> <li>• Updated Figure 6: “Typical Connection for the MT9P111,” on page 8</li> </ul>	
<b>Rev. A</b> .....		<b>9/07</b>
	<ul style="list-style-type: none"> <li>• Initial release</li> </ul>	