Technical Note

Signal Integrity Considerations for Module Design

Introduction

To assist our customers with the module layout process, this application note describes layout best practices for mobile imaging module design. A list of recommendations are also provided to assist with design decisions in the layout process.

A few fundamental signal integrity (SI) concepts are presented in order to understand the background for the design recommendations that are offered. This is by no means an exhaustive description of a complex subject, but offered to help the module designers in understanding the reasoning for the design guidelines

Signal Integrity and EMI

Electromagnetic interference (EMI) is defined as unwanted, conducted or radiated signals of electronic origin that can cause degradation of system performance. While signal integrity refers to methods that ensure electrical signals are of sufficient quality for proper operation. Examples that affect signal integrity include crosstalk, ringing, ground bounce, and power supply noise. Failure to plan for induced noise can cause the final design to work incorrectly, affect image quality, force redesigns, and lower yield.

Although we are not specifically discussing EMI in this application note, techniques to reduce SI will often result in lowering overall system EMI.

Frequency and Time Domain Relationship

The first concept is that a digital waveform observed in the time domain is a combination of a sum of multiple harmonics in the frequency domain. Nonsinusoidal signals can be described as a combination of multiple sinusoidal frequencies of various amplitudes. One must think of each frequency traveling down the signal path individually and how that signal may be affected by the RLC effects of the signal path and then the sum of all of the frequencies will be combined at the endpoint. The result of this is that if every frequency is unaffected by the signal path, then one would have the same waveform at the endpoint as in the beginning. If any particular frequency is affected by the signal path, then the overall signal will become distorted. If this distortion is severe, this may affect the proper operation of your system.

Figure 1: Time Domain of a Trapezoidal Pulse

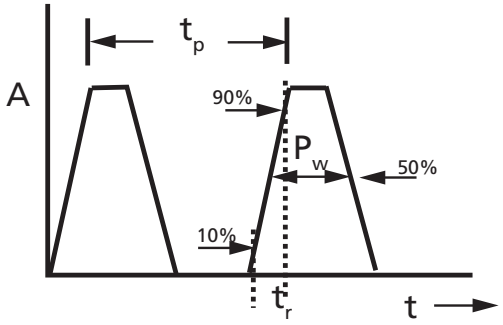
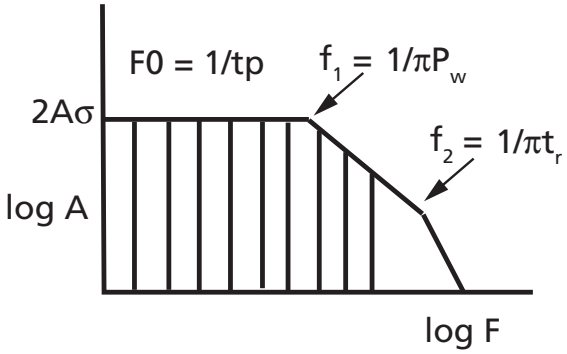


Figure 2: Frequency Domain of a Trapezoidal Pulse

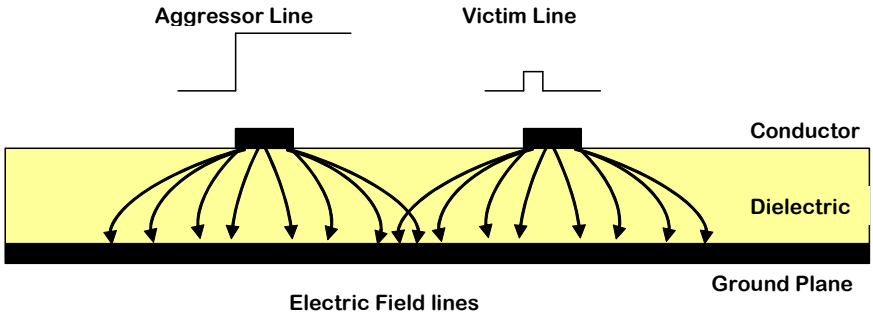


In trying to determine the bandwidth of interest of a particular signal, one must typically focus on the fast rise and fall times of the signals involved. If one observes a clock square wave, with a rise time of Tr, one could use a basic rule of thumb that the bandwidth involved in the frequency domain would be in Figure 2. For example, a digital waveform with a 500ps rise time would generate frequencies of interest to 636 MHz. So, slower rise times will generate less high frequency signals and overall magnitudes will decrease. This is the reason to utilize slew rate control where possible. Slew rate control also reduces EMI.

Inductance, Mutual Inductance, and Mutual Capacitance

Capacitive coupling of two electric fields occur when current is injected in the victim line proportionally to the dV/dT of the aggressor line causes waves to appear on the victim trace. This is one form of crosstalk. Figure 3 illustrates visually how the electric field would interact such that the signal appearing on the aggressor line would show up on the victim line.

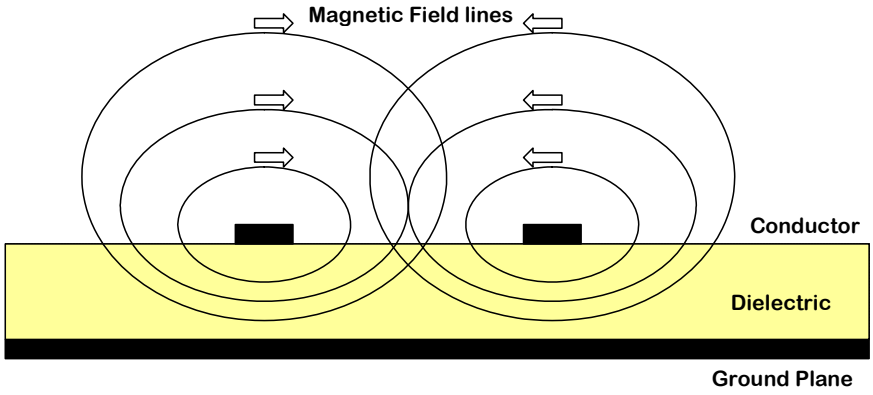
Figure 3: Self and Mutual Capacitance



Self-inductance can be described as the ratio of the magnetic flux produced from a current through a conductive path. The current produces a magnetic field that stores energy. However, magnetic fields in other nearby wires or structures will couple energy and interact with each other. This is another form of crosstalk.

Figure 4 gives a visual feel of how the magnetic fields would interact. If the two traces are brought physically closer together, then the magnetic field lines would begin interacting with each other.

Figure 4: Self and Mutual Inductance



The effect of the adjacent inductive coupling depends upon the direction the adjacent current is flowing. If we imagine a high frequency signal traveling in a wire loop, we can describe the effective inductance that the signal will 'see' as

$Leff = L1 + L2 \ +/- \ 2M$

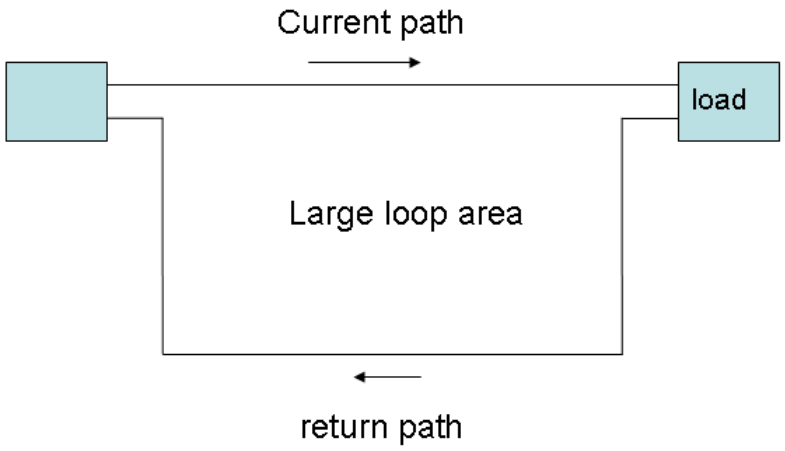
where M describes the mutual inductance, a coupling factor between the conductors.

The +/-M will be '+' for currents going in the same direction and '-' for currents going in the opposite direction. Figure 4 shows the direction of the fields when current is flowing such that the current is flowing into the left conductor and returning on the right conductor in a loop. In this case, the mutual inductance would be subtractive to give an overall lower effective inductance of the current path.

So, we can use mutual inductance to our benefit to reduce the overall effective inductance of the current path. We do this by bringing the return path of the current as close as possible to the source current. Conversely, if currents are going in the same direction, this would increase the effective inductance. In this case, one would want to utilize techniques to minimize the interaction between signals.

We now have a description for a "current loop." A current loop describes the path the current takes from the source and back to its origin. The goal is to make the current loop as small as possible.

Figure 5:



So, if one gets a lower effective inductance when the current return path is as close to the signal wire as possible, then using a power/ground plane under the signal wire can reduce the loop area. Also, for signals going in the same direction, the effective inductance would be higher, so one would want to separate them by a distance, if possible. Therefore, one must think about the current loop area and keeping that as small as possible in the layout. Designs with small loop areas have lower EMI.

Also, currents will follow the path of least impedance. At low frequencies, resistive effects will dominate. While at high frequencies, L and C effects dominate.

Thermal Considerations

Module layout can have a major impact on the noise levels of the final product due to elevating the module temperature. It is important to consider good thermal management strategies to prevent degradation of image quality.

Module Layout Best Practices

The following sections attempt to provide design guidelines and considerations regarding various areas of the layout. We realize that most designs cannot conform to all of these rules due to size and other constraints, but they are presented such that the layout designer can think about the tradeoffs in his own design.

- Follow Micron data sheet and developer guide for information to correctly terminate unused pins.
- The use of multilayer boards with a solid power and ground plane is preferred to lower inductance and to minimize crosstalk.
- If a solid plane is not possible, consider minimizing the overall inductance of the current return path.
- All high-frequency signals should flow over a solid ground plane related to the signal to minimize the current return loop.
- When using flex cables, use a return path under the signal traces where possible.
- For external connections, place all the connectors that will go to the same destination board close to each other to avoid large current return loop.
- Use ground plane under traces to minimize crosstalk (for example, on flex between sensor and connector; a thin lamination under traces is better than a thick one).
- Route signal traces over their respective power/ground return paths. This means digital areas over digital ground, and analog portions over analog ground.
- Differential traces should be adjacent and matched physically.
- Use VIAs carefully. VIAs represent discontinuity in the signal path.
- Use additional ground pads to isolate signals and to allow for short return paths.
- Separate digital and analog grounds.

One must also keep in mind the design trade-off between electrical and thermal requirements. Design rules to optimize signal integrity can often negatively affect thermal performance of the system. Verify that there is a sufficient thermal path to reduce the die operating temperature that would otherwise affect image quality.

Clocks and High-Speed Traces

- Widen spacing between HS signal lines as routing restrictions allow extra space, especially on the clock inputs.
- Keep high speed (that is, fast Tr,Tf) signals away from the clock lines.
- Shield the clock with grounded adjacent traces.
- Keep clock traces as straight, and short, as possible.
- Discontinuities on a transmission path will degrade a signal. Do not use sharp 90-degree bends. Mitered 45-degree bends are preferred.
- Keep clock signals on a single layer.
- Turn on slew rate control, if available, to slow down fast edges when speed is not critical to minimize simultaneous pad switching currents and ground bounce and minimize over- and undershoot due to pulse reflections from the load.
- If necessary, use proper terminations to reduce potential reflections and ringing on fast signals.
- Limit high frequency signals as much as possible.
- Avoid VIAs, which can cause impedance changes and reflections.

Power Supply

- As much as possible, use solid plane layers to distribute power.
- Be aware that shared power distributions may increase crosstalk between physical areas.
- Traces related to power and ground should be as short and as wide as possible to reduce the potential for supply sag and ground bounce effects.
- Consider trace inductance and mutual coupling when designing power distribution.
- Pair respective power supply lines and areas.
- Strive for a low inductance power and ground trace.
- Space power and ground pads to allow for required bypass capacitors.
- Maintain as much plane structure and connectivity as possible. Try not to tear up the ground planes with too many holes and cuts.
- Minimize the spacing between planes to increase coupling and create built in capacitance.
- Do not share VIAs.
- Provide sufficient power and ground connections.
- Connect each ground pad or VIA to the ground and power planes individually. Avoid daisy-chaining connections.
- Remember that bond wires will typically add 1nH/mil for 1mil (25 microns) gold wire.

Power Supply Decoupling and Bypassing

Bypassing is used for reducing the high frequency current flow by shunting and reducing the noise current to ground. Proper bypassing is required for decoupling. The bypassing path must provide significantly lower impedance at the frequency of interest than the power supply leads.

The goal of decoupling, on the other hand, is to prevent the transmission of noise from one part of the circuit to another by providing isolation between the two circuits to insure proper operation.

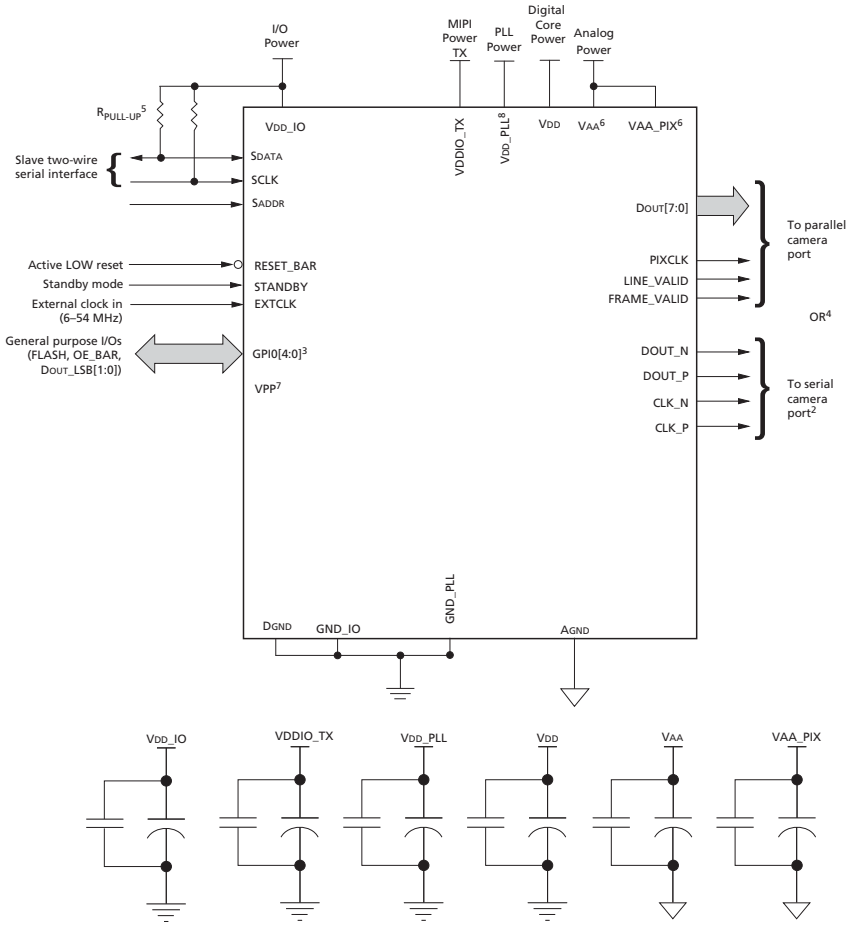
Decoupling and bypassing typically involve using capacitors tied to ground, or other trace signals to reduce noise levels.

Capacitor Guidelines

- Current Micron guidelines recommend a 1µF and 0.1µF capacitor for each supply. However, with every design being unique, modifications can be made depending upon system requirements.
- The minimum decoupling capacitor must be able to supply the current required during worst case switching conditions. One can use $C(dV) = di/dt$ to calculate the required capacitor sizes.
- In a real system with parasitic effects, the circuit will consist of multiple RLC components.
- Use surface mount low effective series resistance (ESR) capacitors to minimize lead inductance over a high range of frequencies.
- Multiple capacitors on a supply makes it easier for physical distribution, lowering effective inductance and ESR. However, in using multiple capacitors, be aware that a frequency resonant pole can be created between the values used.
- Mount the capacitor as close as possible to the sensor power and ground pads.
- Place the smaller, high frequency capacitors nearer to the sensor pads to provide transient currents required.
- Use large, multiple VIAs from the capacitors to the power planes to minimize R and L while allowing for maximum current flow.
- Use wide, short traces between VIAs and capacitor pads, or adjacent to the pad.
- A real world capacitor is not just a bulk capacitor, but can be modeled as a RLC in series. Be aware of the frequency characteristics of the components used.
- Verify that the temperature characteristics of the capacitors used will be suitable.

Current Micron Recomendation

Figure 6: Typical Connection for the MT9M113



It is recommended that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations.

Micron will recommend capacitor placement and values as defined in the data sheet and design guide documents. These are based upon our demo camera design and verified in hardware. Since hardware design is influenced by many factors, such as the uniqueness of the sensor layout, operating condition and component selection, the customer is ultimately responsible for their own design.

Summary

We have presented some general module layout guidelines for our customers to consider and have touched upon a few of the concepts of signal integrity to help familiarize our customers with the basis of those rules.

Schematic and layout reviews are available for Micron customers.

Additional Resources

Additional Imaging Technical Notes are available:

- TN-09-49 Connecting Bypass Capacitors to MT9M112
- TN-00-06 Bypass Capacitor Selection for High-Speed Designs

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

Rev. A 9/17/2007

- Initial release