Technical Note

MT9V024
Latency of Exposure or Gain Switch

Introduction

As new applications have emerged, so has the requirement for camera systems to be able to switch quickly between two imaging tasks. For example, some forward looking camera systems are being used in automobiles to capture an image of lane markers in a lane departure warning system, then quickly switch to capture an image of the horizon in an adaptive head lamp control system. The ideal image sensor operating conditions for capturing these two images vary greatly in exposure time and video gain settings. Therefore, the sensor chosen needs to predictably switch between these two sets of operating conditions.

This technical note discusses and diagrams the latencies involved in the Aptina MT9V024 CMOS digital image sensor's response to a change of either the exposure or gain registers. With an understanding of this latency, a sequence of register settings can guarantee that the intended exposure time and video gain settings are matched with the correct frame readout.

While this document describes the latencies associated with the exposure and gain registers, it can be applied universally to all other registers that are described in the image sensor data sheet.

Frame-Start and AEC/AGC-Sample Descriptions

The MT9V024 image sensor explicitly prevents certain registers from changing in the middle of a readout sequence. If these registers were to change during readout, it would result in a corrupted image showing either inconsistent LINE_VALID (LV) behavior or a change in signal intensity within the same image. These registers are buffered (shadowed) and do not become active until a fixed point in time, referred to as "frame-start," "AEC-sample," or "AGC-sample." These are internally generated timing signals which serve to latch-in, or make active, the shadowed registers. Depending on the exposure mode selected (master, snapshot, or slave [refer to description of R0x07 in MT9V024 datasheet for details]), the frame-start, AEC-sample, and AGC-sample signals will occur at different times in the data output sequence.

- In master mode, under default register settings, the frame-start occurs four row-times before the rising edge of the FRAME_VALID (FV) signal (start of data readout).
- In master mode, under default register settings, the AEC-sample and AGC-sample signals occur simultaneously, four row-times after the falling edge of the FV signal (end of data readout).
- In snapshot or slave modes, under default register settings, the frame-start occurs four row-times after the falling edge of the FV signal (end of data readout).

Mode Sequences

Master Mode Sequence

The sequence of steps for changing the exposure value and seeing this change reflected in a new image at the output of the sensor in master mode (as shown in Figure 1 on page 4) is:

1. Change the exposure setting from A to B by writing a new exposure value to the exposure register using the two-wire serial interface bus in frame *n*.
2. AEC-sample writes the new exposure value to the shadow register near the end of frame *n*.
3. Frame-start activates the new exposure value at the start of frame *n + 1*.
4. The image reflecting this new exposure value is available at the sensor output in frame *n + 2*.

Similarly, the sequence of steps for changing the gain value and seeing this change reflected in a new image at the output of the sensor in master mode (as shown in Figure 2 on page 4) is:

1. Change the gain setting from A to B by writing a new gain value to the gain register using the two-wire serial interface bus in frame *n*.
2. AGC-sample writes the new gain value to the shadow register near the end of frame *n*.
3. Frame-start activates the new gain value at the start of frame *n + 1*.
4. The image reflecting this new gain value is available at the sensor output in frame *n + 1*.

Snapshot Mode Sequence

The sequence of steps for changing the exposure value and seeing this change reflected in a new image at the output of the sensor in snapshot mode (as shown in Figure 3 on page 5) is:

1. Change the exposure setting from A to B by writing a new exposure value to the exposure register using the two-wire serial interface bus in frame *n*.
2. Frame-start activates the new exposure value at the beginning of frame *n + 1*.
3. The new exposure value is used by the sensor to capture a new image in frame *n + 1*.
4. Later in frame *n + 1*, the image reflecting this new exposure value is available at the sensor output.

Similarly, the sequence of steps for changing the gain value and seeing this change reflected in a new image at the output of the sensor in snapshot mode (as shown in Figure 4 on page 5) is:

1. Change the gain setting from A to B by writing a new gain value to the gain register using the two-wire serial interface bus in frame *n*.
2. Frame-start activates the new gain value at the beginning of frame *n + 1*.
3. The new gain value is used by the sensor in frame *n + 1*.
4. Later in frame *n + 1*, the image reflecting this new gain value is available at the sensor output.

Slave Mode Sequence

The sequence of steps for changing the gain value and seeing this change reflected in a new image at the output of the sensor in slave mode (as shown in Figure 5 on page 6) is:

1. Change the gain setting A to B by writing a new gain value to the gain register using the two-wire serial interface bus in frame *n*.
2. Frame-start activates the new gain value at the beginning of frame *n + 1*.
3. The new gain value is used by the sensor in frame *n + 1*.
4. Later in frame *n + 1*, the image reflecting this new gain value is available at the sensor output.

Master Mode Sequences

Figure 1: Latency of Exposure Register in Master Mode

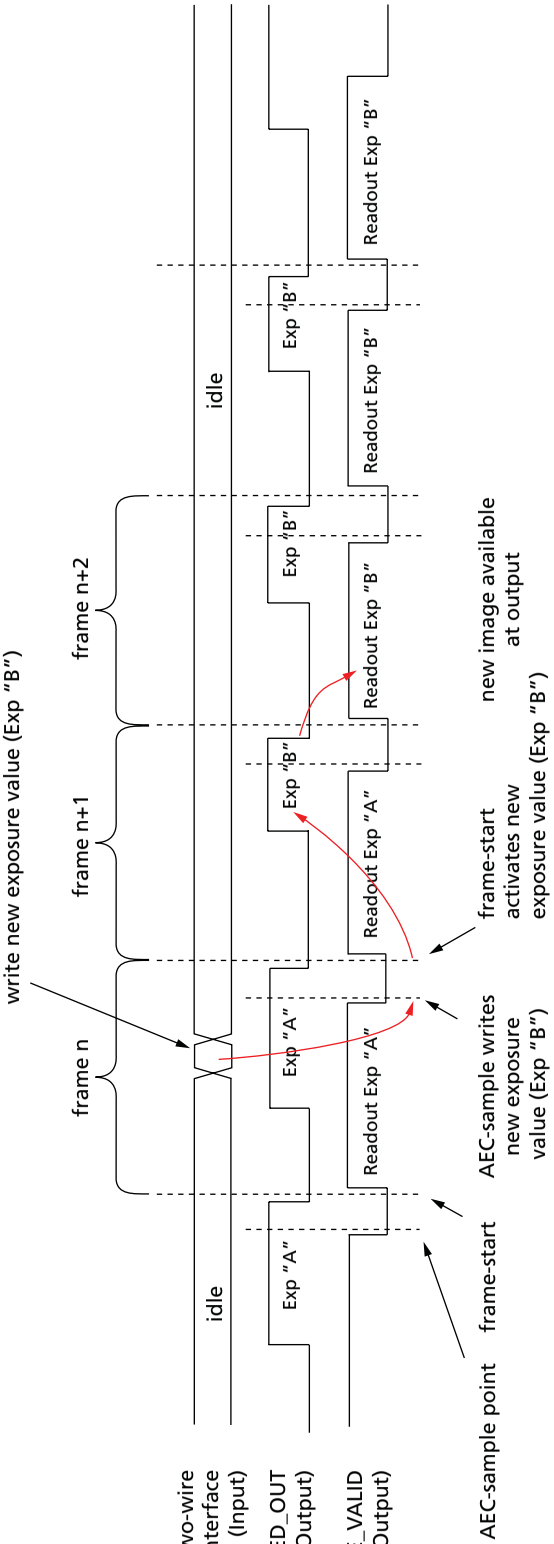
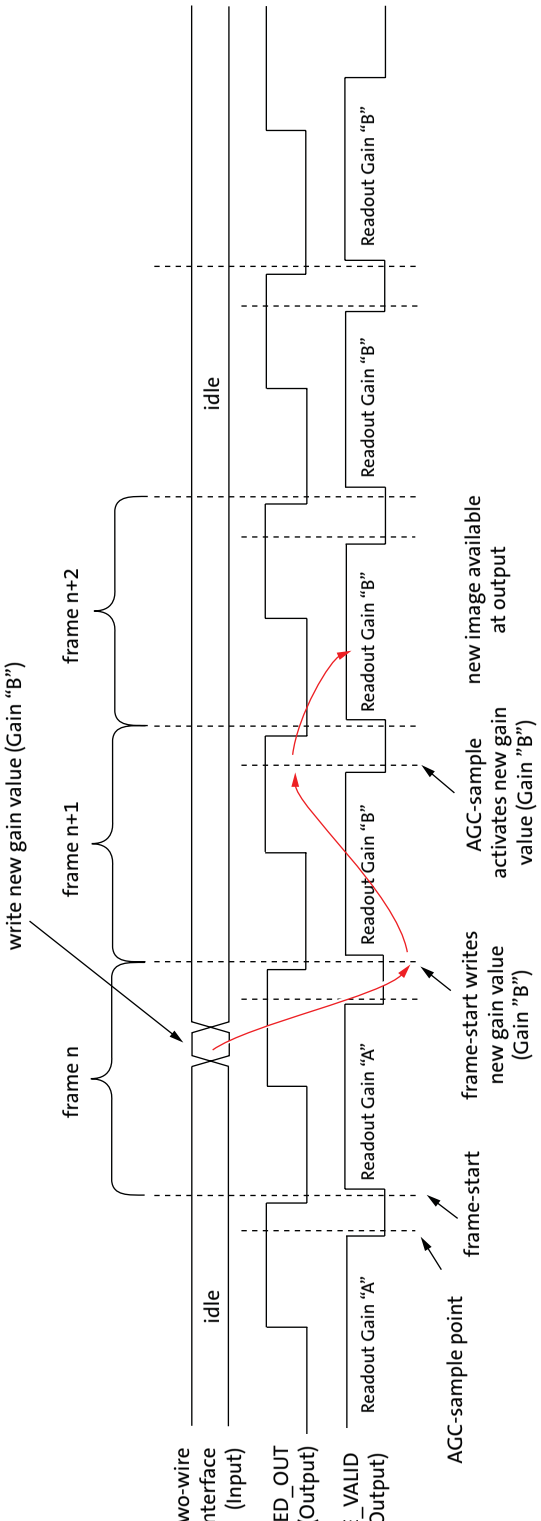


Figure 2: Latency of Gain Register(s) in Master Mode



Snapshot Mode Sequences

Figure 3: Latency of Exposure Register in Snapshot Mode

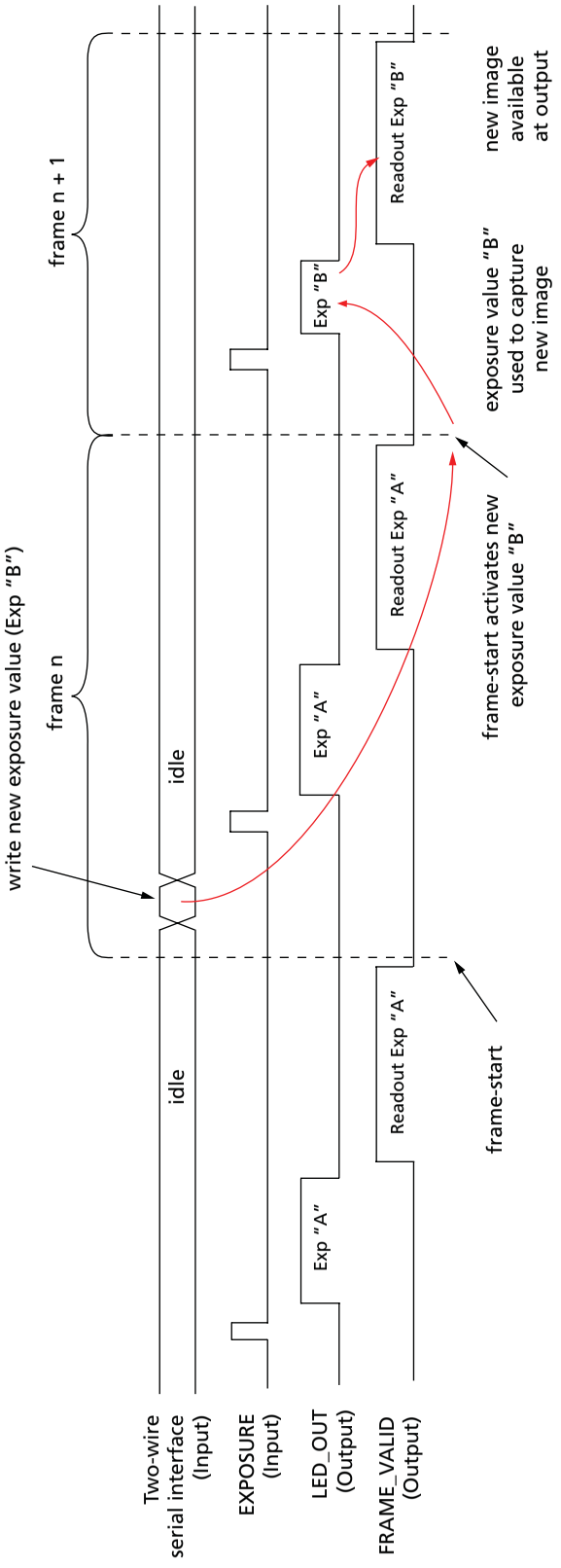
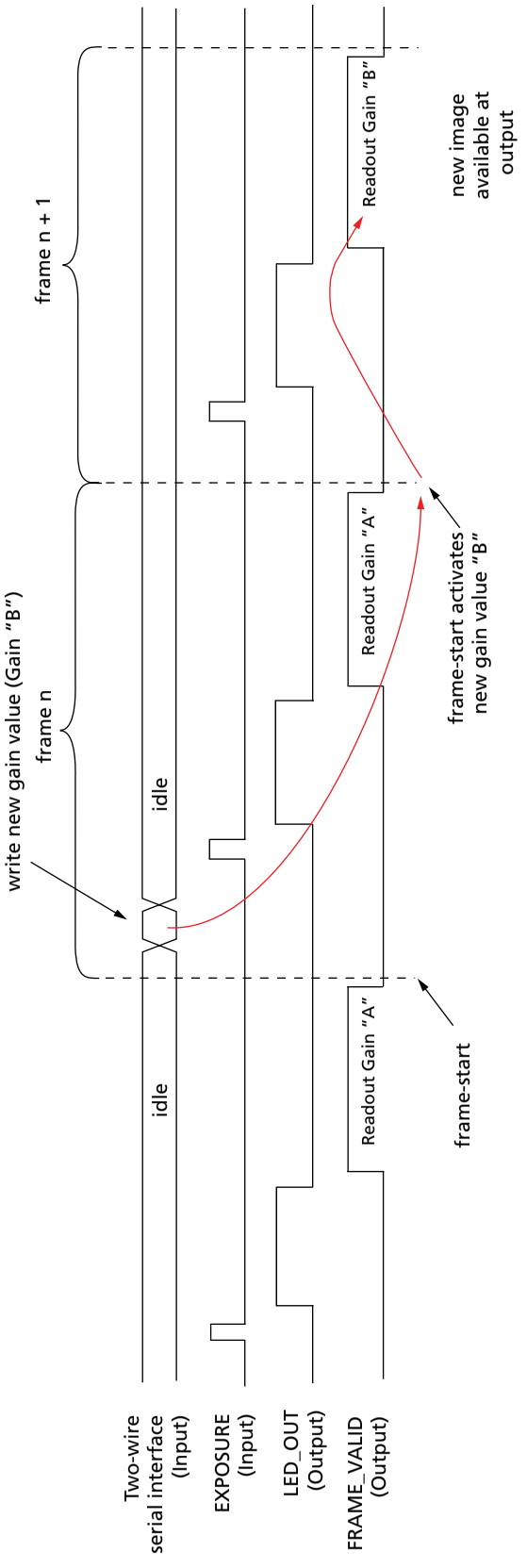
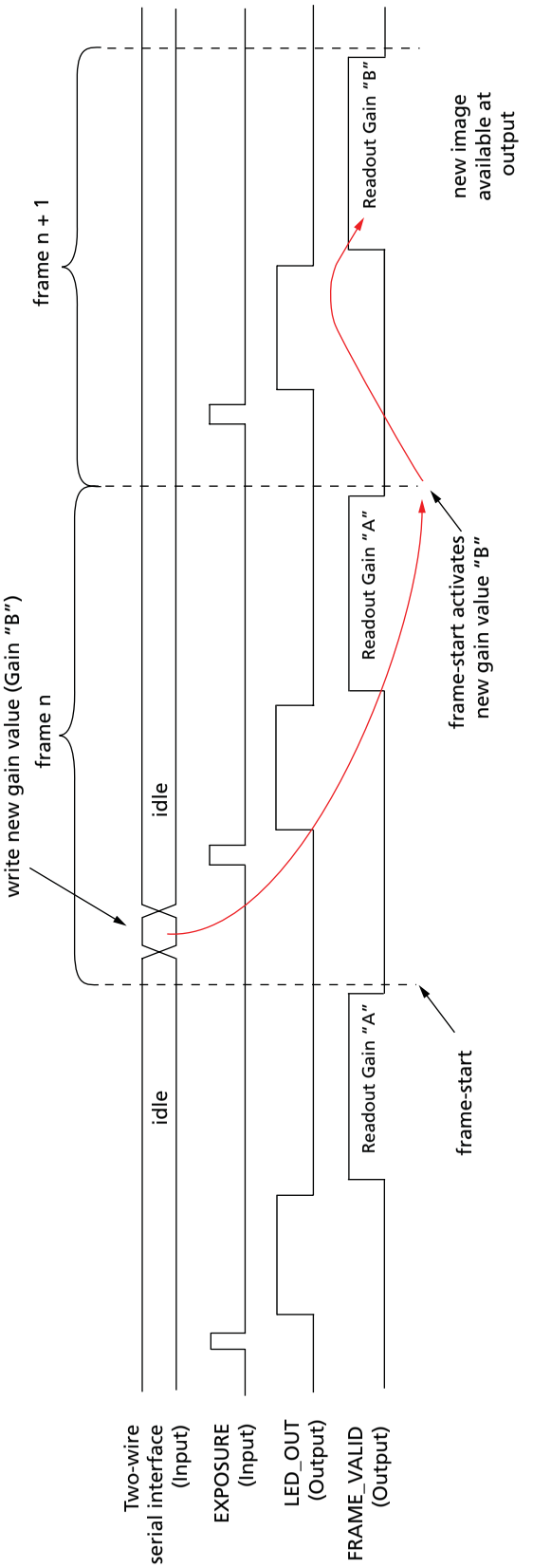


Figure 4: Latency of Gain Register(s) in Snapshot Mode



Slave Mode Sequence

Figure 5: Latency of Gain Register in Slave Mode



Conclusion

With an understanding of the latency involved in making changes to exposure and gain register settings, a system can be designed to predictably switch between two disparate imaging applications in the same camera head.

For more information on register latencies, or for more information on this and other features, refer to the MT9V024 1/3-inch Wide-VGA CMOS digital image sensor data sheet on Aptina's web site at www.aptina.com.

Revision History

Rev. A 6/14/10

- Initial release

10 Eunos Road 8 13-40, Singapore Post Center, Singapore 408600 prodmktg@aptina.com www.aptina.com