Technical Note

MT9V024 Stand-Alone Serial Operation

Introduction

The LVDS (low voltage differential signalling) interface of MT9V024 allows for the streaming of sensor data serially to a standard off-the-shelf deserializer. The pixels (and controls) are packeted—12-bit packets for stand-alone mode and 18-bit packets for stereoscopy mode. All serial signaling (clock and data) is LVDS. The LVDS serial output could either be data from a single sensor (stand-alone) or stream-merged data from two sensors (self and its stereoscopic slave pair). This technical note describes in detail the topology for the stand-alone serial operation.

LVDS Serial (Stand-Alone) Output

Based on the value of R182 bit 0 (10-bit pixel enable), the deserializer attached to a stand-alone sensor will be able to reproduce one of the two parallel outputs:

- Standard PIXEL_DATA[9:2], LINE_VALID, and FRAME_VALID
- PIXEL_DATA[9:0] containing embedded codes for LINE_VALID, and FRAME_VALID which can be retrieved with a small piece of logic

LVDS Output Format

In stand-alone mode, the packet size is 12 bits (2 frame bits and 10 payload bits). The user can select 10- bit pixels or 8- bit pixels. In 8-bit pixel mode, the packet consists of a start bit, 8-bit pixel data, the LINE_VALID bit, the FRAME_VALID bit, and the end bit. For 10-bit pixel mode, the packet consists of a start bit, 10-bit pixel data, and the end bit.

Table 1: LVDS Packet Format in Stand-Alone Mode (Stereoscopy Mode Bit De-Asserted)

12-Bit Packet	use_10-bit_pixels Bit De-Asserted (8-bit mode)	use_10-bit_pixels Bit Asserted (10-bit mode)
Packet[0]	HIGH (Start bit)	HIGH (Start bit)
Packet[1]	PixelData[2]	PixelData[0]
Packet[2]	PixelData[3]	PixelData[1]
Packet[3]	PixelData[4]	PixelData[2]
Packet[4]	PixelData[5]	PixelData[3]
Packet[5]	PixelData[6]	PixelData[4]
Packet[6]	PixelData[7]	PixelData[5]
Packet[7]	PixelData[8]	PixelData[6]
Packet[8]	PixelData[9]	PixelData[7]
Packet[9]	Line_Valid	PixelData[8]
Packet[10]	Frame_Valid	PixelData[9]

Table 1: LVDS Packet Format in Stand-Alone Mode (Stereoscopy Mode Bit De-Asserted)

12-Bit Packet	use_10-bit_pixels Bit De-Asserted (8-bit mode)	use_10-bit_pixels Bit Asserted (10-bit mode)
Packet[11]	LOW (Stop bit)	LOW (Stop bit)

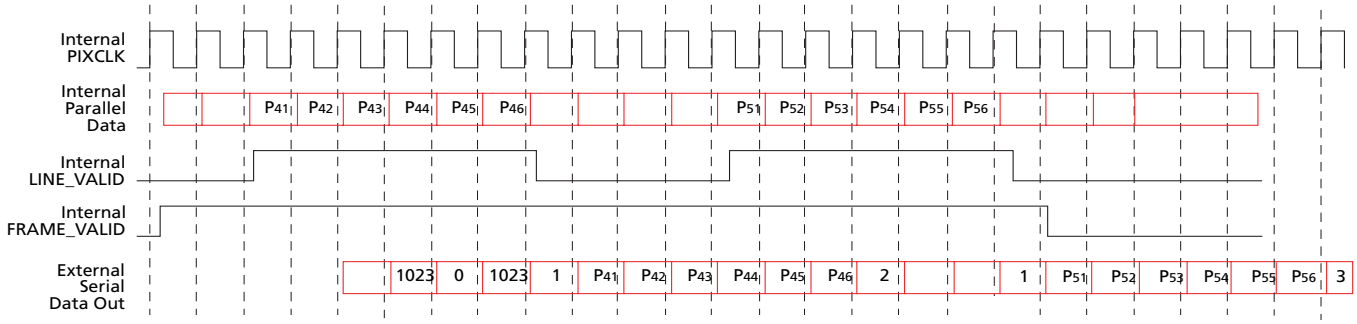
Control signals LINE_VALID and FRAME_VALID can be reconstructed from their respective preceding and succeeding flags that are always embedded within the pixel data in the form of reserved words.

Table 2: Reserved Words in the Pixel Data Stream

Pixel Data Reserved Word	Flag
0	Precedes FRAME_VALID Assertion
1	Precedes LINE_VALID Assertion
2	Succeeds LINE_VALID De-Assertion
3	Succeeds FRAME_VALID De-Assertion

If the sensor provides a pixel whose value is 0, 1, 2, or 3 (that is, the same as a reserved word), then the outgoing serial pixel value is switched to 4.

Figure 1: Standalone Serial Output Format for a 6 x 2 Frame showing location of embedded codes



Notes:
1. External pixel values of 0, 1, 2, 3 are reserved (they only convey control information). Any raw pixel of value 0, 1, 2, and 3 will be substituted with 4.
2. External pixel sequence 1023, 0 1023 is a reserved sequence (conveys control information). Any raw pixel sequence of 1023, 0, 1023 will be substituted with 1023, 4, 1023.

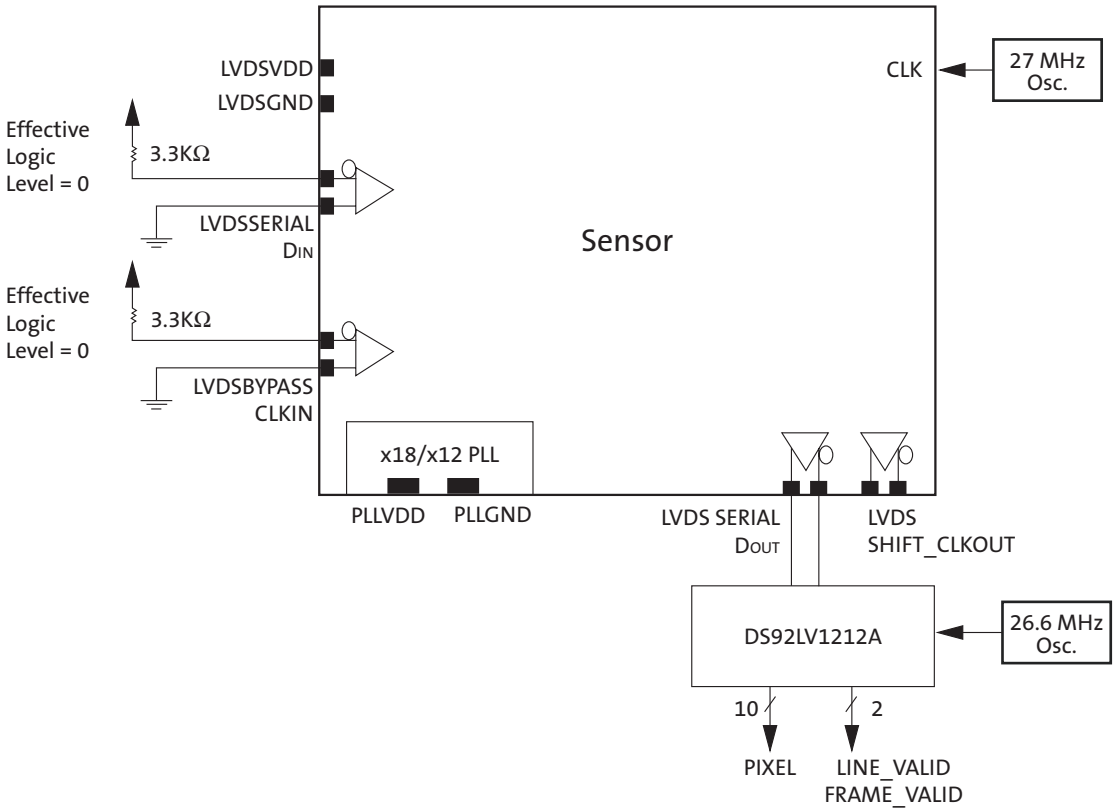
Topology

With the LVDS serial video output, the user can reconstruct the parallel stream using a deserializer as far away as 5 meter (approximately 15 feet) from the sensor. This serial link saves cabling cost of 14 wires (PIXEL_DATA[9:0], LINE_VALID, FRAME_VALID, PIXCLK, GND). Instead, just three wires (2 DIFFERENTIAL LVDS, 1 GND) are sufficient to carry the video signal.

In this configuration, the internal PLL generates the SHIFT_CLK (x12). LVDS signals SER_DATA_OUT and SER_DATA_OUT_ need be connected to a deserializer (that clocked at approximately the same system clock frequency as the sensor).

Figure 2 shows how an off-the-shelf deserializer can be use to retrieve the standard parallel signals of PIXEL_DATA[9:0], LINE_VALID, and FRAME_VALID.

Figure 2: Stand-Alone Topology



Configuration

Below is the typical configuration of the sensor:

1. Power-up sensor
2. Enable LVDS serial data out driver (set R179[4]= 0)
3. De-assert LVDS power-down (set R177[1] = 0)
4. Issue a soft RESET R12[0] = 1 followed by R12[0] = 0
5. Force sync patterns for the deserializer to lock (set R181[0] = 1)
6. Stop applying sync patterns (set R181[0] = 0)

LVDS Data Bus Timing

The LVDS bus timing waveforms and timing specifications are shown in Table 3 and Figure 3.

Figure 3: LVDS Timing

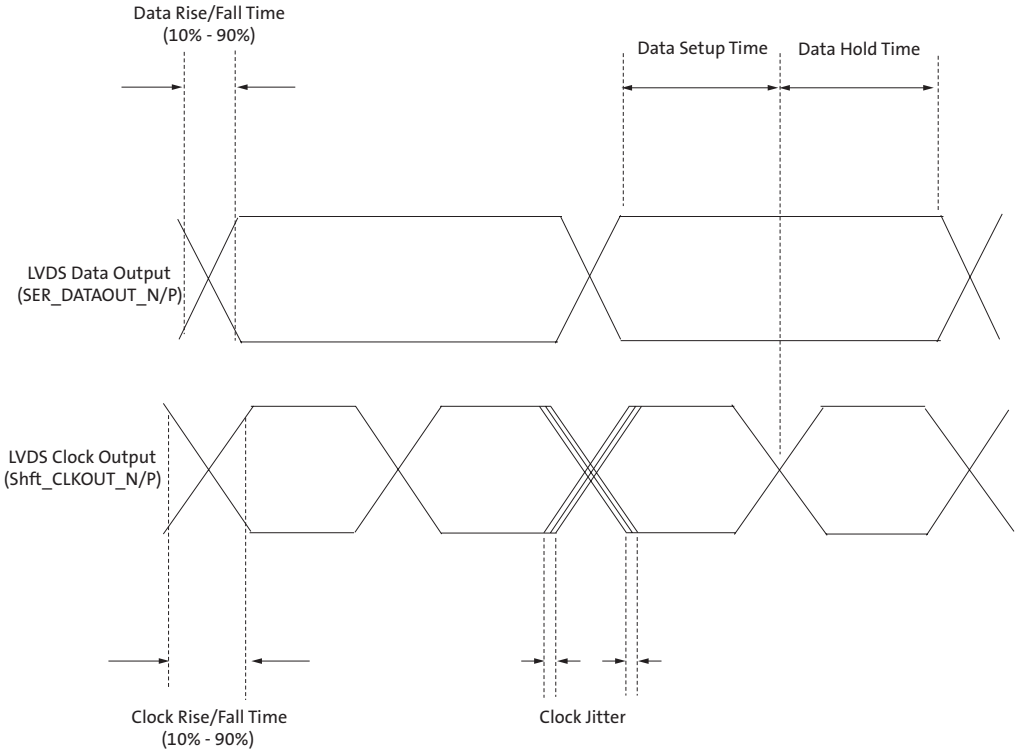


Table 3: LVDS AC Timing Specifications

V_{PWR} = 3.3V ±0.3V; T_J = –40°C to +105°C; output load = 100 Ω; frequency 27 MHz

Parameter	Minimum	Typical	Maximum	Unit
LVDS clock rise time	–	0.22	0.30	ns
LVDS clock fall time	–	0.22	0.30	ns
LVDS data rise time	–	0.28	0.30	ns
LVDS data fall time	–	0.28	0.30	ns
LVDS data setup time	0.3	0.67	–	ns
LVDS data hold time	0.1	1.34	–	ns
LVDS clock jitter	–		92	ps

Conclusion

In addition to its standard parallel output, the MT9V024 can provide a serial video stream output at the full rate of 60fps, a full resolution of 752x480 and a full pixel depth of 10 bits per pixel. This serial stream can be deserialized by an off-the-shelf deserializer upto 5 meters away. For further information and assistance on this feature, please contact your Aptina applications engineer at www.aptina.com.

Revision History

Rev. B **8/19/11**

- Updated trademarks
- Applied updated template

Rev. A **4/20/10**

- Initial release

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