Technical Note

MT9V032
Parallel and Serial Stereo Operation

Introduction

Micron's MT9V032 CMOS image sensor is designed to support lockstep operation. If two sensors are provided the same clock, the same reset, and the same two-wire serial interface stimulus at the device inputs, they will effectively operate in tandem (clock by clock). Therefore, two connected MT9V032 sensors can provide synchronized stereo output. This technical note describes the topology and configuration for the following operation modes:

- parallel stereo
- serial stereo

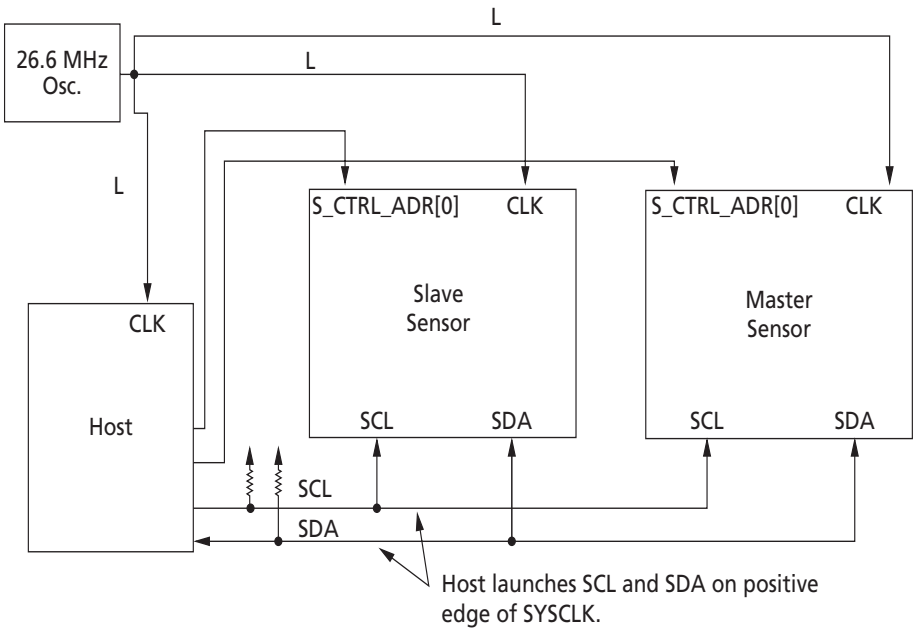
Broadcast and Individual WRITEs for Stereoscopic Operation

In stereoscopic mode, the two cameras are required to run in lockstep mode. This implies that control logic in each sensor will be in exactly the same state on every clock as its pair sensor. To ensure this, all inputs that affect control logic must be identical and arrive at the same time at each sensor.

These inputs include:

- system clock
- system reset
- two-wire serial interface clock—SCL
- two-wire serial interface data—SDA

Figure 1: Two-Wire Serial Interface Configuration in Stereoscopic Mode



Note: All system clock lengths (L) must be equal. SCL and SDA lengths to each sensor (from the host) must also be equal.

The setup in Figure 1 shows how the two sensors can maintain lockstep when their configuration registers are written through the two-wire serial interface. A WRITE to configuration registers would either be broadcast (simultaneous WRITES to both sensors) or individual (WRITE to just one sensor at a time). READs from configuration registers would be individual (READs from one sensor at a time).

One of the two serial interface slave address bits of the sensor is hardwired; the other is controlled by the host, allowing the host to perform either a broadcast or a one-to-one access.

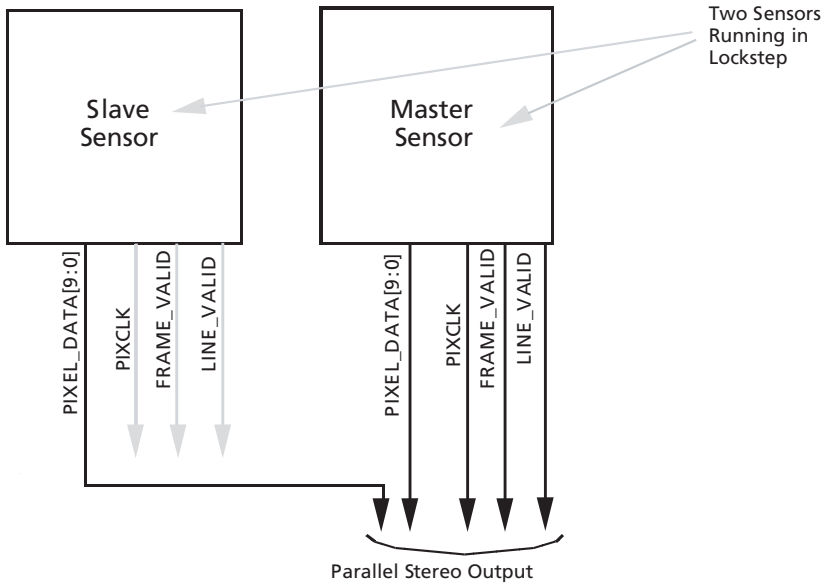
Broadcast WRITES are performed by setting the S_CTRL_ADR input pin for the slave and master sensors to the same state. Individual WRITES are performed by setting the S_CTRL_ADR input pin for the slave and master sensors to opposite states. Similarly, individual READs are performed by setting the S_CTRL_ADR input pin for the slave and master sensors to opposite states.

Note: The clock signal in Figure 1 must be attached to the host and to the two MT9V032 sensors—this guarantees the strict timing requirements of the system. The system may not work properly if the clock signal is not configured as shown.

Stereo Parallel Operation

This is the simpler of the two topologies. As long as the two sensors are in lockstep mode following the topology of Figure 2, the parallel output of each sensor device will be in sync with the other.

Figure 2: Parallel Stereo Operation Topology



Stereo Serial Operation

The LVDS interface allows the serial streaming of sensor data to a standard off-the-shelf deserializer up to 5 meters from the MT9V032 sensor. The pixel data and controls are packeted into 18-bit packets for stereoscopy mode. All serial signaling (clock and data) is LVDS. The LVDS serial output is stream-merged data from two sensors (itself and its stereoscopic pair).

The deserializer used in the stereoscopic configuration reproduces 8-bit parallel pixel data from each sensor (with embedded LINE_VALID and FRAME_VALID) and PIXCLK. Additional logic is required to extract LINE_VALID and FRAME_VALID from the serial data stream.

Since the two sensors are required to run in lockstep in stereoscopy mode, configuration WRITEs through the two-wire serial interface are done in such a way that both sensors can get their configuration updates simultaneously.

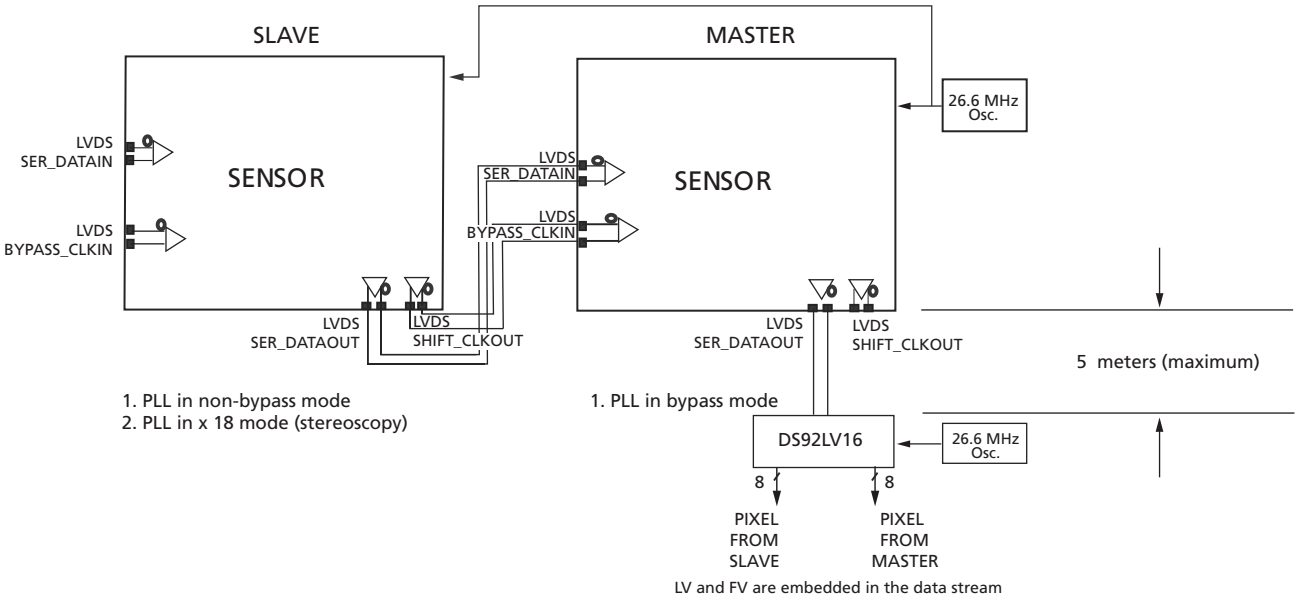
The inter-sensor serial link is designed in such a way that once the data delay (R0xB3[2:0]), shift-clk delay (R0xB2[2:0]), and stream latency select (R0xB4[1:0]) are configured (upon lock of the slave PLL), the master sensor will stream good stereo content regardless of any variation in supply voltage or temperature as long as they are within specification. Register parameters data delay, shift_clk delay, and stream latency select are either predetermined from the board layout or can be empirically determined by reading back the stereo-error flag. This flag gets asserted when the two merged sensor streams are not in sync. The combo register (R0xB9[15:0]) is used for the diagnosis of out-of-sync streams.

In stereo serial operation, the internal PLL generates the SHIFT_CLKOUT (x18) output in phase with the system clock. The LVDS signal SER_DATAOUT must be connected to a deserializer clocked at approximately the same system clock frequency.

Topology

Figure 3 shows how a standard off-the-shelf deserializer can be use to retrieve PIXEL_DATA[9:2]. Additional logic will be required to extract LINE_VALID and FRAME_VALID embedded within the pixel_data stream.

Figure 3: Stereoscopy Topology



Stereo Serial Configuration

The typical configuration of the master and slave sensors is as follows:

1. Power up the sensors.
2. Broadcast WRITE to de-assert LVDS power-down (set R0xB1[1] = 0).
3. Individual WRITE to master sensor putting its internal PLL into bypass mode (set R0xB1[0] = 1).
4. Broadcast WRITE to both sensors to set the stereoscopy bit (set R0x07[5] = 1).
5. Make sure all resolution, vertical blanking, horizontal blanking, window size, and AEC/AGC configurations are done through broadcast WRITE to maintain lockstep.
6. Broadcast WRITE to enable LVDS serial driver (set R0xB3[4] = 0).
7. Broadcast WRITE to enable LVDS receiver (set R0xB2[4] = 0).
8. Individual WRITE to master sensor, putting its internal PLL into bypass mode (set R0xB1[0] = 1).
9. Individual WRITE to slave sensor, enabling its internal PLL (set R0xB1[0] = 0).
10. Individual WRITE to slave sensor, setting it as a stereo slave (set R0x07[6] = 1).
11. Individual WRITEs to master sensor to minimize the inter-sensor skew (set R0xB2[2:0], R0xB3[2:0], and R0xB4[1:0] appropriately). Use R0xB7 and R0xB8 to get lockstep feedback from stereo_error_flag.
12. Broadcast WRITE to issue a soft reset (set R0x0C[0] = 1 followed by R0x0C[0] = 0).

Note: The stereo_error_flag is set if a mismatch has occurred at a reserved byte (slave and master sensor's codes at this reserved byte must match). If the flag is set, steps 11 and 12 are repeated until the stereo_error_flag remains cleared.

LVDS Output Format

In stereoscopic mode, the packet size is 18 bits (2 frame bits and 16 payload bits). The packet consists of a start bit, the master pixel byte (with sync codes), the slave byte (with sync codes), and the end bit.

Table 1: LVDS Packet Format in Stereoscopy Mode (Stereoscopy Mode Bit Asserted)

18-Bit Packet	Function
Packet[0]	HIGH (Start bit)
Packet[1]	MasterSensorPixelData[2]
Packet[2]	MasterSensorPixelData[3]
Packet[3]	MasterSensorPixelData[4]
Packet[4]	MasterSensorPixelData[5]
Packet[5]	MasterSensorPixelData[6]
Packet[6]	MasterSensorPixelData[7]
Packet[7]	MasterSensorPixelData[8]
Packet[8]	MasterSensorPixelData[9]
Packet[9]	SlaveSensorPixelData[2]
Packet[10]	SlaveSensorPixelData[3]
Packet[11]	SlaveSensorPixelData[4]
Packet[12]	SlaveSensorPixelData[5]
Packet[13]	SlaveSensorPixelData[6]
Packet[14]	SlaveSensorPixelData[7]
Packet[15]	SlaveSensorPixelData[8]
Packet[16]	SlaveSensorPixelData[9]
Packet[17]	LOW (Stop bit)

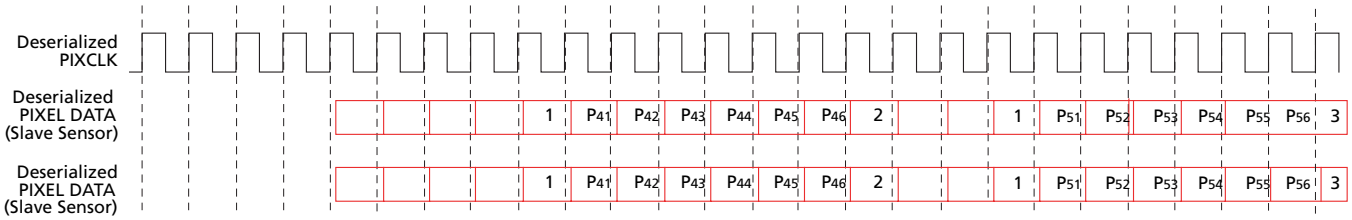
Control signals LINE_VALID and FRAME_VALID can be reconstructed from their respective preceding and succeeding flags that are always embedded within the pixel data in the form of reserved words.

Table 2: Reserved Words in the Pixel Data Stream

Pixel Data Reserved Word	Flag
0	Precedes FRAME_VALID assertion
1	Precedes LINE_VALID assertion
2	Succeeds LINE_VALID De-assertion
3	Succeeds FRAME_VALID De-assertion

If the sensor provides a pixel whose value is 0, 1, 2, or 3 (that is, the same as a reserved word), then the outgoing serial pixel value is switched to 4.

Figure 4: Serial Stereo Output Format for a 6 x 2 Frame



Note: External pixel values of 0, 1, 2, 3 are reserved (they only convey control information). Any raw pixel of value 0, 1, 2, and 3 will be substituted with 4.

With the LVDS serial video output, the deserializer can be up to 5 meters from the sensor. The serial link can save on the cabling cost of 14 wires (DOUT[9:0], LINE_VALID, FRAME_VALID, PIXCLK, GND). Instead, three wires (two serial LVDS, one GND) are sufficient to carry the video signal.

Conclusion

The MT9V032 sensor supports both parallel-stereoscopy and serial-stereoscopy. In either topology, the two sensor devices are required to run in lockstep mode for a pixel-synchronous stereo stream.

For further information and assistance on this feature, contact your local Micron Imaging FAE or refer to our Web site at www.micron.com/imaging.

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Revision History

Rev. A 8/16/2006

- Initial release