Technical Note

MT9V013 Power Sequencing and Sample Register Settings

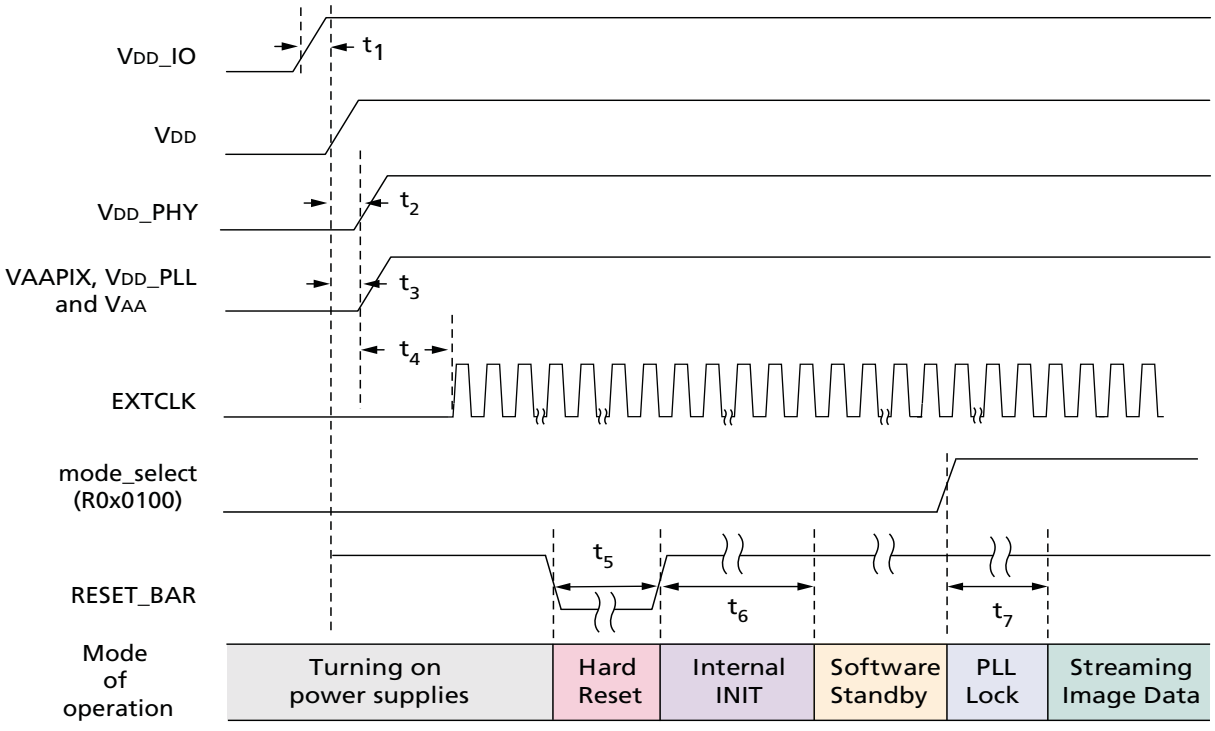
Introduction

This technical note describes both the power-up sequence and power-down sequence and provides sample register settings (MIPI) for the Micron® MT9V013 CMOS image sensor.

Power-Up Sequence

The recommended power-up sequence for the sensor is shown in Figure 1, Power-Up Signal Waveforms and Table 1, "Power-Up Signal Timing," on page 2.

Figure 1: Power-Up Signal Waveforms



Notes: 1. Figure not drawn to scale.

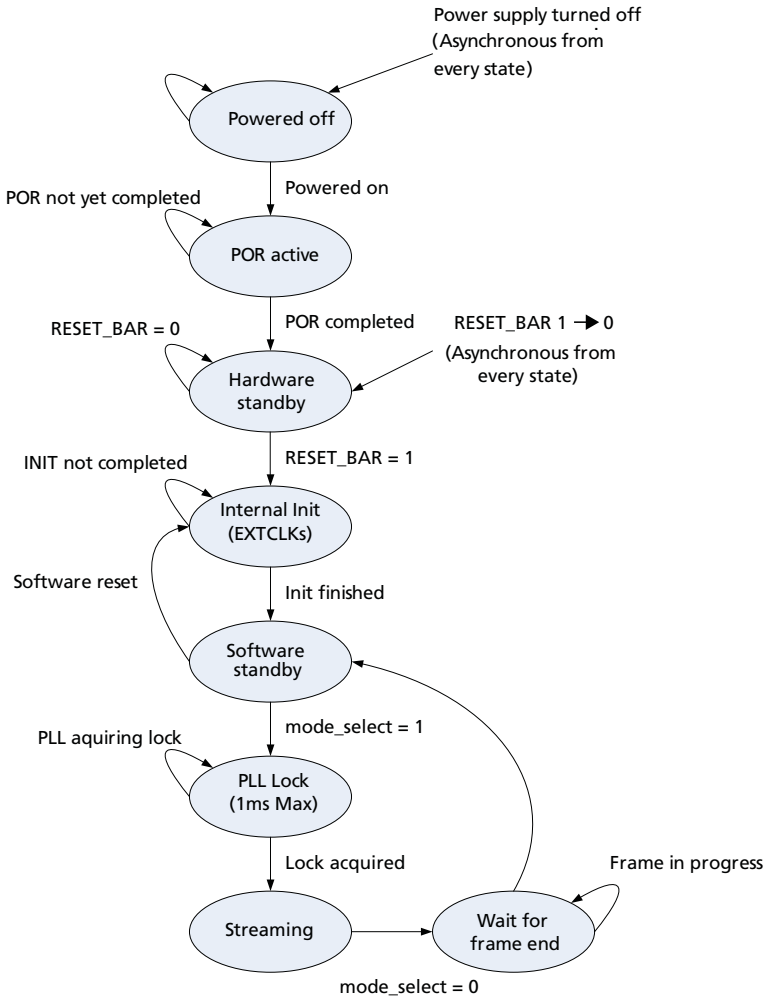
Table 1: Power-Up Signal Timing

Definition	Symbol	Min	Typ	Max	Units
VDD_IO to VDD time	$^{t}1$	0	–	500	ms
VDD to VDD_PHY time	$^{t}2$	1	–	500	ms
VDD to VAA/VAAPIX/ VDD_PLL	$^{t}3$	1	–	500	ms
VAA TO EXTCLK	$^{t}4$	1	–	–	ms
Active hard reset	$^{t}5$	1	–	–	ms
Internal initialization	$^{t}6$	2400	–	–	EXTCLKs
PLL lock time	$^{t}7$	–	–	1	ms

Power-up State Sequence

The recommended power-up sequence for the MT9V013 is shown as a state diagram in Figure 2.

Figure 2: MT9V013 System States For Power-Up



Power-Up Sequence Description

The available power supplies (VDD_IO, VDD, VDD_PLL, VAA, VAAPIX, and VDD_PHY) can be turned on at the same time or have the separation specified below:

1. Turn on the VDD_IO power supply.
2. After 1–500ms, turn on the VDD power supply.
3. After 1–500ms, turn on the VDD_PHY, the VAA/VAAPIX, and the VDD_PLL power supplies.
4. After the last power supply is stable, enable EXTCLK.
5. Assert RESET_BAR for at least 1ms.
6. Wait 2400 EXTCLKs to transition from internal initialization into software standby mode.
7. Configure the PLL, output, and image settings to desired values by writing to registers using the two-wire serial interface bus.
8. Set mode_select = 1 (R0x0100).
9. Wait 1ms for the PLL to lock before the streaming image data state is reached.

Low-Power Standby State

Once the last supply is stable within the valid ranges specified below, the sensor enters a low-power hardware standby state.

- Analog voltage: 2.50–3.10V (2.80V nominal)
- Digital voltage: 1.70–1.95V (1.80V nominal)

Exit from the hardware standby mode is controlled by the latter of two events:

1. The negation of the RESET_BAR (XSHUTDOWN) input.
2. A time-out of the internal power-on reset circuit.

When RESET_BAR is asserted, it asynchronously resets the sensor, truncating any frame that is in progress. At that time, the sensor is in its lowest-powered state. When the sensor leaves the hardware standby state, it performs an internal initialization sequence with a duration of 2400 EXTCLK cycles and then enters a low-power software standby state.

The MT9V013 will not respond to read transactions on its two-wire serial interface while the initialization sequence is in progress. Polling a sensor register (R0x0000–0001 for example) allows the user to determine when the initialization sequence has completed. Register R0x0000-0001 will return a value of 0x2200 when the initialization sequence is completed.

When the sensor leaves software standby mode, it enables the voltage-controlled oscillator (VCO) through mode_select = 1. An internal delay (1 ms max) will keep the PLL disconnected until the PLL can achieve phase lock. Once the lock sequence is completed, the sensor begins streaming new image data.

Note: Cycle times listed here are preliminary and subject to change.

Soft Reset Sequence

The MT9V013 has the option of software reset control by writing a “1” to the software_reset register (R0x0103). A software reset asynchronously resets the sensor, truncating any frame that is in progress. The sensor briefly enters the hardware standby state and then starts its internal initialization sequence. At that point, the behavior is identical to the power-on reset sequence.

Register Descriptions

The following registers should be set during internal initialization.

Table 2: Register Descriptions
Hexadecimal values are preceded 0x. All other values are in decimal.

Register	Description
R0x0100	**mode_select (RW)** Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low-power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface. This register field is an alias of R0x301A[2].
R0x0103–0104	**software_reset (RW)** This bit always reads as 0. Setting this bit initiates a reset sequence; the frame being generated will be truncated. This register field is an alias of R0x301A–301B[0].
R0x0104–0105	**grouped_parameter_hold (RW)** 0 = Update of many of the registers is synchronized to frame start. 1 = Inhibit register updates; register changes will remain pending until this bit is returned to "0". When this bit is returned to 0, all pending register updates will be made on the next frame start. This register field is an alias of R0x301A–301B[15].
R0x0202–0203	**coarse_integration_time (RW)** Integration time programmed in units of line_length_pck. This register is an alias of R0x3012–3013.
R0x301A–301B	**reset_register (RW)**
R0x3056–3057	**green1_gain(R/W)**
R0x3058–3059	**blue_gain(R/W)**
R0x305A–305B	**red_gain(R/W)**
R0x305C–305D	**green2_gain(R/W)**
R0x0302–0303	**vt_sys_clk_div (RW)** Clock divisor applied to PLL output clock to generate video timing system clock.
R0x0304–0305	**pre_pll_clk_div** Clock divisor applied to EXTCLK to generate PLL input clock.
R0x0306–0307	**pll_multiplier (RW)** Clock multiplier applied to PLL input clock.
R0x0340–0341	**frame_length_lines (RW)** The number of complete lines (rows) in the output frame, including visible lines and vertical blanking lines. This register is an alias of R0x300A–300B.
R0x0342–0343	**line_length_pck (RW)** The number of pixel clock periods in one line (row) time, including visible pixels and horizontal blanking time. This register is an alias of R0x300C–300D.
R0x0344–0345	**x_addr_start (RW)** The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. This register is an alias of R0x3004–3005.
R0x0346–0347	**y_addr_start (RW)** The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. This register is an alias of R0x3002–3005.

Table 2: Register Descriptions (continued)
Hexadecimal values are preceded 0x. All other values are in decimal.

Register	Description
R0x0348–0349	**x_addr_end (RW)** The last column of visible pixels to be read out. This register is an alias of R0x3008–3009.
R0x034A–034B	**y_addr_end (RW)** The last row of visible pixels to be read out. This register is an alias of R0x3006–3007.
R0x034C–034D	**x_output_size (RW)** Set X output size of the displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of x_addr_end and x_addr_start.
R0x034E–034F	**y_output_size (RW)** Set Y output size of the displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of y_addr_end and y_addr_start. The output image will have two additional rows containing embedded data, in accordance with the frame format descriptors.
R0x0382–0383	**x_odd_inc (RW)** Increment applied to odd addresses in X (column) direction. 1 = Normal readout 3 = Read out alternate pixel pairs to halve the amount of horizontal data in a frame (“skip 2x”) This register field is an alias of R0x3040–3041[7:5].
R0x0386–0387	**y_odd_inc (RW)** Increment applied to odd addresses in Y (row) direction. 1 = Normal readout 3 = Read out alternate pixel pairs to halve the amount of vertical data in a frame (“skip 2x”) This register field is an alias of R0x3040–3041[4:2].

Register Values For Specific Modes

Table 3 shows the register settings required to operate the MT9V013 in a number of different modes. All the register settings are using a 16 MHz external clock.

Table 3: Register Values in Specific Modes

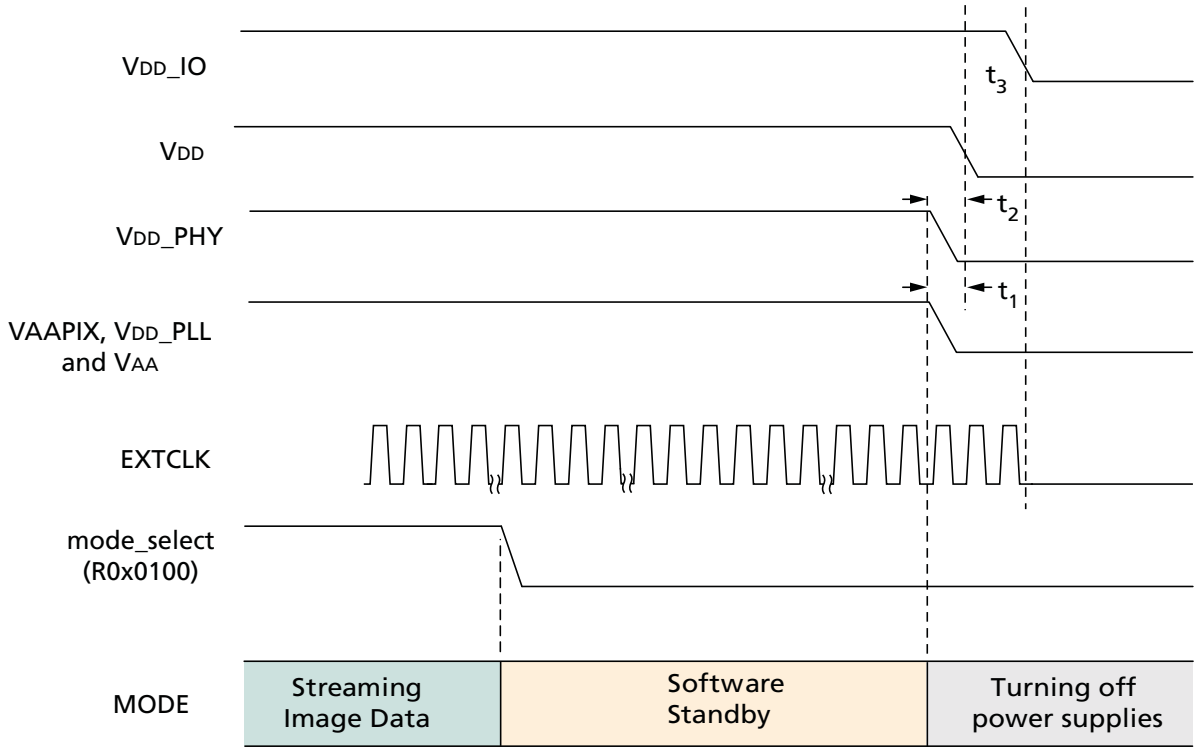
Register Number	Register Description	Modes of Operation[1]		
		Mode 1[2]	Mode 2[3]	Mode 3[4]
R0x0103	software_reset[5]	0x0001	0x0001	0x0001
R0x301A	reset_register	0x0018	0x0018	0x0018
R0x0100	mode_select	0x0000	0x0000	0x0000
R0x3064	Reserved	0x0804	0x0804	0x0804
R0x0304	pre_pll_clk_div	0x0004	0x0004	0x0004
R0x0306	pll_multiplier	0x0021	0x0013	0x0012
R0x0302	vt_sys_clk_div	0x0001	0x0001	0x0001
R0x0300	vt_pix_clk_div[6]	0x000A	0x000A	0x000A
R0x0104	grouped_parameter_hold	0x0001	0x0001	0x0001
R0x0344	x_addr_start	0x0004	0x0004	0x0004
R0x0346	y_addr_start	0x0004	0x0004	0x0004
R0x0348	x_addr_end	0x01E3	0x01E3	0x01E1
R0x034A	y_addr_end	0x0283	0x0283	0x0281
R0x0382	x_odd_inc	0x0001	0x0001	0x0003
R0x0386	y_odd_inc	0x0001	0x0001	0x0003
R0x034C	x_output_size	0x0280	0x0280	0x0140
R0x034E	y_output_size	0x01E0	0x01E0	0x00F0
R0x0202	coarse_integration_time[7]	0x013D	0x01B4	0x00D3
R0x0340	frame_length_lines	0x01FB	0x01FB	0x0103
R0x0342	line_length_pck	0x034A	0x034A	0x0202
R0x3056	green1_gain[7]	0x0230	0x0230	0x0230
R0x3058	blue_gain[7]	0x0230	0x0230	0x0230
R0x305A	red_gain[7]	0x0230	0x0230	0x0230
R0x305C	green2_gain[7]	0x0230	0x0230	0x0230
R0x0104	grouped_parameter_hold	0x0000	0x0000	0x0000
R0x0100	mode_select	0x0001	0x0001	0x0001

Notes:
1. Sample frame rates might not be optimal for flicker detection.
2. Mode 1 = VGA (640 x 480), RAW10, 31 fps, 16 MHz EXTCLK, 13.2 MHz pixel clock.
3. Mode 2 = VGA (640 x 480), RAW10, 18 fps, 16 MHz EXTCLK, 7.6 MHz pixel clock.
4. Mode 3 = QVGA (320 x 240), 2x skip, RAW10, 54 fps, 16 MHz EXTCLK, 7.2 MHz pixel clock.
5. A 300ms delay was used after a write access to this register, actual values may vary.
6. vt_pix_clk_div is fixed.
7. Integration time and gain values are examples only. Adjustments might be necessary.

Power-Down Sequence

The recommended power-down sequence for the sensor is shown in Figure 3, Power-Down Waveforms and Table 4, Power-Down Timing.

Figure 3: Power-Down Waveforms



Notes: 1. Figure not drawn to scale.

Table 4: Power-Down Timing

Definition	Symbol	Min	Typ	Max	Units
VAA/VAAPIX/VDD_PLL to VDD	$^{t}1$	0	–	500	ms
VDD_PHY to VDD	$^{t}2$	0	–	500	ms
VDD to VDD_IO	$^{t}3$	0	–	500	ms

Power-Down Sequence Description

The available power supplies (VDD_IO, VDD, VDD_PLL, VAA, VAAPIX, and VDD_PHY) can be turned off at the same time or have the separation specified below:

1. Disable streaming image data if the output is active by setting mode_select = 0 (R0x0100).
2. The soft standby state is reached after the current row or frame (depending on configuration) has ended.
3. Turn off the VAA/VAAPIX, VDD_PLL, and VDD_PHY power supplies.
4. After 1–500ms, turn off VDD power supply.
5. After 1–500ms, turn off VDD_IO power supply.

Conclusion

The MT9V013 sensor has recommended power-up and power-down sequences as well as a low power mode, which can reduce current drain and extend battery life.

For the latest data sheet, refer to Micron's Web site www.micron.com.

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Revision History

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- Initial release