Technical Note

MT9V022
Guidelines for Circuit Board Design

Introduction

This technical note includes guidelines for effective PCB design for the Aptina® MT9V022 CMOS image sensor. It discusses placement of and connection to bypass capacitors, provides schemes for analog and digital ground partitioning, and highlights various layout and design issues. These recommendations provide useful information for a more effective design.

Bypass Capacitors

Combinations of 0.01µF to 1.0µF ceramic surface mount (SMT) capacitors are recommended for the system design. The bypass capacitors should be placed as close as possible to the power pins on the image sensor. This is extremely important for the bypass capacitors used on VAA and VAA_PIX. Separate bypass capacitors should be used for VAA, VAA_PIX, VDD, and VDDLVDS. A minimum of 0.1µF capacitor is recommended for VDD and VDDLVDS.

Figure 1: Recommended Bypass Capacitors

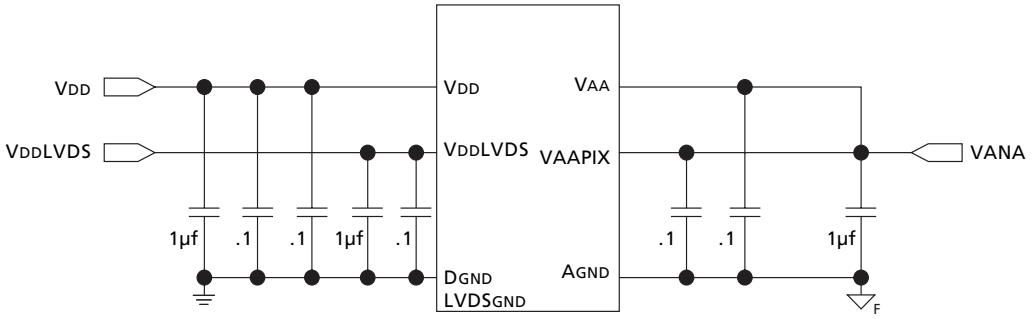
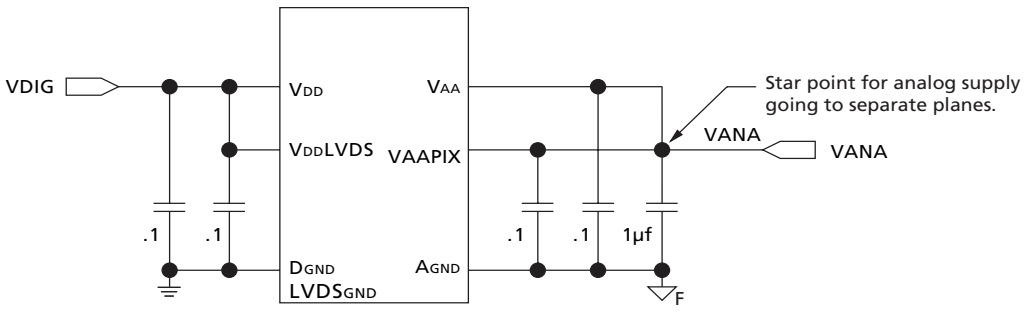


Figure 2: Minimum Bypass Capacitors



Layout

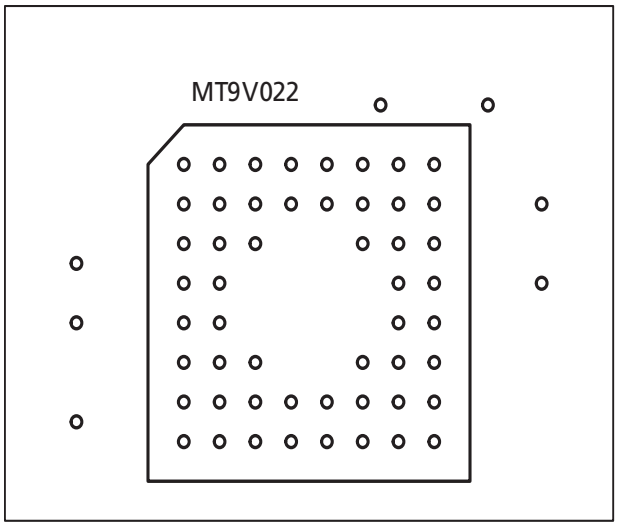
The following suggestions can help in achieving improved image sensor performance:

- A single ground plane design (common analog and digital grounds) should be used.
- When separate, analog and digital grounds should be tied together beneath the image sensor.
- Power planes should be split into analog and digital domains.
- Power supplies should be bypassed by SMT capacitors, and should not contain any inductances, especially for V_{AA} and V_{AA_PIX}.
- Analog and digital power supplies should be provided by independent voltage regulators. Analog and digital power supplies should not be tied together as this could cause high-frequency switching noise from the digital domain to couple to the analog domain.

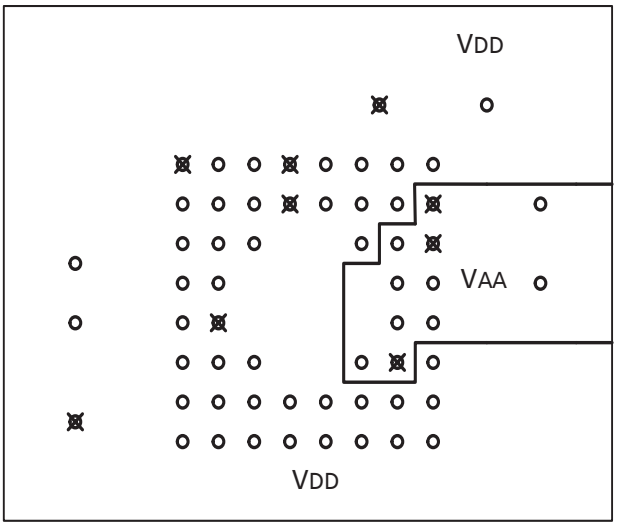
Good layout is important for system noise reduction. Traces must be kept as short as possible. Ground and power planes should be used to minimize the overall system impedances. If planes are not used, keep ground and power traces as thick as possible.

Analog signal traces and digital signal traces should be kept as far away from each other as possible. Analog signals should be routed over the analog power and ground planes. Digital signals should be routed over the digital power and ground planes. Digital components, such as the clock oscillator, should be placed over the digital ground and power planes. This routing and placement is intended to minimize clock coupling.

Figure 3: Recommended Module Configuration

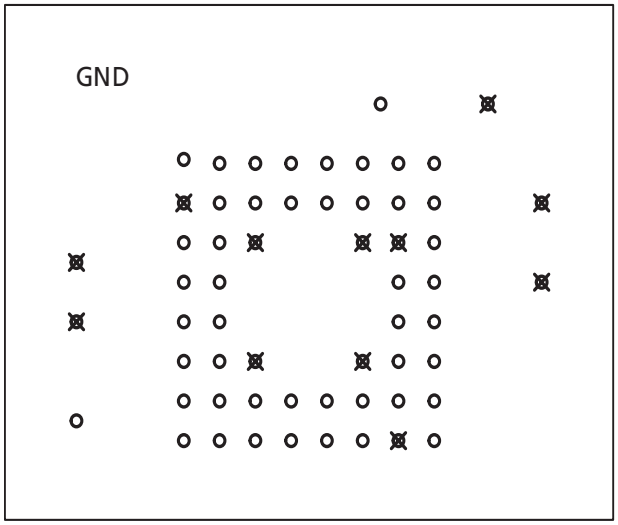


Top Layer



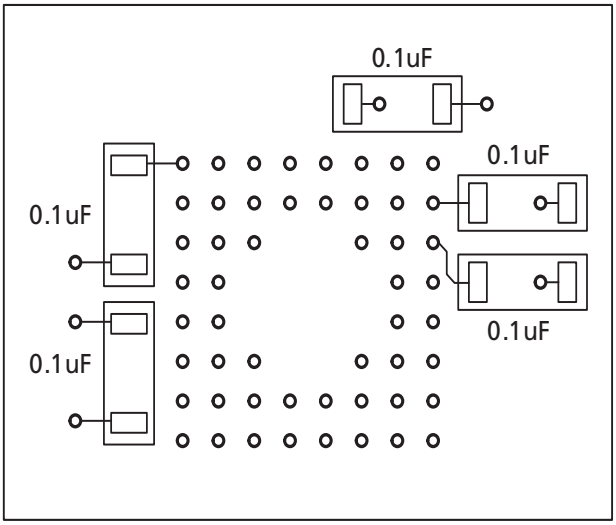
Power Plane Layer

Separate analog and digital power planes



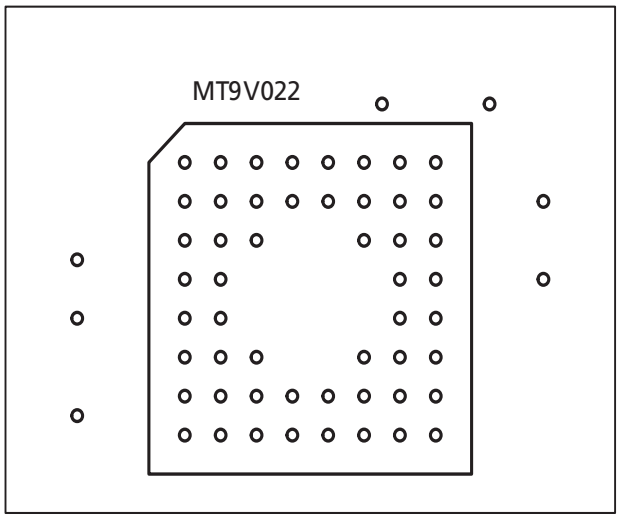
Ground Plane Layer

Recommended single ground plane

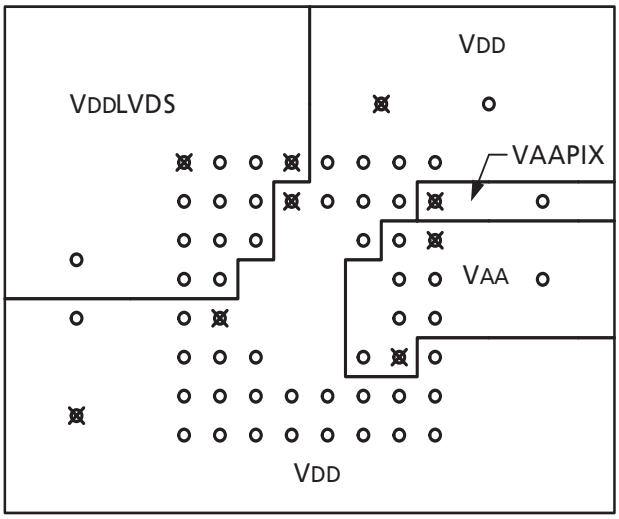


Bottom Layer

Figure 4: Alternate Module Configuration

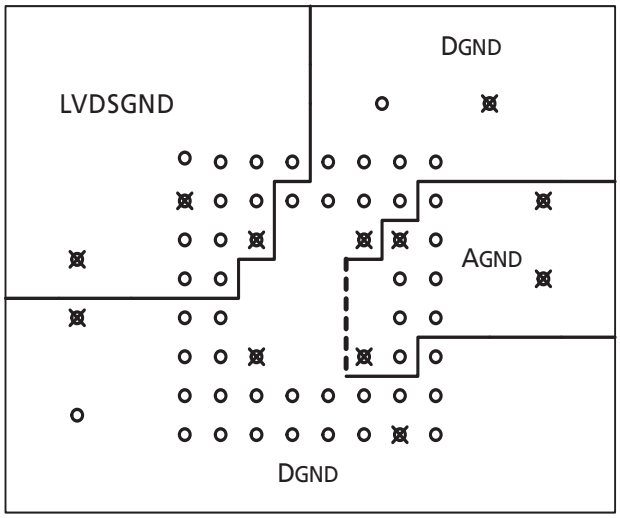


Top Layer

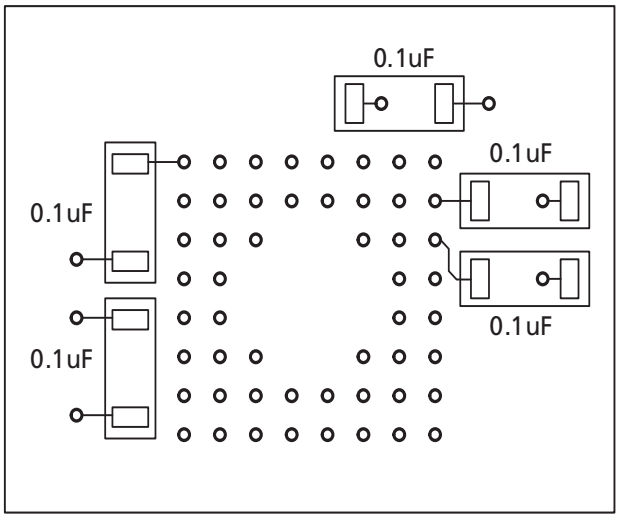


Power Plane Layer

Separate VDD and VDDLVDS is optional
Separate VAA and VAAPIX is optional



Ground Plane Layer



Bottom Layer

Recommended location to bridge AGND and DGND planes under image sensor

Separate DGND and LVDSGND is optional

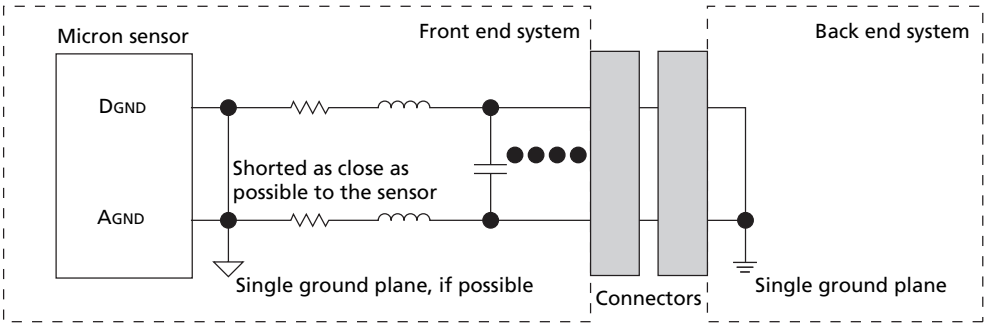
Analog Ground and Digital Ground Terminations

Depending on the availability of pins from the back-end system, either an unlimited pinout or a limited pinout approach can be selected.

Unlimited Pinout

Unlimited pinout is the best approach to minimize the ground potential between DGND and AGND. Ideally, all ground references should have the same potential (single ground point). The following suggested termination (shown in Figure 5) demonstrates that concept.

Figure 5: Unlimited Pinout Grounding Approach

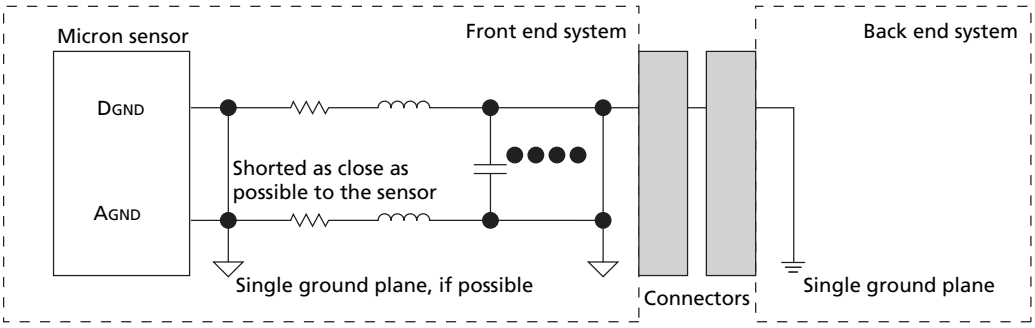


In this configuration, all resistance and inductance of these two traces was reduced at least by half; a parallel-circuit characteristic and all mutual capacitance between the traces was minimized to zero because of two shorted connections at both ends. Therefore, the DGND and AGND of the sensor have the same potential and are very close to the back-end ground potential.

Limited Pinout

Given a limited number of pins available from the back-end system, the following suggested termination is not the preferred method, but still provides an adequate grounding scheme, as shown in Figure 6.

Figure 6: Limited Pinout Grounding Approach



In this configuration, all resistance and inductance of these two traces was also reduced at least by half, and all mutual capacitance between these two traces was also minimized. However, the resistance, inductance, and capacitance of the connectors were not minimized. This would cause the sensor DGND and AGND having higher ground potential compared to the back-end ground potential.

In high clock-frequency systems, the current return path tends to follow the shortest inductance path. Since this configuration has only one ground connection between the front-end and back-end system, the DGND and AGND could have different ground potential due to the difference between current return paths. This could cause the imager to perform erratically. If the front-end has a single ground plane, this effect would be minimized. If this is not the case, design consideration for the physical layout of this pin should be carefully analyzed.

Conclusion

Several approaches can be taken while designing circuit boards, though some are more effective than others in minimizing system noise levels and reducing crosstalk. The methods for handling bypass capacitors, ground terminations, layouts, and configurations that are described in this technical note provide guidelines to consider when designing circuit boards.

For additional information, refer to Aptina's Web site at www.aptina.com.

Revision History

Rev. B **9/10**

- Updated to Aptina template

Rev. A **3/06**

- Initial release

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