

TN-09-281: AR0132 Trigger Mode Introduction

# **Technical Note**

# **AR0132 Trigger Mode Operation**

## Introduction

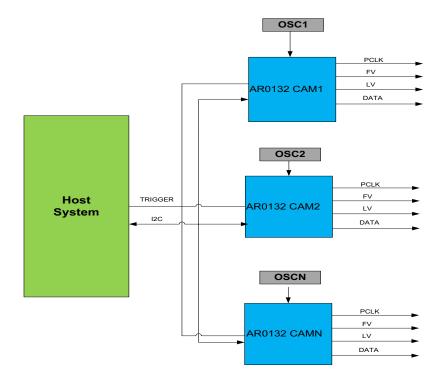
This technical note explains the supported TRIGGER modes (Pulse TRIGGER and Continuous TRIGGER mode) by the AR0132 sensor. TRIGGER mode can be used to support the synchronization of multiple cameras systems.

# **Background**

In certain applications such as stereo, surround view, and panoramic cameras, multiple sensors need to have their video streams synchronized. The AR0132 image sensor uses its TRIGGER pin to synchronize the exposure and output of multiple image sensors.

Figure 1 below shows a typical surround view system using multiple cameras. The host system provides a common TRIGGER signal to each camera. Each camera system has its own oscillator that supplies a clock to the sensor. Image output interface is shown as parallel in Figure 1, but for the AR0132 it can be either parallel or HiSPi. The host system processes the incoming image video streams from each camera in a manner specific to the application.

Figure 1: Diagram of Multiple Camera System





### **Pulse TRIGGER Mode**

The pulse TRIGGER mode outputs a single frame in response to a HIGH state placed on the TRIGGER input pin. The pin is level sensitive rather than edge sensitive. Sensor integration time (exposure) begins when the sensor detects that the TRIGGER pin has been held HIGH for three consecutive clock cycles. After integration time is complete, the sensor begins the readout of the image data. During integration time of pulse TRIGGER mode, the FLASH output pin is at HIGH.

If the TRIGGER signal is applied simultaneously to multiple sensors sharing a common configuration, the frame readout of the sensors will be synchronized to within two PIXCLK.

Table 1 lists the register settings necessary to enter the TRIGGER mode.

#### Table 1: TRIGGER Mode Register Settings

Register	Register Name	Bit	Bit Name	Bit Description	Value in Dec
0x301A	Reset Register	8	Trigger Enable	0= Trigger disabled 1= Trigger enabled	1
0x301A	Reset Register	11	Forced PLL On	0= PLL off during standby 1= PLL on during standby	1

It is recommended to set "Forced PLL On" to avoid any synchronization differences that might occur due to the PLL exiting a low-power standby state. This bit keeps the PLL always active between successive TRIGGER pulses.

Figure 2 below and Figure 3 on page 4 show the timing diagram for pulse TRIGGER mode at Linear mode and HDR mode respectively.



Figure 2: Pulse TRIGGER Mode Diagram at Linear Mode

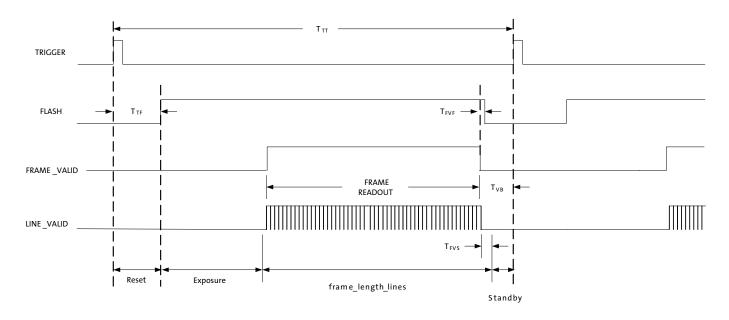


Table 2: Timing Parameters for Pulse TRIGGER Mode at Linear Mode

Symbol	Description	Value
T <sub>TPW</sub>	Pulse width of TRIGGER	>3 PIXCLK_PERIOD
Line_Length_PCK	Length of one readout line in PIXCLKs	= R0x300C
Frame_Length_Lines	Length of one readout frame in lines	= R0x300A
T <sub>TF</sub>	Rising edge of TRIGGER to rising edge of FLASH	= 7 * Line_Length_PCK * PIXCLK_PERIOD
T <sub>EXPOSURE</sub> TIME	Sensor exposure time	= R0x3012 * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FVF</sub>	Falling edge of FRAME_VALID to falling edge of FLASH	if R0x30B0[12:10]=0, = 12 PIXCLK_PERIOD if R0x30B0[12:10]>0, = ((4 + R0x30B0[12:10]) * Line_Length_PCK - 438) * PIXCLK_PERIOD
T <sub>FRAME VALID</sub>	FRAME_VALID time	= (R0x3006 - R0x3002) * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FRAME_TIME</sub>	Frame output time	=T <sub>FRAME_VALID</sub> + T <sub>VB</sub> = Frame_Length_Lines * Line_Length_PCK * PIXCLK_PERIOD
$T_{VB}$	Falling edge FRAME_VALID to next rising TRIGGER	> ((4 + R0x30B0[12:10]) * Line_Length_PCK * PIXCLK_PERIOD) + (16 * EXTCLK_PERIOD)
T <sub>FVS</sub>	Falling edge of FRAME_VALID to entering standby	= ((4 + R0x30B0[12:10]) * Line_Length_PCK * PIXCLK_PERIOD) + (16 * EXTCLK_PERIOD)
T <sub>TT</sub>	Time between successive TRIGGER pulses	> T <sub>TF</sub> + T <sub>EXPOSURE_TIME</sub> + T <sub>FRAME_VALID</sub> + T <sub>VB</sub>



Figure 3: Pulse TRIGGER Mode Diagram at HDR Mode

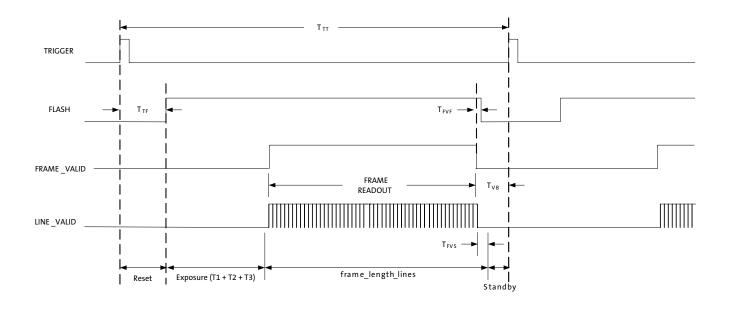


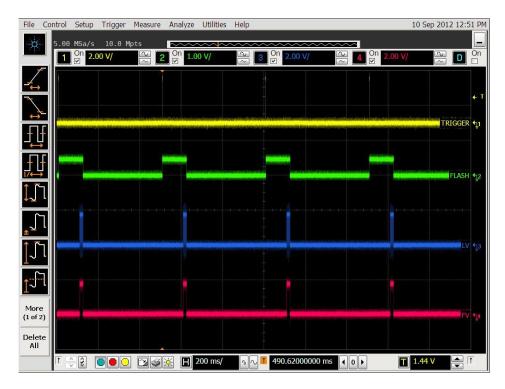
Table 3: Timing Parameters for Pulse TRIGGER Mode at HDR Mode

Symbol	Description	Value
T <sub>TPW</sub>	Pulse width of TRIGGER	>3 PIXCLK_PERIOD
Line_Length_PCK	Length of one readout line in PIXCLKs	= R0x300C
Frame_Length_Lines	Length of one readout frame in lines	= R0x300A
T <sub>TF</sub>	Rising edge of TRIGGER to rising edge of FLASH	= 7 * Line_Length_PCK * PIXCLK_PERIOD
T <sub>EXPOSURE</sub> TIME	Sensor exposure time	= (R0x3012 + R0x307C + R0x3080) * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FVF</sub>	Falling edge of FRAME_VALID to falling edge of FLASH	if R0x30B0[12:10]=0, = 12 PIXCLK_PERIOD if R0x30B0[12:10]>0, = ((4 + R0x30B0[12:10]) * Line_Length_PCK - 438) * PIXCLK_PERIOD
T <sub>FRAME VALID</sub>	FRAME_VALID time	= (R0x3006 - R0x3002) * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FRAME_TIME</sub>	Frame output time	=T <sub>FRAME_VALID</sub> + T <sub>VB</sub> = Frame_Length_Lines * Line_Length_PCK * PIXCLK_PERIOD
$T_{VB}$	Falling edge FRAME_VALID to next rising TRIGGER	> ((4 + R0x30B0[12:10]) * Line_Length_PCK * PIXCLK_PERIOD) + (16 * EXTCLK_PERIOD)
T <sub>FVS</sub>	Falling edge of FRAME_VALID to entering standby	= ((4 + R0x30B0[12:10]) * Line_Length_PCK * PIXCLK_PERIOD) + (16 * EXTCLK_PERIOD)
T <sub>TT</sub>	Time between successive TRIGGER pulses	> T <sub>TF</sub> + T <sub>EXPOSURE_TIME</sub> + T <sub>FRAME_VALID</sub> + T <sub>VB</sub>

Figure 4 on page 5 shows the scope shots of the related signals of pulse TRIGGER mode.



Figure 4: Scope Shot of Related Signals in Pulse TRIGGER Mode



# **Example Frame Rate Calculations**

Two examples follow on performing frame rate calculations for the AR0132 image sensor, shown in Table 4 below and Table 6 on page 8.

Table 4: Example 1: Shows Frame Rate for Linear Mode

Image Sensor Condition	Setting Description	Register [Bits] = Value
Exposure mode	Pulse TRIGGER	R0x301A[8] = 1
PIXCLK frequency	74.25 MHz	N/A
Line_Length_PCK	1650	R0x300C = 1650
Frame_Length_Lines	990	R0x300A = 990
Coarse Integration Time	672	R0x3012 = 672

Step 1: Calculate the exposure delay  $(T_{TF})$ .

$$exposure\_delay = \frac{7 \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
 (EQ 1)

$$exposure\_delay = \frac{7 \times 1650}{74.25 \text{ MHz}} = 155.5 \,\mu s$$
 (EQ 2)

Step 2: Calculate the frame time  $(T_{FRAME\ TIME})$ .

$$frame\_time = \frac{Frame\_Length\_Lines \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
 (EQ 3)

$$frame\_time = \frac{990 \times 1650}{74.25 \text{ MHz}} = 22 \text{ ms}$$
 (EQ 4)

Step 3: Calculate the exposure time ( $T_{\text{EXPOSURE\_TIME}}$ ).

$$exposure\_time = \frac{Coarse\_Integration\_Time \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
(EQ 5)

$$exposure\_time = \left(\frac{672 \times 1650}{74.25 \text{ MHz}}\right) = 14.93 \text{ ms}$$
 (EQ 6)

Step 4: Calculate the frame rate.

$$frame\_rate = \frac{1}{[frame\_time] + [exposure\_time + exposure\_delay]}$$
 (EQ 7)

$$frame\_rate = \frac{1}{[14.93ms] + [22ms + 155.5 \mu s]}$$
 (EQ 8)

$$frame\_rate = \frac{1}{37.09ms}$$
 (EQ 9)

$$frame\_rate = 26.96Hz$$
 (EQ 10)



Table 5: Example 2: Shows Frame Rate for HDR Mode

Image Sensor Condition	Setting Description	Register [Bits] = Value
Exposure mode	Pulse TRIGGER	R0x301A[8] = 1
PIXCLK frequency	74.25 MHz	N/A
Line_Length_PCK	1650	R0x300C = 1650
Frame_Length_Lines	990	R0x300A = 990
Coarse Integration Time	672	R0x3012 = 672
T2	42	R0x307C = 42
T3	3	R0x3080 = 3

Step 1: Calculate the exposure delay  $(T_{TF})$ .

$$exposure\_delay = \frac{7 \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
 (EQ 11)

$$exposure\_delay = \frac{7 \times 1650}{74.25 \text{ MHz}} = 155.5 \,\mu s$$
 (EQ 12)

Step 2: Calculate the frame time ( $T_{FRAME\_TIME}$ ).

$$frame\_time = \frac{Frame\_Length\_Lines \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
 (EQ 13)

$$frame\_time = \frac{990 \times 1650}{74.25 \text{ MHz}} = 22 \text{ ms}$$
 (EQ 14)

Step 3: Calculate the exposure time ( $T_{\text{EXPOSURE\_TIME}}$ ).

$$exposure\_time = \frac{(Coarse\_Integration\_Time + T2 + T3) \times Line\_Length\_PCK}{PIXCLK\_frequency}$$
 (EQ 15)

$$exposure\_time = \left(\frac{(672 + 42 + 3) \times 1650}{74.25 \text{ MHz}}\right) = 15.93 \text{ ms}$$
 (EQ 16)

Step 4: Calculate the frame rate.

$$frame\_rate = \frac{I}{[frame\_time] + [exposure\_time + exposure\_delay]}$$
(EQ 17)

$$frame\_rate = \frac{1}{[15.93ms] + [22ms + 155.5\mu s]}$$
 (EQ 18)

$$frame\_rate = \frac{1}{38.09ms}$$

$$frame\_rate = 26.25Hz$$
(EQ 19)



TN-09-281: AR0132 Trigger Mode Continuous TRIGGER Mode

#### **Continuous TRIGGER Mode**

Continuous TRIGGER mode is a mode where multiple images can be output in response to a single TRIGGER signal. It is enabled by holding the TRIGGER pin HIGH.

As long as the TRIGGER pin is held in a HIGH state, new images will be output. After the TRIGGER pin returns to a LOW state, the image sensor stops outputting any new images and waits for the next HIGH state on the TRIGGER pin. The TRIGGER pin state is detected during the vertical blanking period  $T_{\rm VB}$ ).

Figure 5 shows the timing diagram of continuous TRIGGER mode. After initial exposure time and  $T_{TF}$  completes, the first frame is read out. New frames then output continuously as long as TRIGGER signal maintains high.

Figure 5: Continuous TRIGGER Mode

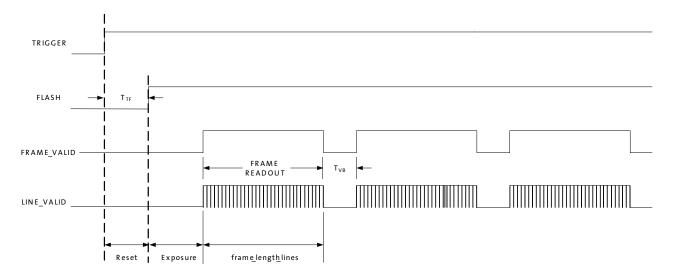


Table 6: Timing Parameters for Pulse TRIGGER Mode at Continuous Mode

Symbol	Description	Value
Line_Length_PCK	Length of one readout line in PIXCLKs	= R0x300C
Frame_Length_Lines	Length of one readout frame in lines	= R0x300A
T <sub>TF</sub>	Rising edge of TRIGGER to rising edge of FLASH	= 7 * Line_Length_PCK * PIXCLK_PERIOD
T <sub>EXPOSURE</sub> TIME	Sensor exposure time	= R0x3012 * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FRAME VALID</sub>	FRAME_VALID time	= (R0x3006 - R0x3002) * Line_Length_PCK * PIXCLK_PERIOD
T <sub>FRAME_TIME</sub>	Frame output time	= T <sub>FRAME_VALID</sub> + T <sub>VB</sub> = Frame_Length_Lines * Line_Length_PCK * PIXCLK_PERIOD
T <sub>VB</sub>	Falling edge FRAME_VALID to next rising TRIGGER	= (7 + R0x30B0[12:10] + R0x30D4[3:0]) * Line_Length_PCK * PIXCLK_PERIOD

Continuous TRIGGER mode is not recommended for camera systems where each image sensor will have different clock sources. Minor differences in output frequency between these clock sources will lead to the readouts of the later frames no longer being synchronized between all cameras. The following example shows the worst case clock drift estimation between two camera systems under the given condition.



TN-09-281: AR0132 Trigger Mode Conclusion

Table 7: Key Parameters

Condition	Setting Description	Register [Bits] = Value
Camera Oscillator	27MHz +/-50ppm	N/A
PIXCLK_PERIOD	13.47ns	N/A
Window_Height	960	R0x3006-R0x3002 = 960
Line_Length_PCK	1650	R0x300C = 1650

#### Step 1: Calculate the amount of clock frequency error.

Clock_Accuracy = 1/Nominal_Frequecy x Error	(EQ 20)
Clark Assurance 1/27MHz = 5000000 1 05200	(EO 21)

$$Clock\_Accuracy = 1/27MHz \ x \ 50ppm = 1.852ps$$
 (EQ 21)

#### Step 2: Calculate the maximum drift over one frame readout.

Frame\_Drift = Window\_Height x Line\_Length\_PCK x Clock\_Accuracy x 2 (EQ 22)
$$Frame_Drift = 960 x 1650 x 1.852ps x 2 = 5.867\mu s$$
 (EQ 23)

#### Step 3: Covert the Frame Drift to PIXCLK PERIOD.

$$Frame\_Drift = 5.867\mu s \ x \ (1 \ PIXCLK\_PERIOD)/13.46ns = 436 \ PIXCLK\_PERIOD$$
 (EQ 24)

#### **Conclusion**

This technical note describes the AR0132 TRIGGER modes (Pulse TRIGGER and Continuous TRIGGER.) Camera designs can use the TRIGGER input signal and TRIGGER mode to synchronize the output video streams from multiple image sensors.

For most applications, the pulse TRIGGER mode is the recommended mode as it provides the greatest amount of control of and synchronization between two separate cameras.

Applications where achieving the highest sustained frame rate is of most importance would find that continuous TRIGGER mode is recommended. Continuous TRIGGER synchronization can be best sustained if each camera receives the same input clock source.

For more information on this and other features, refer to the AR0132 data sheet located at Aptina's Web site at www.aptina.com.

## **Aptina Confidential and Proprietary**



TN-09-281: AR0132 Trigger Mode Revision History

<b>Revision History</b>	
Rev. A	
•	Initial release

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