Technical Note

MT9T012
Skipping and Binning Modes

Introduction

This document describes the binning and skipping mode features of Micron's MT9T012 CMOS image sensor. Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view.

Binning is a type of subsampling that gathers image data from all pixels in the active window, rather than a subset of them. It also achieves superior image quality, avoiding the aliasing artifacts that can be characteristic of subsampling.

The MT9T012 has row and column binning modes that can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by averaging the two adjacent rows and columns (adjacent same-color pixels). Both 2X skipping and binning are supported on the MT9T012.

Notes:
1. Column binning is also called x-binning; row/column binning is also called x-y binning.
2. The MT9T012 Rev 7 image sensor currently supports up to 2 x 2 skipping and binning; 3 x 3 and 4 x 4 are not recommended.

Skipping

Skipping reduces the amount of data processed by the analogue chain in the sensor, thereby allowing the frame rate to be increased. Skipping is enabled by setting _odd_inc=3 and/or y_odd_inc=3. This reduces the amount of row and column data on behalf of the skip2 readout mode.

The effect of different skipping settings on the pixel array readout is shown in Figures 1 through 5.

Figure 1: Pixel Readout (no skipping/binning)

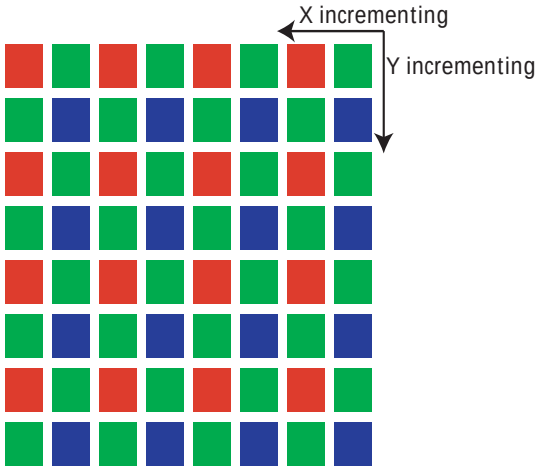


Figure 2: 2X X-Direction Skipping (x_odd_inc=3, y_odd_inc=1)

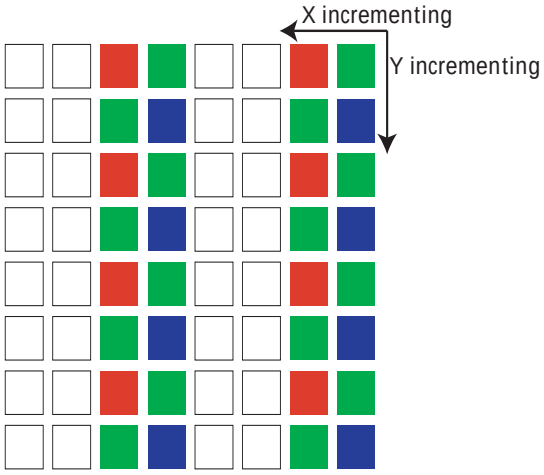


Figure 3: 2X, Y-Direction Skipping (x_odd_inc=1, y_odd_inc=3)

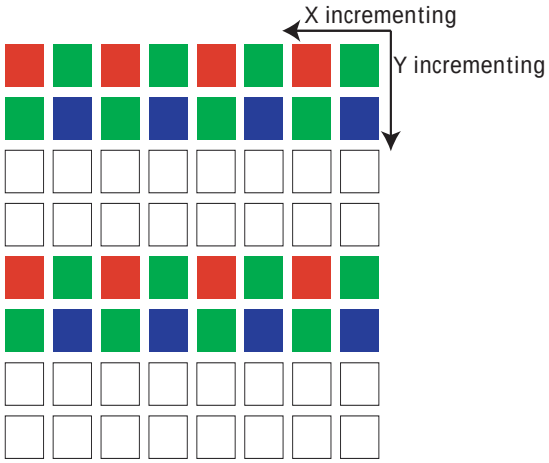


Figure 4: 2X, X-Y Direction Skipping (x_odd_inc=3, y_odd_inc=3)

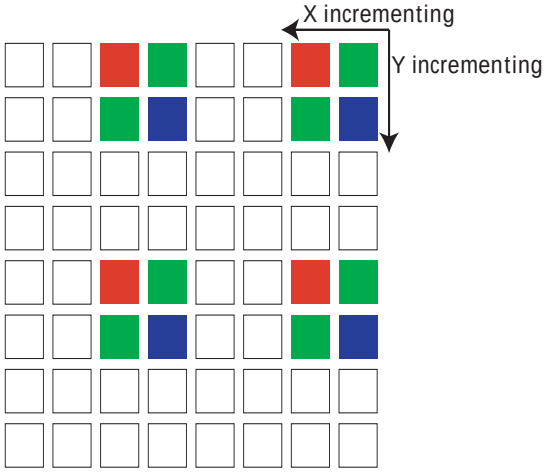
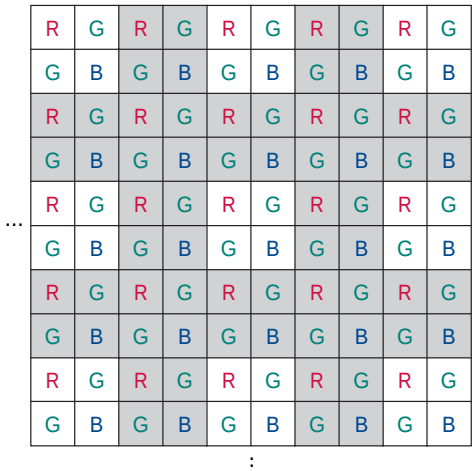


Figure 5: Simple Overview of 2X, X-Y Skipping



Binning

The MT9T012 binning is enabled by selecting the appropriate subsampling register setting. For x-binning, the register setting is x_odd_inc=3, y_odd_inc=1, and x_bin=1. For 2 x 2, xy-binning, the register setting is x_odd_inc=3, y_odd_inc=3, and xy_bin=1. These registers refer to the binning bit in read_mode (R0x3040-1). The effect of different binning settings is shown in Figure 6 and Figure 7.

Figure 6: 2X, X-Direction Binning

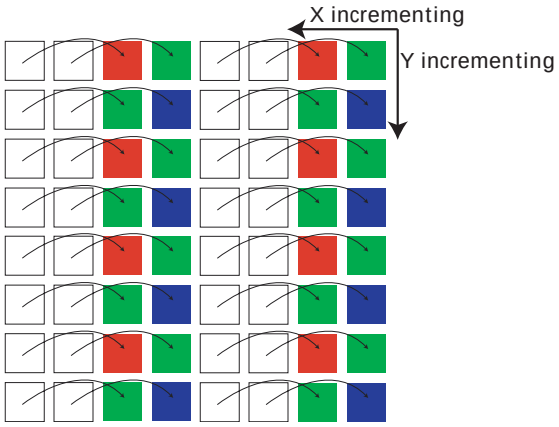
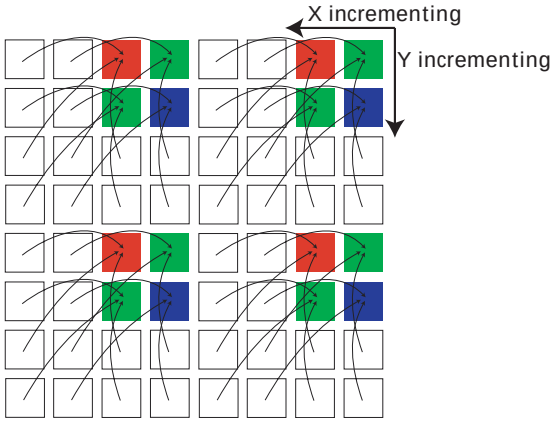


Figure 7: 2X, X-Y Direction Binning



Binning Restrictions

The following restriction applies to the MT9T012 image sensor only. Other parts may have different restrictions; refer to specific device data sheets for further information.

Binning imposes different requirements involving the sequencing of the pixel array and the timing limits on the operation of the sensor. In particular, xy-binning requires two READ operations from the pixel array for each line of output data, which increases the minimum line blanking time. The SMIA specification cannot accommodate this variation because its parameter limit registers are defined as static.

As a result, when xy-binning is enabled, some of the programming limits declared in the parameter limit registers are no longer valid. In addition, the default values for some of the manufacture-specific registers need to be reprogrammed. The recommended settings are shown in Table 1. (None of these adjustments are required for x-binning.)

Also, prior to applying the register adjustments required for binning mode (shown in Table 1), the user must disable the lock bit by first setting R0x301A bit 3 to "0." The sensor must be taken out of streaming mode before switching between binned and non-binned operation.

When xy-binning and vertical-flip are enabled, the first row in the output image is binned incorrectly. It is binned with itself instead of with the adjacent, same-color row. The result is the first row has a lower intensity than other rows in the image; this occurs for all settings of y_add_start.

Table 1: Required Register Adjustments for Binning Mode

Register Address	Register	Type	Default (Normal Readout)	Recommended Setting During Binning	Notes
0x1148	min_line_blanking_pck	Read-only	0x02AC	0x0468	Read-only register for control software; does not affect operation of sensor.
0x1144	min_line_length_pck	Read-only	0x03A8	0x05FD	Read-only register for control software; does not affect operation of sensor.
0x1008	fine_integration_time_min	Read-only	0x0204	0x03E5	Read-only register for control software; does not affect operation of sensor.
0x100A	fine_integration_time_max_margin	Read-only	0x0100	0x0215	Read-only register for control software; does not affect operation of sensor.
0x300E	sample_time_pck	Read/write	0x01EC	0x03CD	Affects operation of sensor
0x3010	fine_correction	Read/write	0x0100	0x0215	Affects operation of sensor
0x3014	fine_integration_time	Read/write	0x0204	0x03E5	Normal default is minimum value
0x1180	x_addr_min	Read-only	0	2	
0x1184	x_addr_max	Read-only	0x0807	0x0805	Keep binned column within the array
0x1182	y_addr_min	Read-only	0	0	Unchanged
0x1186	y_addr_max	Read-only	0x0607	0x0605	Keep binned row within the array

Sample Register Settings for Skipping

```
[Achieve 1024x768 by 2x2 Skipping]
REG=0x0103, 0x01                    // SOFTWARE_RESET

DELAY=300
REG=0x301A, 0x18c4                  // ENABLE PARALLEL OUTPUT
REG=0x0100, 0x0000                  // MODE_SELECT (Stop Streaming)
DELAY=300
REG=0x0104, 0x0001                  //GROUPED_PARAMETER_HOLD

// (default) timing parameters
REG=0x1148, 0x02AC                  // MIN_LINE_BLANKING_PCK
REG=0x1144, 0x03A8                  // MIN_LINE_LENGTH_PCK
REG=0x1008, 0x0204                  // FINE_INTEGRATION_TIME_MIN
REG=0x100A, 0x0100                  // FINE_INTEGRATION_TIME_MAX_MARGIN
REG=0x300E, 0x01EC                  // SAMPLE_TIME_PCK
REG=0x3010, 0x0100                  // FINE_CORRECTION
REG=0x3014, 0x0204                  // FINE_INTEGRATION_TIME_

// Configure new size
REG=0x0344, 4                       //X_Start_Addr
REG=0x0346, 4                       //Y_Start_Addr
REG=0x0348, 2049                    //X_Stop_Addr
REG=0x034A, 1537                    //Y_Stop_Addr
REG=0x382, 0x0003                   //X_ODD_INC
REG=0x386, 0x0003                   //Y_ODD_INC
REG=0x34C, 1024                     //X_OUTPUT_SIZE
REG=0x34E, 768                      //Y_OUTPUT_SIZE

// Set frame timing
REG=0x0202, 1551                    //COARSE_INTEGRATION_TIME
REG=0x0340, 1552                    //FRAME_LENGTH_LINES
REG=0x0342, 2732                    //LINE_LENGTH_PCK

//Increasing the gains
REG=0x0206, 0x0020                  // ANALOGUE_GAIN_CODE_GREENR (4x)
REG=0x0208, 0x0030                  // ANALOGUE_GAIN_CODE_RED (6x)
REG=0x020A, 0x0030                  // ANALOGUE_GAIN_CODE_BLUE (6x)
REG=0x020C, 0x0020                  // ANALOGUE_GAIN_CODE_GREENB (4x)
REG=0x104, 0x0000                   // GROUPED_PARAMETER_HOLD
REG=0x100, 0x0001                   // MODE_SELECT (Start Streaming)
```

Sample Register Settings for Binning

```
// Notes:
// Values without 0x (hexidecimal) designation are in decimal.
// Integration and gain values are samples only.

[Achieve 1024x768 by 2x2 binning]
REG=0x0103, 0x01                    // SOFTWARE_RESET
DELAY=300
REG=0x301A, 0x18c4                  // ENABLE PARALLEL OUTPUT
REG=0x0100, 0x0000                  // MODE_SELECT (Stop Streaming)

DELAY=300
REG=0x0104, 0x0001                  //GROUPED_PARAMETER_HOLD

// Binning timing parameters
REG=0x1148, 0x0468                  // MIN_LINE_BLANKING_PCK
REG=0x1144, 0x05FD                  // MIN_LINE_LENGTH_PCK
REG=0x1008, 0x03E5                  // FINE_INTEGRATION_TIME_MIN
REG=0x100A, 0x0215                  // FINE_INTEGRATION_TIME_MAX_MARGIN
REG=0x300E, 0x03CD                  // SAMPLE_TIME_PCK
REG=0x3010, 0x0215                  // FINE_CORRECTION
REG=0x3014, 0x03E5                  // FINE_INTEGRATION_TIME_

// Configure new size
REG=0x0344, 4                       //X_Start_Addr
REG=0x0346, 4                       //Y_Start_Addr
REG=0x0348, 2049                    //X_Stop_Addr
REG=0x034A, 1537                    //Y_Stop_Addr
REG=0x382, 0x0003                   //X_ODD_INC
REG=0x386, 0x0003                   //Y_ODD_INC
BITFIELD=0x3040, 0x0400, 1          // Enable binning
REG=0x34C, 1024                     //X_OUTPUT_SIZE
REG=0x34E, 768                      //Y_OUTPUT_SIZE

// Set frame timing
REG=0x0202, 1551                    //COARSE_INTEGRATION_TIME
REG=0x0340, 1552                    //FRAME_LENGTH_LINES

REG=0x0342, 2732                    //LINE_LENGTH_PCK

//Increasing the gains
REG=0x0206, 0x0020                  // ANALOGUE_GAIN_CODE_GREENR (4x)
REG=0x0208, 0x0030                  // ANALOGUE_GAIN_CODE_RED (6x)
REG=0x020A, 0x0030                  // ANALOGUE_GAIN_CODE_BLUE (6x)
REG=0x020C, 0x0020                  // ANALOGUE_GAIN_CODE_GREENB (4x)

REG=0x104, 0x0000                   // GROUPED_PARAMETER_HOLD
REG=0x100, 0x0001                   // MODE_SELECT (Start Streaming)
```

Conclusion

This technical note highlights the binning and skipping features of the MT9T012. For more information on this and other features, refer to the MT9T012, 1/3.2-inch, 3.1-megapixel CMOS digital image sensor data sheet on Micron's Web site at www.micron.com/imaging.

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Revision History

Rev A. 09/06

Initial release